INTEGRATED CIRCUITS

DATA HANDBOOK

FAST TTL Logic Series
Supplement to IC15

BOOK IC15 1989

Philips Components

PHILIPS

FAST TTL LOGIC SERIES

SUPPLEMENT

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* Supplement data supersedes Handbook IC15 data.

Function selection guide (all FAST products)

GATES

FUNCTION	DEVICE NUMBER
INVERTERS	
Hex Inverter	74F04
Hex Inverter, Schmitt Trigger	74F14
NAND	
Quad 2-Input	74F00
Triple 3-Input	74F10
Dual 4-Input, Schmitt Trigger	74F13
Dual 4-Input	74F20
8-Input	74F30
Quad 2-Input, Schmitt Trigger	74F132
13-Input	74F133
NOR	
Quad 2-Input	74F02
Triple 3-Input	74F27
Dual 5-Input	74F260
AND	
Quad 2-Input	74F08
Triple 3-Input	74F11
OR	
Quad 2-Input	74F32
EXCLUSIVE OR	
Quad 2-Input	74F86
COMBINATION	
Dual 2-Wide, 2-Input AND-OR-Invert	74F51
4-2-3-2 Input AND-OR-Invert	74F64
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Hex Inverter Buffer/Driver OC	74F06
Hex Buffer/Driver OC	74F07
Dual 4-Input NAND	74F40
Dual 4-Input NAND 30Ω Transmission Line Driver	74F3040
Quad 2-Input NAND	74F37
Quad 2-Input NAND, OC	74F38
Quad 2-Input NAND 30Ω Transmission Line Driver	74F3037
Quad 2-Input NAND 30Ω Transmission Line Driver, OC	74F3038
Hex 2-Input NAND	74F804
Hex 2-Input NAND Center Power Pin	74F1804
Hex 2-Input NOR	74F805
Hex 2-Input NOR Center Power Pin	74F1805
Hex 2-Input AND	74F808
Hex 2-Input AND Center Power Pin	74F1808
Hex 2-Input OR	74F832
Hex 2-Input OR Center Power Pin	74F1832

FLIP-FLOPS

FUNCTION	DEVICE NUMBER	PINS	CLOCK EDGE	INV	NINV
D	74F74	14	↑	X	X
D, MetastableTransparent	74F74A	14	↑	X	X
JK	74F109	16	↑	X	X
JK, Metastable Transparent	74F109A	16	↑	X	X
JK	74F112	16	↓	X	X
JK	74F113	14	↓	X	X
JK	74F114	14	↓	X	X
Dual D, Metastable Transparent	74F728	14	↑	X	X
Dual D, Metastable Transparent	74F729	14	↑	X	X
Quad D	74F173	16	↑		X
Quad D	74F175	16	↑	X	X
Hex D	74F174	16	↑		X
Hex D with Enable	74F378	16	↑		X
Octal D	74F273	20	↑		X
Octal D with Enable	74F377	20	↑		X
Octal D, 3-State	74F374	20	↑		X
Octal D, 3-State	74F534	20	↑	X	
Octal D, 3-State	74F564	20	↑	X	
Octal D, 3-State	74F574	20	↑		X
Octal D, 3-State (ACL Pinout)	74F11374	24	↑		X

REGISTERS/REGISTER FILES

FUNCTION	DEVICE NUMBER	BITS	CLOCK
Quad Parallel Register	74F379	4	↑
Quad Two Port	74F398	4X2	↑
Quad Two Port	74F399	4X2	↑
Dual Octal	74F604	8X2	↑
Dual Octal	74F605	8X2	↑
Octal Mail Box Register	74F755	8	↑
8-Bit, Inverting	74F826	8	↑
8-Bit, Non-Inverting	74F825	8	↑
9-Bit, Inverting	74F824	9	↑
9-Bit, Non-Inverting	74F823	9	↑
10-Bit, Inverting	74F822	10	↑
10-Bit, Non-Inverting	74F821	10	↑
Register File	74F670	4X4	↑

FAST Function Selection Guide

LATCHES

FUNCTION	DEVICE NUMBER	PINS	NINV	INV	3-STATE
Dual 4-Bit Addressable	74F256	16	X		
Dual 4-Bit Addressable	74F259	16	X		
Dual Octal Latch	74F1604	28	X		
Octal	74F373	20	X		X
8-Bit	74F533	20		X	X
8-Bit Transparent	74F563	20		X	X
8-Bit Transparent	74F573	20	X		X
8-Bit (ACL Pinout)	74F11373	24	X		X
8-Bit	74F846	24		X	X
8-Bit	74F845	24	X		X
9-Bit	74F844	24		X	X
9-Bit	74F843	24	X		X
10-Bit	74F842	24		X	X
10-Bit	74F841	24	X		X
8-Bit Multimode Buffered	74F412	24	X		X
8-Bit Multimode Buffered	74F432	24		X	X

MULTIPLEXERS/ENCODERS

FUNCTION	DEVICE NUMBER	NINV	INV	3-STATE
Dual 4-Input	74F153	X		
Dual 4-Input	74F253	X		
Dual 4-Input	74F352	X		
Dual 4-Input	74F353	X		X
Quad 2-Input	74F157/157A	X		
Quad 2-Input	74F158/158A		X	
Quad 2-Input	74F257/257A	X		X
Quad 2-Input	74F258/258A		X	X
Quad 2-Input	74F298	X		
Quad 3-Input	74F723	X	X	X
Quad 3-Input with 30Ω Termination	74F723-1	X	X	X
Quad 4-Input	74F725	X		
Quad 4-Input with 30Ω Termination	74F725-1	X		
Quad Data Multiplexers	74F732			X
Quad Data Multiplexers	74F733	X	X	X
Quint 2-Input	74F711	X	X	X
Quint 2-Input with 30Ω Termination	74F711-1	X	X	X
Quint 3-Input	74F712	X		
Quint 3-Input with 30Ω Termination	74F712-1	X		
8-Input	74F151/151A	X	X	
8-Input	74F251/251A	X	X	X
8-to-3 Priority Encoder	74F148		X	

DEMULTIPLEXERS/DECODERS

FUNCTION	DEVICE NUMBER
Dual 1-of-4	74F139
Dual 1-of-4	74F539
1-of-8	74F138
1-of-8	74F538
Octal with Address Latch and Acknowledge	74F547
Octal with Acknowledge	74F548
1-of-10	74F537
1-of-16	74F154

BUFFERS

FUNCTION	DEVICE NUMBER	PINS	NINV/INV	3-STATE/OC
Quad Buffer	74F125	14	NINV	3-State
Quad Buffer	74F126	14	NINV	3-State
Hex Buffer	74F365	16	NINV	3-State
Hex Buffer	74F366	16	INV	3-State
Hex Buffer	74F367	16	NINV	3-State
Hex Buffer	74F368	16	INV	3-State
Octal Buffer	74F240	20	INV	3-State
Octal Buffer	74F241	20	NINV	3-State
Octal Buffer	74F244	20	NINV	3-State
Octal Buffer	74F540	20	INV	3-State
Octal Buffer	74F541	20	NINV	3-State
Octal Buffer	74F756	20	INV	OC
Octal Buffer	74F757	20	NINV	OC
Octal Buffer	74F760	20	NINV	OC
Octal Buffer (ACL Pinout)	74F11240	24	INV	3-State
Octal Buffer (ACL Pinout)	74F11244	24	NINV	3-State
Octal Buffer	74F1240	20	INV	3-State
Octal Buffer	74F1241	20	NINV	3-State
Octal Buffer	74F1244	20	NINV	3-State
Octal 30Ω Transmission Line/Backplane Driver	74F30240	24	INV	OC
Octal 30Ω Transmission Line/Backplane Driver	74F30244	24	NINV	OC
Octal Buffer with Parity	74F455	24	INV	3-State
Octal Buffer with Parity	74F456	24	NINV	3-State
Octal Buffer with Parity	74F655A	24	INV	3-State
Octal Buffer with Parity	74F656A	24	NINV	3-State
10-Bit Buffer	74F827	24	NINV	3-State
10-Bit Buffer	74F828	24	INV	3-State

TRANSCEIVERS

FUNCTION	DEVICE NUMBER	PINS	NINV/INV	3-STATE/OC
Quad Transceiver	74F242	14	INV	3-State
Quad Transceiver	74F243	14	NINV	3-State
Quad Transceiver	74F1242	14	INV	3-State
Quad Transceiver	74F1243	14	NINV	3-State
Octal Transceiver	74F245	20	NINV	3-State
Octal Transceiver	74F545	20	NINV	3-State
Octal Transceiver with IEEE-488 Termination Resistor	74F588	20	NINV	3-State
Octal Transceiver	74F620	20	INV	3-State
Octal Transceiver	74F621	20	NINV	OC
Octal Transceiver	74F622	20	INV	OC
Octal Transceiver	74F623	20	NINV	3-State
Octal Transceiver	74F640	20	INV	3-State
Octal Transceiver	74F641	20	NINV	OC
Octal Transceiver	74F642	20	INV	OC
Octal Transceiver	74F1245	20	NINV	3-State
Octal 30Ω Transmission Line/Backplane Transceiver	74F30245	24	NINV	A(3-State),B(OC)
Octal 30Ω Transmission Line/Backplane Transceiver	74F30640	24	INV	A(3-State),B(OC)
Octal Latched Transceiver	74F543	24	NINV	3-State
Octal Latched Transceiver	74F544	24	INV	3-State
Dual Latched Transceiver with Parity	74F899	28	NINV	3-State
Octal Latched Transceiver (ACL Pinout)	74F11543	28	NINV	3-State
Octal Latched Transceiver (ACL Pinout)	74F11544	28	INV	3-State
Octal Registered Transceiver with Parity and Status Flags	74F552	28	NINV	3-State
Octal Transceiver/Register	74F646/646A	24	NINV	3-State
Octal Transceiver/Register	74F647	24	NINV	OC
Octal Transceiver/Register	74F648/648A	24	INV	3-State
Octal Transceiver/Register	74F649	24	INV	OC
Octal Transceiver/Register	74F651/651A	24	INV	3-State
Octal Transceiver/Register	74F652/652A	24	NINV	3-State
Octal Transceiver/Register	74F653	24	INV	OC
Octal Transceiver/Register	74F654	24	NINV	OC
Octal Transceiver/Register (ACL Pinout)	74F11646	28	NINV	3-State
Octal Transceiver/Register (ACL Pinout)	74F11648	28	INV	3-State
Octal Transceiver/Register (ACL Pinout)	74F11651	28	INV	3-State
Octal Transceiver/Register (ACL Pinout)	74F11652	28	NINV	3-State
8-Bit Registered Transceiver	74F2952	24	NINV	3-State
8-Bit Registered Transceiver	74F2953	24	INV	3-State
Octal Transceiver with Parity	74F657/657A	24	NINV	3-State
9-Bit Transceiver	74F864	24	INV	3-State
9-Bit Transceiver	74F863	24	NINV	3-State
10-Bit Transceiver	74F862	24	INV	3-State
10-Bit Transceiver	74F861	24	NINV	3-State
Pi-Bus Transceiver	74F776	28	NINV	OC
Futurebus Transceiver	74F8960	28	INV	OC
Futurebus Transceiver	74F8961	28	NINV	OC
High Speed Quad Backplane Transceiver	74F3893	20	NINV	OC

SHIFT REGISTERS

BITS	SERIAL IN	PARALLEL IN	SERIAL OUT	PARALLEL OUT	DEVICE NUMBER	CLOCK	COMMENTS
4	X	X		X	74F194	↑	
4	X	X	X	X	74F195	↑	
4		X		X	74F350		Shift Right, 3-State
4	X	X		X	74F395	↑	Shift Right, 3-State
8	X			X	74F164	↑	
8	X	X		X	74F166	↑	
8	X	X		X	74F198	↑	Bidirectional
8	X	X		X	74F199	↑	Shift Right
8	X	X	X	X	74F299	↑	3-State
8	X	X	X	X	74F322	↑	3-State
8	X	X	X	X	74F323	↑	3-State
8	X			X	74F595	↑	Output Latch, 3-State
8		X	X		74F597	↑	Input Latches
8	X	X	X	X	74F598	↑	Input Latches, 3-State
8	X	X	X		74F739	↑	2:1 Mux-in, Shift Right
8	X	X	X		74F835	↑	2:1 Mux-In, Latched 'B' Inputs
10/9	X	X	X		74F847	↑	
16	X		X	X	74F674	↓	
16	X	X	X		74F676	↓	

COUNTERS

FUNCTION	DEVICE NUMBER	TYPE	PRESETTABLE	PARALLEL ENTRY	CLOCK
Synchronous	74F160A	Decade	X	S	↑
Synchronous	74F162A	Decade	X	S	↑
Up/Down	74F168	Decade	X	S	↑
Up/Down	74F190	Decade	X	A	↑
Up/Down	74F192	Decade	X	A	↑
Up/Down, 3-State	74F568	Decade	X	S	↑
Synchronous	74F161A	BCD	X	S	↑
Synchronous	74F163A	BCD	X	S	↑
Up/Down	74F169	BCD	X	S	↑
Up/Down	74F191	BCD	X	A	↑
Up/Down	74F193	BCD	X	A	↑
Up/Down, 3-State	74F569	BCD	X	S	↑
Ripple	74F393	BCD			↓
Up/Down, 3-State	74F269	8-Bit	X	S	↑
Up/Down, 3-State	74F579	8-Bit	X	S(I/O)	↑
Up/Down, 3-State	74F779/779A	8-Bit	X	S(I/O)	↑

PARITY CHECKERS

FUNCTION	DEVICE NUMBER
9-Bit Odd/Even Parity Generator/Checker	74F280A/B
Octal Buffer with Parity	74F455
Octal Buffer with Parity	74F456
Octal Buffer with Parity	74F655A
Octal Buffer with Parity	74F656A
Octal Transceiver with Parity	74F657/657A
Octal Latched Tranceiver with Parity	74F899

ARITHMETIC FUNCTIONS

FUNCTION	DEVICE NUMBER
4-Bit ALU	74F181
4-Bit ALU	74F381
4-Bit ALU with Overflow Output for Two's Complement	74F382
ALU/Function Generator	74F881
4-Bit Binary Full Adder	74F83
4-Bit Binary Full Adder	74F283
Look-Ahead Carry Generator	74F182
Look-Ahead Carry Generator	74F882
Quad Serial Adder	74F385
4-Bit BCD ALU	74F582
4-Bit BCD Adder	74F583

COMPARATORS

FUNCTION	DEVICE NUMBER
4-Bit Comparator	74F85
8-Bit Comparator	74F521
8-Bit Registered Comparator	74F524

LSI DRAM CONTROLLERS

FUNCTION	DEVICE NUMBER	PORTS	MIN. ACCESS TIME (NS)	PAGE MODE	ADDRESS LATCHES	PACKAGE AND PIN COUNT DIP AND PLCC
256K DRAM Dual Ported Controller	74F764	2	40	No	Yes	DIP-40, PLCC-44
256K DRAM Dual Ported Controller	74F764-1	2	40	No	Yes	DIP-40, PLCC-44
256K DRAM Dual Ported Controller	74F765	2	40	No	No	DIP-40, PLCC-44
256K DRAM Dual Ported Controller	74F765-1	2	40	No	No	DIP-40, PLCC-44
DRAM and Interrupt Vector Controller	74F1761	1	40	No	N/A	DIP-48, PLCC-44
4-Mbit Memory Address Multiplexer	74F1762	N/A	N/A	N/A	No	DIP-40, PLCC-44
1-Mbit Intelligent DRAM Controller	74F1763	1	40	Yes	Yes	DIP-48, PLCC-44
1-Mbit DRAM Dual Ported Controller	74F1764	2	40	No	Yes	DIP-48, PLCC-44
1-Mbit DRAM Dual Ported Controller	74F1764-1	2	40	No	Yes	DIP-48, PLCC-44
1-Mbit DRAM Dual Ported Controller	74F1765	2	40	No	No	DIP-48, PLCC-44
1-Mbit DRAM Dual Ported Controller	74F1765-1	2	40	No	No	DIP-48, PLCC-44

RAMS

FUNCTION	DEVICE NUMBER	NINV	INV	3-STATE
64-Bit	74F189A		X	X
64-Bit	74F219A	X		X
Register Stack, 16X4 RAM	74F410			X

FIFOs

FUNCTION	DEVICE NUMBER	TYPICAL Fmax (MHZ)	3-STATE
16X4 Synchronous FIFO	74F222	30	3-State
16X4 Synchronous FIFO	74F224	30	3-State
16X5 Asynchronous FIFO	74F225	30	3-State

SPECIAL FUNCTIONS

FUNCTION	DEVICE NUMBER
4-Input Asynchronous Bus Arbiter	74F786
Microprogram Sequence Controller	74F838

Data sheet location and product status reference list

Data sheet location and product status reference list

type 74F..	location of latest data	product status	type 74F..	location of latest data	product status
00	IC15	F	157A	IC15	F
02	IC15	F	158A	IC15	F
04	IC15	F	160A	IC15	F
06	supplement	F	161A	IC15	F
07	supplement	F	162A	IC15	F
08	IC15	F	163A	IC15	F
10	IC15	F	164	supplement	F
11	IC15	F	166	IC15	F
13	IC15	F	168	IC15	F
14	IC15	F	169	IC15	F
20	IC15	F	173	IC15	F
27	IC15	F	174	IC15	F
30	IC15	F	175	IC15	F
32	IC15	F	181	IC15	F
37	IC15	F	182	IC15	F
38	IC15	F	189A	supplement	F
40	IC15	F	190	IC15	F
51	IC15	F	191	IC15	F
64	IC15	F	192	IC15	F
74	IC15	F	193	IC15	F
74A	supplement	P	194	IC15	F
83	IC15	F	195	IC15	F
85	IC15	F	198	supplement	F
86	IC15	F	199	supplement	F
109	IC15	F	219A	supplement	F
109A	supplement	P	222	supplement	P
112	IC15	F	224	supplement	P
113	IC15	F	225	supplement	P
114	IC15	F	240	IC15	P
125	IC15	F	241	IC15	F
126	IC15	F	242	IC15	F
132	IC15	F	243	IC15	F
133	IC15	F	244	IC15	F
138	IC15	F	245	IC15	F
139	IC15	F	251	IC15	F
148	IC15	F	251A	IC15	F
151	IC15	F	253	IC15	F
151A	IC15	F	256	IC15	F
153	IC15	F	257	IC15	F
154	supplement	F	257A	IC15	F

F = final product specification for a released product.
P = preliminary specification for a product in development.

Data sheet location and product status reference list

type 74F..	location of latest data	product status	type 74F..	location of latest data	product status
258A	IC15	F	537	IC15	F
259	IC15	F	538	IC15	F
260	IC15	F	539	IC15	F
269	IC15	F	540	IC15	F
273	IC15	F	541	IC15	F
280A	IC15	F	543	IC15	F
280B	IC15	F	544	IC15	F
283	IC15	F	545	IC15	F
298	IC15	F	547	supplement	F
299	IC15	F	548	IC15	F
322	supplement	F	552	supplement	F
323	IC15	F	563	supplement	F
350	IC15	F	564	supplement	F
352	IC15	F	568	IC15	F
353	IC15	F	569	IC15	F
365	IC15	F	573	supplement	F
366	IC15	F	574	supplement	F
367	IC15	F	579	IC15	F
368	IC15	F	582	IC15	F
373	IC15	F	583	IC15	F
374	IC15	F	588	IC15	F
377	IC15	F	595	supplement	F
378	IC15	F	597	IC15	P
379	IC15	F	598	IC15	P
381	IC15	F	604	IC15	F
382	IC15	F	605	IC15	F
385	IC15	F	620	IC15	F
393	IC15	F	621	IC15	F
395	IC15	F	622	IC15	F
398	IC15	F	623	IC15	F
399	IC15	F	640	IC15	F
410	supplement	F	641	IC15	F
412	IC15	F	642	IC15	F
432	IC15	F	646	supplement	F
455	IC15	F	646A	supplement	P
456	IC15	F	647	IC15	F
521	IC15	F	648	supplement	F
524	IC15	F	648A	supplement	P
533	IC15	F	649	IC15	F
534	IC15	F	651	supplement	F

F = final product specification for a released product.
P = preliminary specification for a product in development.

Data sheet location and product status reference list

type 74F..	location of latest data	product status
651A	supplement	P
652	supplement	F
652A	supplement	P
653	IC15	F
654	IC15	F
655A	IC15	F
656A	IC15	F
657	supplement	F
657A	supplement	P
670	supplement	F
674	supplement	F
676	IC15	F
711	supplement	P
711-1	supplement	P
712	supplement	P
712-1	supplement	P
723	supplement	P
723-1	supplement	P
725	supplement	P
725-1	supplement	P
728	supplement	P
729	supplement	P
732	supplement	F
733	supplement	F
739	supplement	P
755	supplement	F
756	supplement	F
757	supplement	F
760	supplement	F
764	IC15	F
764-1	IC15	P
764A	IC15	P
765	supplement	F
765-1	supplement	P
765A	IC15	P
776	supplement	F
779	IC15	F
779A	supplement	P
786	supplement	F
804	supplement	F
805	supplement	P
808	supplement	P
821	supplement	F
822	supplement	F
823	supplement	F
824	supplement	F
825	supplement	F
826	supplement	F
827	IC15	F
828	IC15	F
832	supplement	P
835	supplement	F
838	supplement	P
841	supplement	F
842	supplement	F
843	supplement	F
844	supplement	F
845	supplement	F
846	supplement	F
847	supplement	P
861	IC15	F
862	IC15	F
863	IC15	F
864	IC15	F
881	IC15	F
882	IC15	F
899	supplement	P
1240	IC15	F
1241	IC15	F
1242	IC15	F
1243	IC15	F
1244	IC15	P
1245	IC15	P
1604	supplement	P
1761	supplement	P
1762	supplement	F
1763	supplement	P
1764	IC15	P
1764-1	IC15	P
1765	IC15	P

F = final product specification for a released product.
P = preliminary specification for a product in development.

Data sheet location and product status reference list

type 74F..	location of latest data	product status	type 74F..	location of latest data	product status
1765-1	IC15	P	8961	supplement	F
1804	supplement	F	11240	supplement	P
1805	supplement	P	11244	supplement	P
1808	supplement	P	11373	supplement	P
1832	supplement	P	11374	supplement	P
2952	supplement	F	11543	supplement	P
2953	supplement	F	11544	supplement	P
3037	IC15	F	11646	supplement	P
3038	IC15	F	11648	supplement	P
3040	IC15	F	11651	supplement	P
3893	supplement	P	11652	supplement	P
8960	supplement	P			

F = final product specification for a released product.
P = preliminary specification for a product in development.

Supplement data sheets

FAST 74F06, 74F07 Inverter/Buffer/Drivers

'F06 Hex Inverter Buffer/Driver (Open Collector)
'F07 Hex Buffer/Driver (Open Collector)

FEATURES

- **Open Collector output drive 64mA**
- **High speed**
- **12V output termination voltage**
- **Symmetrical propagation delays**

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F06	3.5ns	18mA
74F07	4.5ns	21mA

ORDERING INFORMATION

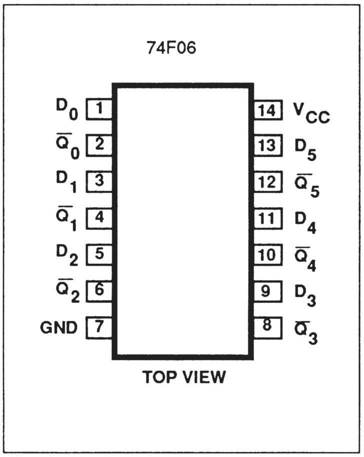
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F06N, N74F07N
14-Pin Plastic SO	N74F06D, N74F07D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

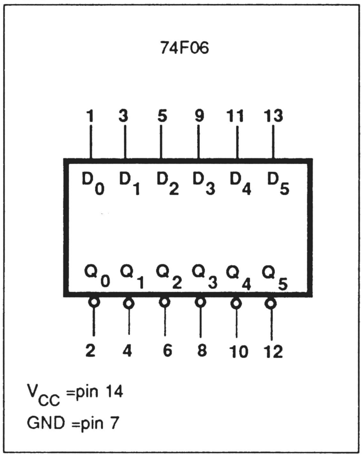
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_n	Data input	1.0/1.0	20µA/0.6mA
$\overline{Q}_n$	Data output ('F06)	OC/106.7	OC/64mA
Q_n	Data output ('F07)	OC/106.7	OC/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
2. OC = Open Collector.

PIN CONFIGURATION

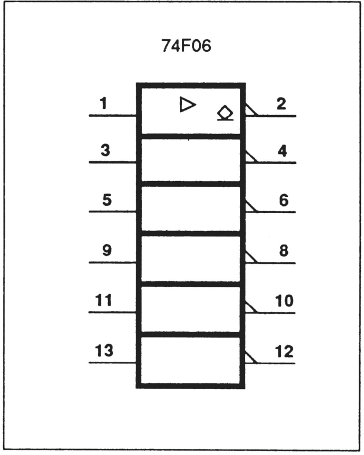

74F06
D_0 1
$\overline{Q}_0$ 2
D_1 3
$\overline{Q}_1$ 4
D_2 5
$\overline{Q}_2$ 6
GND 7
8 $\overline{Q}_3$
9 D_3
10 $\overline{Q}_4$
11 D_4
12 $\overline{Q}_5$
13 D_5
14 V_{CC}
TOP VIEW

LOGIC SYMBOL

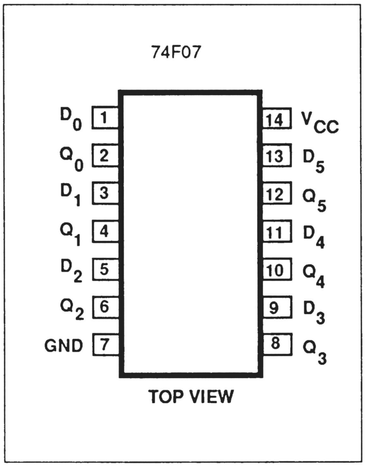

74F06
1 3 5 9 11 13
D_0 D_1 D_2 D_3 D_4 D_5
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5
2 4 6 8 10 12

V_{CC} =pin 14
GND =pin 7

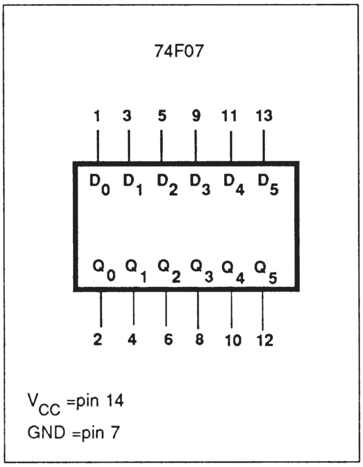
LOGIC SYMBOL(IEEE/IEC)


74F06
1
2
3
4
5
6
9
8
11
10
13
12

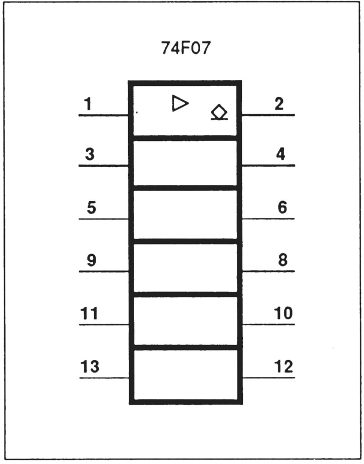
PIN CONFIGURATION


74F07
D0 1
Q0 2
D1 3
Q1 4
D2 5
Q2 6
GND 7
14 VCC
13 D5
12 Q5
11 D4
10 Q4
9 D3
8 Q3
TOP VIEW

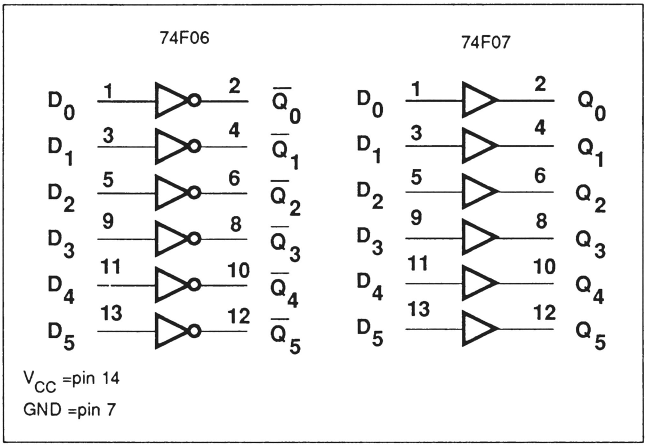
LOGIC SYMBOL


74F07
1 3 5 9 11 13
D0 D1 D2 D3 D4 D5
Q0 Q1 Q2 Q3 Q4 Q5
2 4 6 8 10 12
VCC =pin 14
GND =pin 7

LOGIC SYMBOL(IEEE/IEC)


74F07
1
2
3
4
5
6
9
8
11
10
13
12

LOGIC DIAGRAM


74F06
D0 1 2 Q̅0
D1 3 4 Q̅1
D2 5 6 Q̅2
D3 9 8 Q̅3
D4 11 10 Q̅4
D5 13 12 Q̅5
VCC =pin 14
GND =pin 7
74F07
D0 1 2 Q0
D1 3 4 Q1
D2 5 6 Q2
D3 9 8 Q3
D4 11 10 Q4
D5 13 12 Q5

FUNCTION TABLE

INPUTS	OUTPUTS	
	74F06	74F07
D_n	$\overline{Q}_n$	Q_n
L	H	L
H	L	H

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +12	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	High-level output voltage			12	V
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		74F06, 74F07			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current			V_{CC} = MIN, V_{IL} = MAX, V_{OH} =MAX, V_{IH} = MIN				250	µA
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, I_{OL} =MAX V_{IH} = MIN	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{CC}	Supply current (total)	74F06	I_{CCH}	V_{CC} = MAX			5.0	8.0	mA
			I_{CCL}				30	43	mA
		74F07	I_{CCH}				10	14	mA
			I_{CCL}				32	45	mA

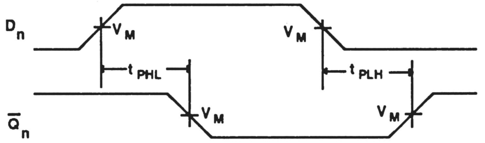
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

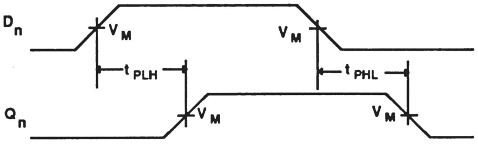
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 100Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 100Ω		
				Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay D_n to $\overline{Q}_n$	74F06	Waveform 1	2.0	3.5	6.0	1.5	6.5	ns
t_{PHL}				1.5	3.0	5.5	1.0	6.0	
t_{PLH}	Propagation delay D_n to Q_n	74F07	Waveform 2	2.0	4.0	6.0	2.0	6.5	ns
t_{PHL}				3.0	5.0	7.0	2.5	7.5	

AC WAVEFORMS


D_n
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Q}_n$
V_M
V_M

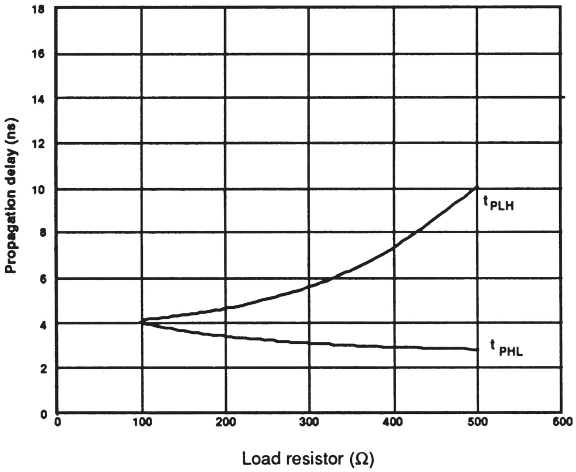
Waveform 1. Propagation Delay For inverting outputs


D_n
V_M
V_M
t_{PLH}
t_{PHL}
Q_n
V_M
V_M

Waveform 2. Propagation Delay For non-inverting outputs

NOTE: For all waveforms, $V_M = 1.5V$.

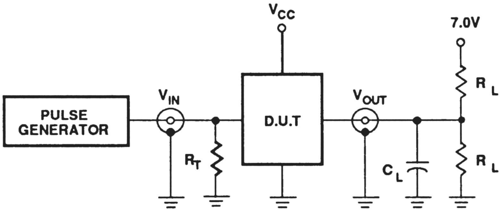
TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



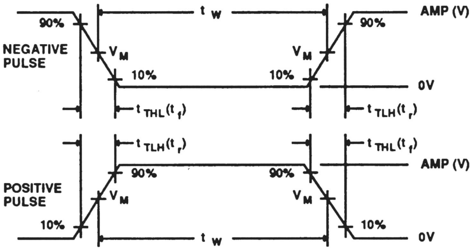
NOTE:

When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
7.0V
R_L
PULSE GENERATOR
V_{IN}
D.U.T
V_{OUT}
R_T
C_L
R_L

Test Circuit for Open Collector Outputs


t_w
AMP (V)
90%
90%
NEGATIVE PULSE
V_M
V_M
10%
10%
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
0V
t_w

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F74A
FLIP-FLOP

Synchronizing Dual D-Type Flip-Flop

Preliminary Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F74A	200 MHz	10mA

FEATURES

- **Metastable Immune Characteristics**
- **Same pinout and function as 74F74**
- **See 74F728 for Synchronizing Cascaded D-Type Flip-Flop**
- **See 74F729 for Synchronizing Cascaded Dual D-Type Flip-Flop with Edge-Triggered Set and Reset**
- **See 74F109A for Synchronizing Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flops**

DESCRIPTION

The 74F74A is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also true and complementary outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-Low inputs and operate independently of the Clock (CP) input. Data must be stable just one setup time prior to the Low-to-High transition of the clock for guaranteed propagation delays.

Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D input may be changed without affecting the levels of the output.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F74AN
14-Pin Plastic SO	N74F74AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

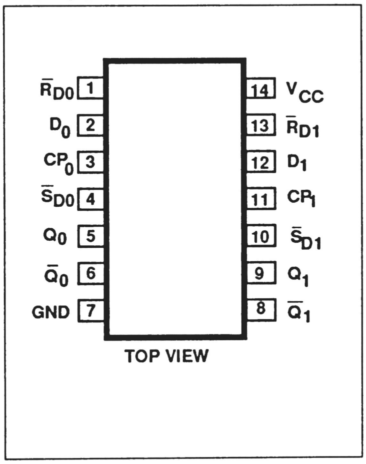
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0, D_1	Data inputs	1.0/0.166	20μA/100μA
CP_0, CP_1	Clock inputs (active rising edge)	1.0/0.083	20μA/50μA
$\overline{S}_{D0}$, $\overline{S}_{DI}$	Set inputs (active Low)	1.0/0.083	20μA/50μA
$\overline{R}_{D0}$, $\overline{R}_{DI}$	Reset inputs (active Low)	1.0/0.083	20μA/50μA
Q_0, Q_I, $\overline{Q}_0$, $\overline{Q}_I$	Data outputs	50/33	1.0mA/20mA

NOTE:

One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

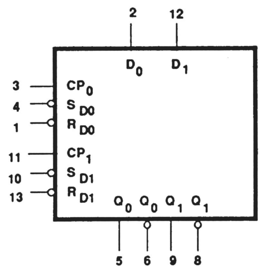
The 74F74A is designed so that the outputs can never display a metastable state due to setup and hold times violations. If setup and hold times are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F74A are: $\tau < .100$ns, T_0=1μs, and h=3.3ns.

PIN CONFIGURATION



$\overline{R}_{D0}$ 1
D_0 2
CP_0 3
$\overline{S}_{D0}$ 4
Q_0 5
$\overline{Q}_0$ 6
GND 7
14 V_{CC}
13 $\overline{R}_{D1}$
12 D_1
11 CP_1
10 $\overline{S}_{D1}$
9 Q_1
8 $\overline{Q}_1$
TOP VIEW

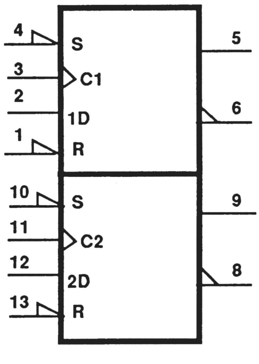
LOGIC SYMBOL



2
12
D_0
D_1
3
4
1
CP_0
S_{D0}
R_{D0}
11
10
13
CP_1
S_{D1}
R_{D1}
Q_0 $\overline{Q}_0$ Q_1 $\overline{Q}_1$
5
6
9
8

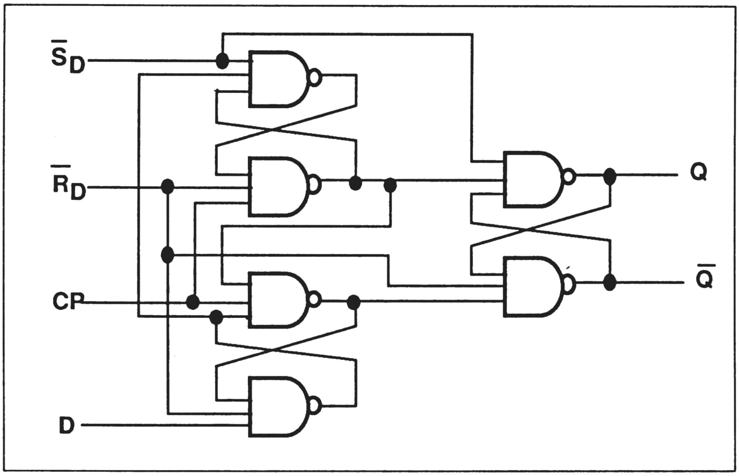
V_{CC} =pin 14
GND =pin 7

LOGIC SYMBOL(IEEE/IEC)



4
3
2
1
S
C1
1D
R
5
6
10
11
12
13
S
C2
2D
R
9
8

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$	
L	H	X	X	H	L	Asynchronous Set
H	L	X	X	L	H	Asynchronous Reset
L	L	X	X	H	H	Undetermined*
H	H	↑	h	H	L	Load "1"
H	H	↑	l	L	H	Load "0"
H	H	↥	X	NC	NC	Hold

H = High voltage level
h-= High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
↥ = Low-to-High clock transition
NC =No change from the previous setup
* = The output in this configuration is not guaranteed to meet the minimum V_{OH} levels when Set and Reset are near V_{IL} maximum. Also, this setup is

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} =MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} =MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	D_n	V_{CC} = MAX, V_I = 0.5V					-100	µA
		CP_n,$\overline{S}_{Dn}$, $\overline{R}_{Dn}$						-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				10	16	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs High in turn.

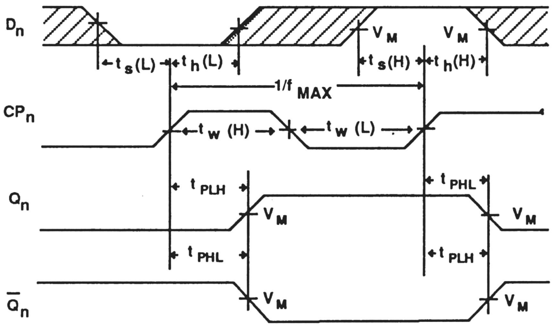
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1		200		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveform 1	2.0 2.0	2.9 3.3	4.5 5.0	2.0 2.0	5.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$, $\overline{R}_{Dn}$ to Q_n or $\overline{Q}_n$	Waveform 2	2.0 2.0	2.8 3.3	4.5 5.0	2.0 2.0	5.5 6.0	ns

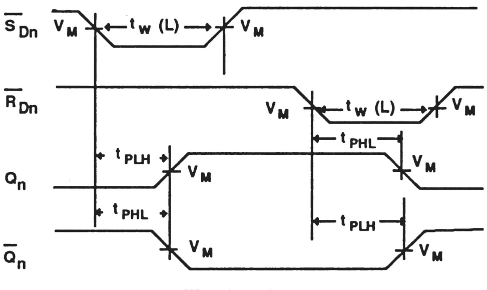
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_n to CP_n	Waveform 1	1.0 1.0			1.0 1.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_n to CP_n	Waveform 1	1.0 1.0			1.0 1.0		ns
t_w(H) t_w(L)	CP Pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
t_w(L)	$\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ Pulse width, Low	Waveform 2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to CP_n	Waveform 3	2.0			2.0		ns

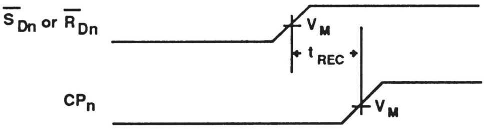
AC WAVEFORMS


Dn
t_s(L)
t_h(L)
V_M
V_M
t_s(H)
t_h(H)
1/f MAX
CPn
t_w (H)
t_w (L)
t_{PLH}
t_{PHL}
Qn
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Q}$n
V_M
V_M

Waveform 1. Propagation Delay For data to output, data setup time and hold times, and clock width


$\overline{S}_{Dn}$
V_M
t_w (L)
V_M
$\overline{R}_{Dn}$
V_M
t_w (L)
V_M
t_{PHL}
t_{PLH}
Qn
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Q}$n
V_M
V_M

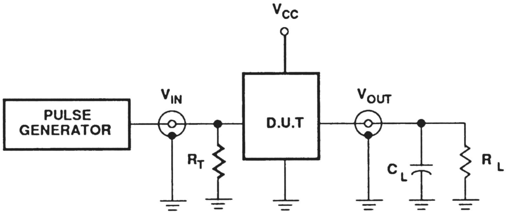
Waveform 2.
Propagation Delay for set and reset to output, set and reset pulse width


$\overline{S}_{Dn}$ or $\overline{R}_{Dn}$
V_M
t_{REC}
CPn
V_M

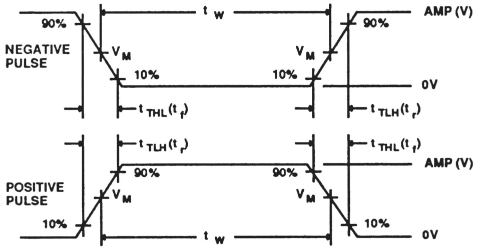
Waveform 3.
Recovery time for set or reset to clock

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_CC
PULSE GENERATOR
V_IN
R_T
D.U.T
V_OUT
C_L
R_L

Test Circuit For Totem-Pole Outputs


90%
t_w
AMP (V)
90%
NEGATIVE PULSE
V_M
V_M
10%
10%
0V
t_{THL}(t_f)
t_{TLH}(t_r)
t_{TLH}(t_r)
t_{THL}(t_f)
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
0V
t_w

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	**Rep. Rate**	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAST 74F109A
FLIP-FLOP

Synchronizing Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flops

Preliminary Specification

FEATURES

- **Metastable Immune Characteristics**
- **Same pinout and function as 74F109**
- **See 74F74A for Synchronizing Dual D-Type Flip-Flop**
- **See 74F728 for Synchronizing Cascaded D-Type Flip-Flop**
- **See 74F729 for Synchronizing Cascaded Dual D-Type Flip-Flop with Edge-Triggered Set and Reset**

DESCRIPTION

The 74F109A is a dual positive edge-triggered JK-type flip-flop featuring individual J, $\overline{K}$, Clock, Set and Reset inputs; also true and complementary outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-Low inputs and operate independently of the Clock (CP) inputs.

The J and $\overline{K}$ are edge-triggered inputs which control the state changes of the flip-flops as described in the Function Table. The J and $\overline{K}$ inputs must be stable just one setup time prior to the Low-to-High transition of the clock for guaranteed propagation delays. The J$\overline{K}$ design allows operation as a D flip-flop by tying J and $\overline{K}$ inputs together.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F109A	200 MHz	10mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F109AN
16-Pin Plastic SO	N74F109AD

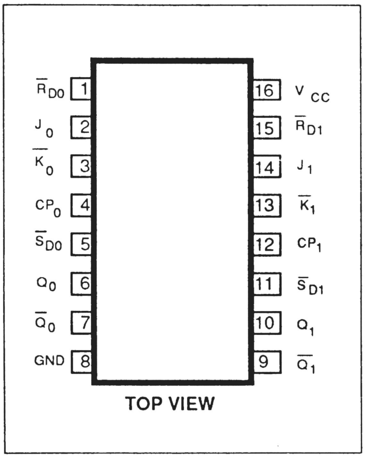
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_0, J_1	J inputs	1.0/0.166	20µA/100µA
$\overline{K}_0, \overline{K}_1$	K inputs	1.0/0.166	20µA/100µA
CP_0, CP_1	Clock inputs (active rising edge)	1.0/0.083	20µA/50µA
$\overline{S}_{D0}, \overline{S}_{DI}$	Set inputs (active Low)	1.0/0.083	20µA/50µA
$\overline{R}_{D0}, \overline{R}_{DI}$	Reset inputs (active Low)	1.0/0.083	20µA/50µA
$Q_0, Q_I, \overline{Q}_0, \overline{Q}_I$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

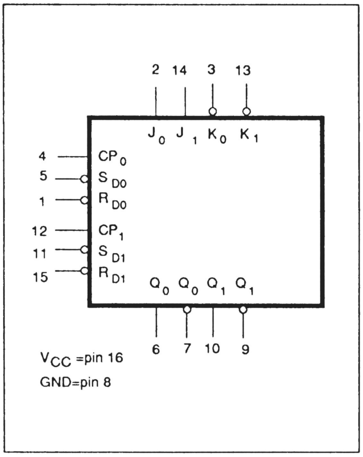
The 74F109A is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup and hold times are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F109A are: τ < .100ns, T_o=1µs, and h=3.3ns.

PIN CONFIGURATION



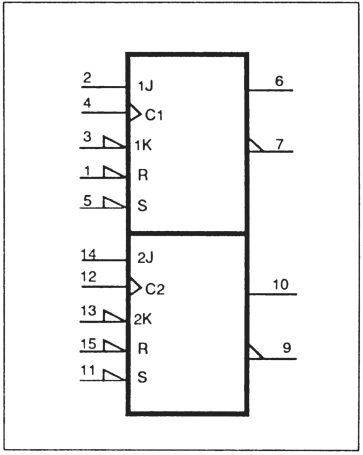
$\overline{R}_{D0}$ 1
J_0 2
$\overline{K}_0$ 3
CP_0 4
$\overline{S}_{D0}$ 5
Q_0 6
$\overline{Q}_0$ 7
GND 8
16 V_{CC}
15 $\overline{R}_{D1}$
14 J_1
13 $\overline{K}_1$
12 CP_1
11 $\overline{S}_{D1}$
10 Q_1
9 $\overline{Q}_1$
TOP VIEW

LOGIC SYMBOL



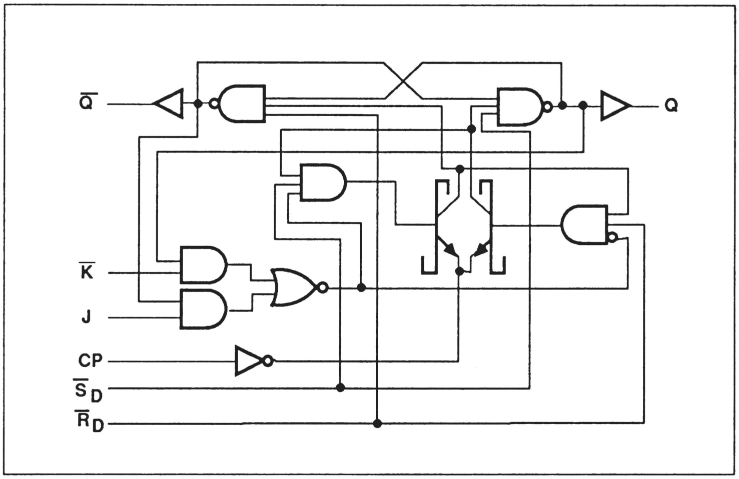
2 14 3 13
J_0 J_1 K_0 K_1
4 CP_0
5 S_{D0}
1 R_{D0}
12 CP_1
11 S_{D1}
15 R_{D1}
Q_0 Q_0 Q_1 Q_1
6 7 10 9
V_{CC} =pin 16
GND=pin 8

LOGIC SYMBOL(IEEE/IEC)



2 1J
4 C1
3 1K
1 R
5 S
6
7
14 2J
12 C2
13 2K
15 R
11 S
10
9

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
$\overline{S}_D$	$\overline{R}_D$	CP	J	$\overline{K}$	$\overline{Q}$	$\overline{Q}$	
L	H	X	X	X	H	L	Asynchronous Set
H	L	X	X	X	L	H	Asynchronous Reset
L	L	X	X	X	H	H	Undetermined (Note)
H	H	↑	h	l	$\overline{q}$	q	Toggle
H	H	↑	l	l	L	H	Load "0"(Reset)
H	H	↑	h	h	H	L	Load "1" (Set)
H	H	↑	l	h	q	$\overline{q}$	Hold "no change"

H = High voltage level
h-= High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
q=Lower case indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
Note =Both outputs will be High if both $\overline{S}_D$ and $\overline{R}_D$ go Low simultaneously.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} =MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} =MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	J, $\overline{K}$, CP_n	V_{CC} = MAX, V_I = 7.0V					0.1	mA
		$\overline{S}_{Dn}$, $\overline{R}_{Dn}$						0.2	mA
I_{IH}	High-level input current	J, $\overline{K}$, CP_n	V_{CC} = MAX, V_I = 2.7V					20	µA
		$\overline{S}_{Dn}$, $\overline{R}_{Dn}$						20	µA
I_{IL}	Low-level input current	J, $\overline{K}$	V_{CC} = MAX, V_I = 0.5V					-100	µA
		CP_n, $\overline{S}_{Dn}$, $\overline{R}_{Dn}$						-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX				10	16	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs High in turn.

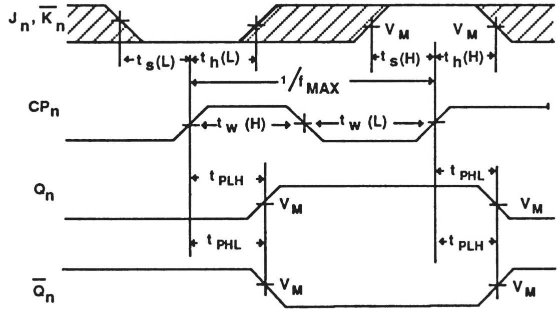
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1		200		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveform 1	2.0 2.0	2.9 3.3	4.5 5.0	2.0 2.0	5.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$, $\overline{R}_{Dn}$ to Q_n or $\overline{Q}_n$	Waveform 2	2.0 2.0	2.8 3.3	4.5 5.0	2.0 2.0	5.5 6.0	ns

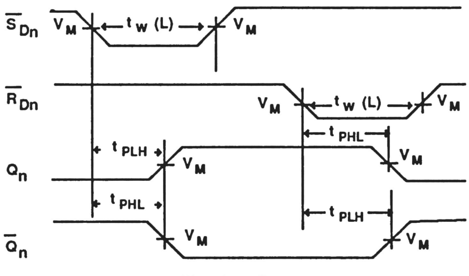
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J_n, $\overline{K}_n$ to CP	Waveform 1	1.0 1.0			1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J_n, $\overline{K}_n$ to CP	Waveform 1	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	$\overline{S}_D$ or $\overline{R}_D$ Pulse width, Low	Waveform 2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{S}_D$ or $\overline{R}_D$ to CP	Waveform 3	2.0			2.0		ns

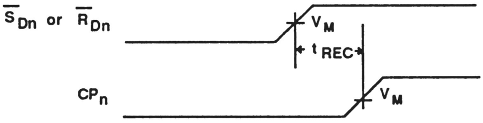
AC WAVEFORMS


Jn, K̄n
VM
VM
ts(L)
th(L)
ts(H)
th(H)
1/fMAX
CPn
tw (H)
tw (L)
Qn
tPLH
tPHL
VM
VM
tPHL
tPLH
Q̄n
VM
VM

Waveform 1. Propagation Delay For data to output, data setup time and hold times, clock width, and maximum clock frequency


S̄Dn
VM
tw (L)
VM
R̄Dn
VM
tw (L)
VM
tPHL
Qn
tPLH
VM
VM
tPHL
tPLH
Q̄n
VM
VM

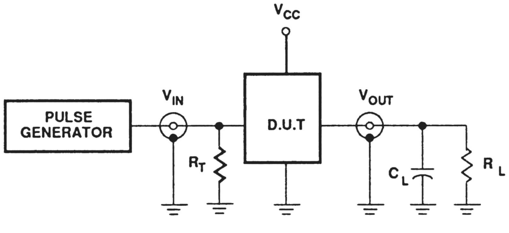
Waveform 2.
Propagation Delay for set and reset to output, set and reset pulse width


S̄Dn or R̄Dn
VM
tREC
CPn
VM

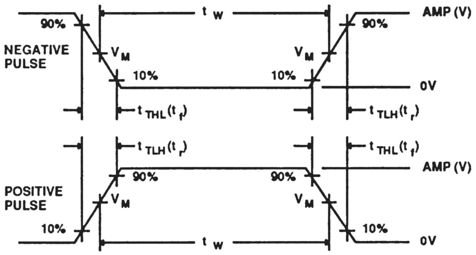
Waveform 3.
Recovery time for set or reset to clock

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
VIN
VOUT
PULSE GENERATOR
D.U.T
RT
CL
RL

Test Circuit For Totem-Pole Outputs


NEGATIVE PULSE
90%
VM
10%
tw
VM
10%
90%
AMP (V)
0V
tTHL(tf)
tTLH(tr)
POSITIVE PULSE
tTLH(tr)
tTHL(tf)
90%
90%
AMP (V)
VM
VM
10%
10%
tw
0V

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F154
Decoder/Demultiplexer

1-of-16 Decoder/Demultiplexer
Product Specification

FEATURES

- **16-line demultiplexing capability**
- **Mutually exclusive outputs**
- **2-input enable gate for strobing or expansion**

DESCRIPTION

The 74F154 decoder accepts four active High binary address inputs and provides 16 mutually exclusive active Low outputs. The 2-input Enable ($\overline{E}_0$, $\overline{E}_1$) gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for expansion othe decoder. The Enable gate has two AND'ed inputs which must be Low to enable the outputs.

The 74F154 can be used as a 1-of-16 demultiplexer by using one of the Enable inputs as the multiplexed data input. When the other Enable is Low, the addressed output will follow the state of the applied data.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N74F154	5.5 ns	26mA

ORDERING INFORMATION

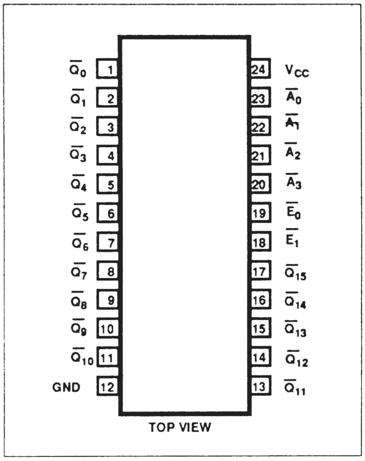
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F154N
24-Pin Plastic SOL	N74F154D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

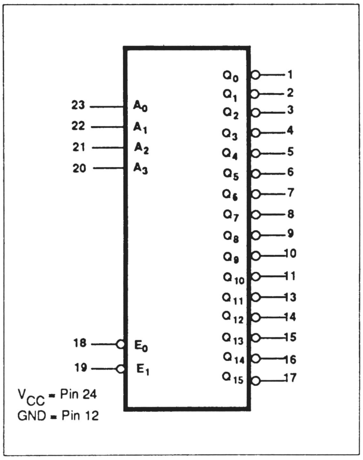
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{E}_0$, $\overline{E}_1$	Enable inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}_0$ - $\overline{Q}_{15}$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

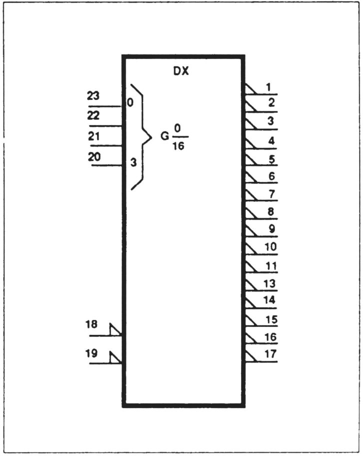
PIN CONFIGURATION


$\overline{Q}_0$ 1
$\overline{Q}_1$ 2
$\overline{Q}_2$ 3
$\overline{Q}_3$ 4
$\overline{Q}_4$ 5
$\overline{Q}_5$ 6
$\overline{Q}_6$ 7
$\overline{Q}_7$ 8
$\overline{Q}_8$ 9
$\overline{Q}_9$ 10
$\overline{Q}_{10}$ 11
GND 12
24 V_{CC}
23 A_0
22 A_1
21 A_2
20 A_3
19 $\overline{E}_0$
18 $\overline{E}_1$
17 $\overline{Q}_{15}$
16 $\overline{Q}_{14}$
15 $\overline{Q}_{13}$
14 $\overline{Q}_{12}$
13 $\overline{Q}_{11}$
TOP VIEW

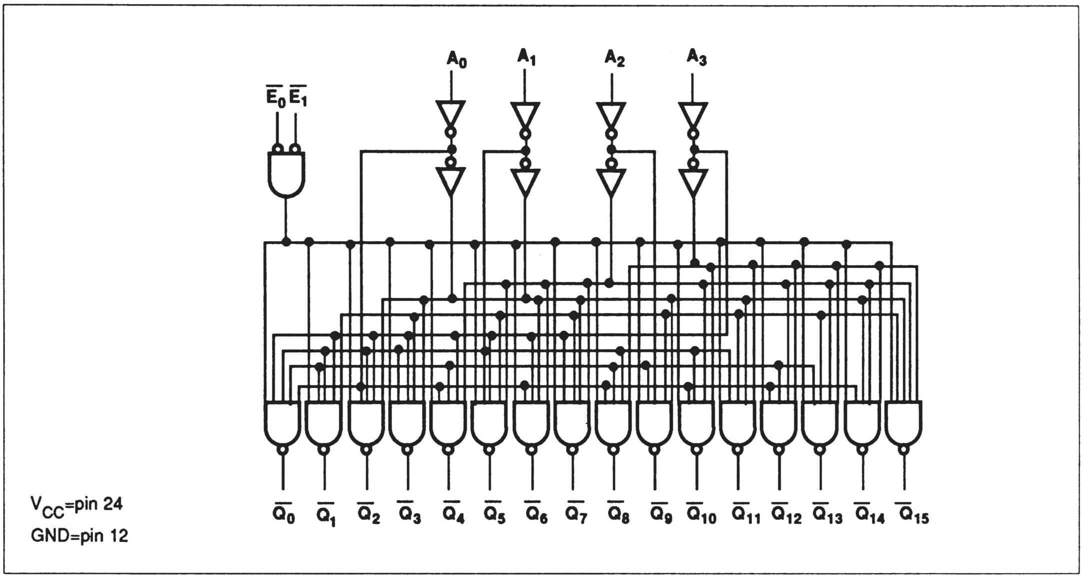
LOGIC SYMBOL


23 A_0
22 A_1
21 A_2
20 A_3
18 E_0
19 E_1
Q_0 1
Q_1 2
Q_2 3
Q_3 4
Q_4 5
Q_5 6
Q_6 7
Q_7 8
Q_8 9
Q_9 10
Q_{10} 11
Q_{11} 13
Q_{12} 14
Q_{13} 15
Q_{14} 16
Q_{15} 17
V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)


DX
23
22
21
20
0
3
G $\frac{0}{16}$
18
19
1
2
3
4
5
6
7
8
9
10
11
13
14
15
16
17

LOGIC DIAGRAM


A_0
A_1
A_2
A_3
$\overline{E}_0$ $\overline{E}_1$
$\overline{Q}_0$
$\overline{Q}_1$
$\overline{Q}_2$
$\overline{Q}_3$
$\overline{Q}_4$
$\overline{Q}_5$
$\overline{Q}_6$
$\overline{Q}_7$
$\overline{Q}_8$
$\overline{Q}_9$
$\overline{Q}_{10}$
$\overline{Q}_{11}$
$\overline{Q}_{12}$
$\overline{Q}_{13}$
$\overline{Q}_{14}$
$\overline{Q}_{15}$

V_{CC}=pin 24
GND=pin 12

FUNCTION TABLE

INPUTS						OUTPUTS															
$\overline{E}_0$	$\overline{E}_1$	A_0	A_1	A_2	A_3	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$	$\overline{Q}_8$	$\overline{Q}_9$	$\overline{Q}_{10}$	$\overline{Q}_{11}$	$\overline{Q}_{12}$	$\overline{Q}_{13}$	$\overline{Q}_{14}$	$\overline{Q}_{15}$
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			26	40	mA

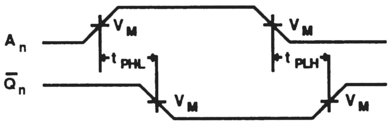
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

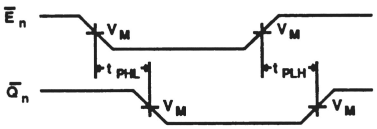
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Q}_n$	Waveform 1	2.0 3.5	5.0 6.5	9.5 10.0	1.5 3.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay E_n to $\overline{Q}_n$	Waveform 2	2.0 4.0	4.0 6.0	7.5 9.0	1.5 3.5	8.0 9.5	ns

AC WAVEFORMS


A n
Q̄ n
V M
t PHL
V M
t PLH
V M
V M

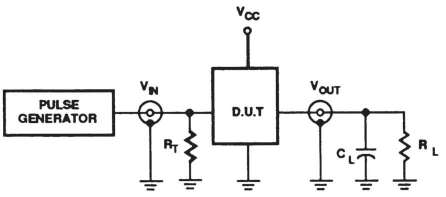
Waveform 1. Propagation Delay For Address To Output


Ē n
Q̄ n
V M
t PHL
V M
t PLH
V M
V M

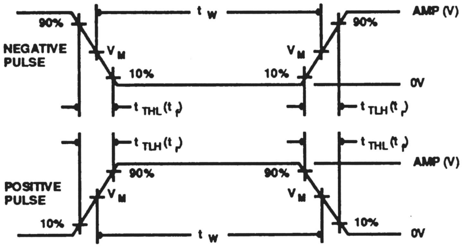
Waveform 2. Propagation Delay For Enable To Output

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


V CC
PULSE GENERATOR
V IN
R T
D.U.T
V OUT
C L
R L

Test Circuit For Totem-Pole Outputs


NEGATIVE PULSE
90%
V M
10%
t W
V M
10%
90%
AMP (V)
0V
t THL (t f)
t TLH (t r)
t TLH (t r)
t THL (t f)
POSITIVE PULSE
90%
V M
10%
90%
V M
10%
AMP (V)
0V
t W

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAST 74F164

Shift Register

8-Bit Serial-In Parallel-Out Shift Register
Product Specification

FEATURES

- **Gated serial data inputs**
- **Typical shift frequency of 100MHz**
- **Asynchronous Master Reset**
- **Fully buffered clock and data inputs**
- **Fully synchronous data transfers**

DESCRIPTION

The 74F164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered through one of two inputs (D_{sa}, D_{sb}); either input can be used as an active High enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied High.

Data shifts one place to the right on each Low-to-High transition of the Clock (CP) input, and enters into Q_0 the logical AND of the the two data inputs (D_{sa}, D_{sb}) that existed one setup time before the rising clock edge. A Low level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs Low.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F164	100MHz	33mA

ORDERING INFORMATION

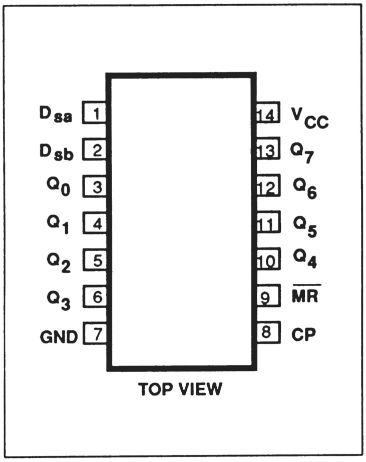
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F164N
14-Pin Plastic SOL	N74F164D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

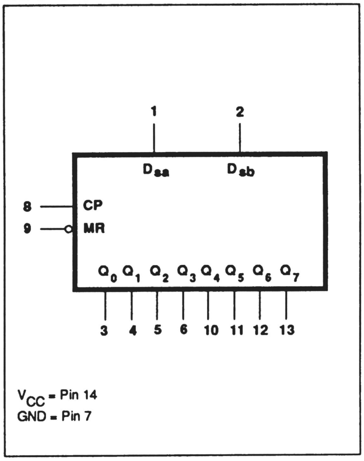
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{sa} , D_{sb}	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
Q_0 - Q_7	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

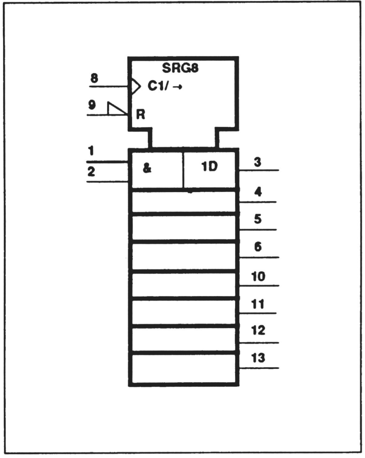
PIN CONFIGURATION



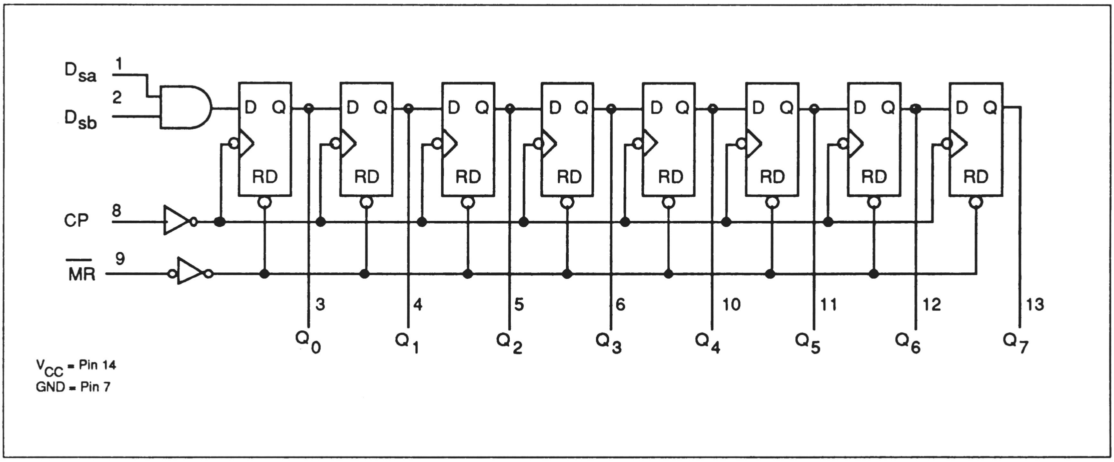
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	Q_1 - - - - Q_7	
L	X	X	X	L	L L	Reset (clear)
H	↑	l	l	L	q_0 q_6	Shift
H	↑	l	h	L	q_0 q_6	
H	↑	h	l	L	q_0 q_6	
H	↑	h	h	H	q_0 q_6	

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
q_n = Lower case letters indicate the state of the referenced input (or output) on setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

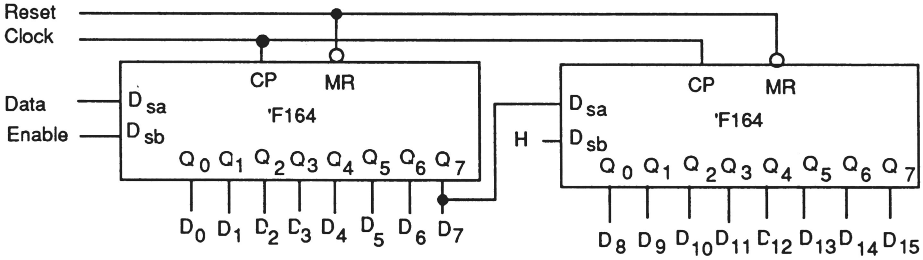
(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]	V_{CC} = MAX			33	55	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. Measure I_{CC} with the serial inputs grounded , the clock input at 2.4 V, and a momentary ground, then 4.5V applied to Master Reset, and all outputs open.

APPLICATION


Reset
Clock
Data
Enable
CP
MR
'F164
D_{sa}
D_{sb}
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
H
CP
MR
'F164
D_{sa}
D_{sb}
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
D_8 D_9 D_{10} D_{11} D_{12} D_{13} D_{14} D_{15}

NOTE: The 'F164 can be cascaded to form synchronous shift registers of longer length. Here, two 'F164 are combined to form a 16 bit shift register.

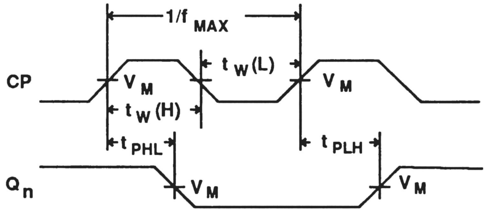
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.0 5.0	5.0 7.0	8.0 10.0	2.5 5.0	9.0 11.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	4.0	7.5	10.5	4.0	11.5	ns

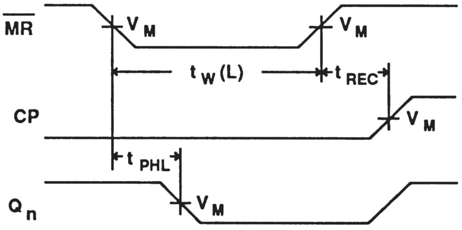
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 3	7.0 7.0			5.0 5.0		ns
$t_s(H)$ $t_s(L)$	Hold time, High or Low D_n to CP	Waveform 3	1.0 1.0			2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width High or Low	Waveform 1	4.0 7.0			4.0 7.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width Low	Waveform 2	7.0			7.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	7.0			7.0		ns

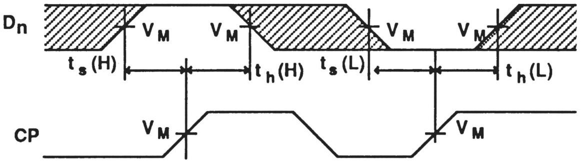
AC WAVEFORMS


1/f MAX
CP
V M
t W(L)
V M
t W(H)
t PHL
t PLH
Q n
V M
V M

Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency


MR
V M
V M
t W(L)
t REC
CP
V M
t PHL
Q n
V M

Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

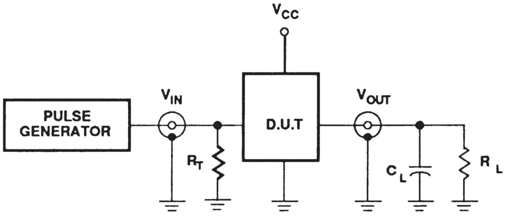

D n
V M
V M
V M
V M
t s(H)
t h(H)
t s(L)
t h(L)
CP
V M
V M

Waveform 3. Data Setup And Hold Times

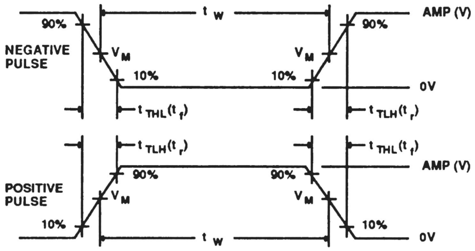
NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V CC
PULSE GENERATOR
V IN
R T
D.U.T
V OUT
C L
R L

Test Circuit For Totem-Pole Outputs


t w
AMP (V)
90%
90%
NEGATIVE PULSE
V M
V M
10%
10%
0V
t THL(t f)
t TLH(t r)
t TLH(t r)
t THL(t f)
AMP (V)
90%
90%
POSITIVE PULSE
V M
V M
10%
10%
0V
t w

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F189A

64-Bit TTL Bipolar RAM

Product Specification

DESCRIPTION

The 74F189A is a high-speed, 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-State and are in the High-impedance state whenever the Chip Select ($\overline{CE}$) input is High. The outputs are active only in the Read mode and the output data is the complement of the stored data.

Ordering information can be found on the following page.

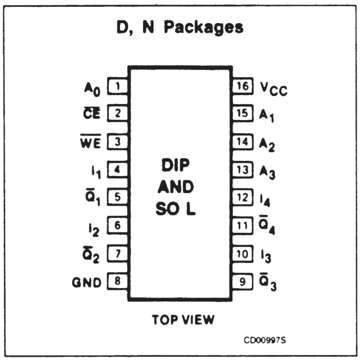
FEATURES

- **Address access time: 10ns max**
- **Power dissipation: 4.3mW/bit typ**
- **Schottky clamped TTL**
- **One chip enable input**
- **I/O**
  - **Inputs: PNP Buffered**
  - **Outputs: 3-State**

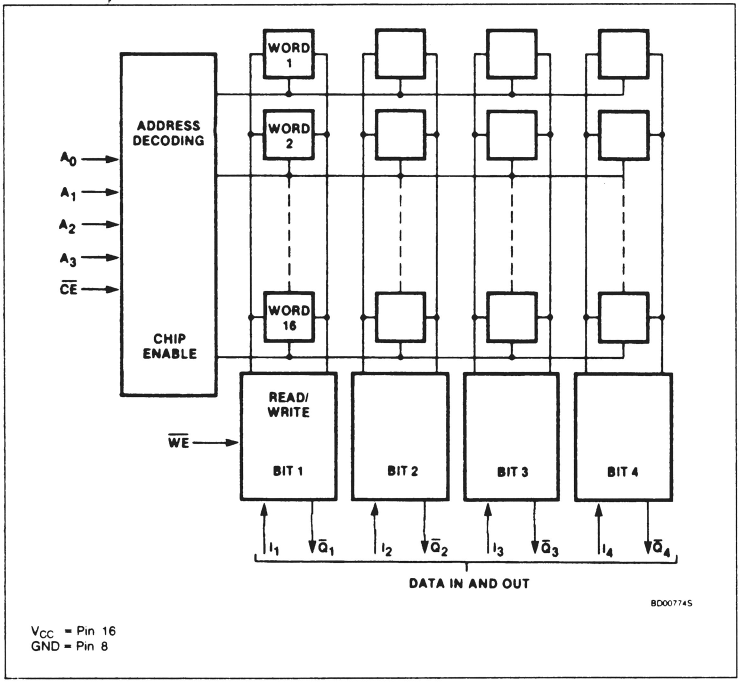
APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Push down stacks**
- **Control store**

PIN CONFIGURATION


D, N Packages
A_0 1
$\overline{CE}$ 2
$\overline{WE}$ 3
I_1 4
$\overline{Q}_1$ 5
I_2 6
$\overline{Q}_2$ 7
GND 8
16 V_{CC}
15 A_1
14 A_2
13 A_3
12 I_4
11 $\overline{Q}_4$
10 I_3
9 $\overline{Q}_3$
DIP AND SO L
TOP VIEW
CD00997S

BLOCK DIAGRAM


ADDRESS DECODING
CHIP ENABLE
A_0
A_1
A_2
A_3
$\overline{CE}$
WORD 1
WORD 2
WORD 16
READ/WRITE
$\overline{WE}$
BIT 1
BIT 2
BIT 3
BIT 4
I_1
$\overline{Q}_1$
I_2
$\overline{Q}_2$
I_3
$\overline{Q}_3$
I_4
$\overline{Q}_4$
DATA IN AND OUT
BD00774S
V_{CC} = Pin 16
GND = Pin 8

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Plastic Dual-In-Line 300mil-wide	N74F189N
16-Pin Plastic Small Outline 300mil-wide	N74F189D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V_{DC}
V_{IN}	Input voltage	−0.5 to +7.0	V_{DC}
V_{OH}	Output voltage High	−0.5 to +5.5	V_{DC}
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +70°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input voltage[2]						
V_{IC}[7]	Clamp	$V_{CC} = 5.25V$, $I_I = -18mA$			−1.2	V
Output voltage						
V_{OH}	High	$V_{CC} = 4.75V$, $V_{IH} = 2.0V$, $V_{IL} = 0.8V$ $I_{OH} = -3.0mA$	2.4			V
V_{OL}[2,3]	Low	$I_{OL} = 20mA$		0.35	0.5	
Input current						
I_{IH}	High	$V_{CC} = 5.25V$ $V_{IN} = 5.5V$			40	µA
I_{IL}	Low	$V_{IN} = 0.5V$			0.6	
Output current						
I_{OZ}	Off-state	$V_{CC} = 5.25V$ $V_{IH} = 2.0V$, $2.4V \geqslant V_{OUT} \geqslant 0.5V$			±50	µA
I_{OS}[11]	Short circuit	(See Note)	−60		−150	mA
Supply current[6]						
I_{CC}		$V_{CC} = 5.25V$, $\overline{WE}$, $\overline{CE}$ = GND			70	mA
Capacitance						
C_{IN}	Input	$V_{CC} = 5.0V$ $V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	I_n	$\overline{Q}_n$
Read	0	1	X	Compliment of stored data
Write "0"	0	0	0	Hi-Z
Write "1"	0	0	1	Hi-Z
Disable	1	X	X	Hi-Z

X = Don't care

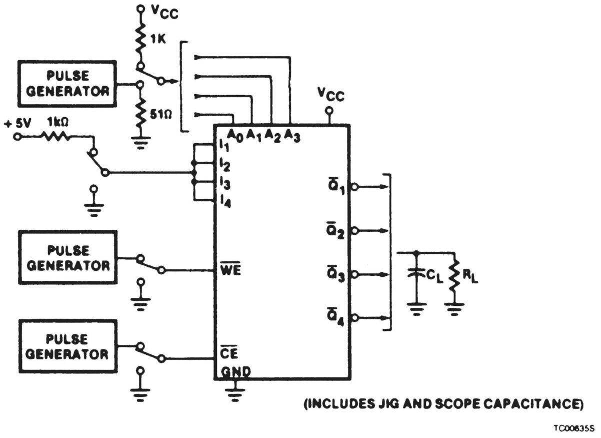
AC ELECTRICAL CHARACTERISTICS $R_L = 500\Omega$, $C_L = 50pF$, $0°C \leqslant T_A \leqslant +70°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
Access time							
t_{AA}	Address	Output	Address			10	ns
t_{CE}	Chip enable	Output	Chip enable			7.5	ns
Disable time[8]							
t_{CD}		Output	Chip enable			7.5	ns
Response time[8]							
t_{WD}		Output	Write enable			8.5	ns
Write recovery time							
t_{WR}		Output	Write enable			7.5	ns
Setup and hold time							
t_{WSA}[9] t_{WHA}	Setup time Hold time	Write enable	Address	0 0.5			ns
t_{WSD} t_{WHD}	Setup time Hold time	Write enable	Data in	5 0			
t_{WSC} t_{WHC}	Setup time Hold time	Write enable	$\overline{CE}$	4.5 4			
Pulse width							
t_{WP}[10]	Write enable			6.5			ns

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Output sink current is supplied through a resistor to V_{CC}.
3. All sense outputs in Low state.
4. To guarantee a Write into the slowest bit.
5. Positive current is defined as into the terminal referenced.
6. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 0.45V, and the output open.
7. Test each input one at a time.
8. Measured at a delta of 0.3V from the logic level with $R_1 = 500\Omega$, $R_2 = 500\Omega$ and $C_L = 50pF$.
9. Measured with minimum t_{WP}.
10. Measured with minimum t_{WSA}.
11. For I_{OS} test: V_{CC} = 5.75 V V_{OUT} = 0.5 V

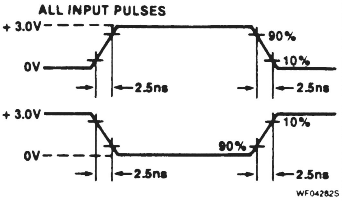
TEST LOAD CIRCUIT


VCC
1K
51Ω
PULSE GENERATOR
+5V
1kΩ
VCC
A0 A1 A2 A3
I1
I2
I3
I4
Q̄1
Q̄2
Q̄3
Q̄4
PULSE GENERATOR
WE
CL
RL
PULSE GENERATOR
CE
GND
TC00635S

(INCLUDES JIG AND SCOPE CAPACITANCE)

Loading Conditions

VOLTAGE WAVEFORM

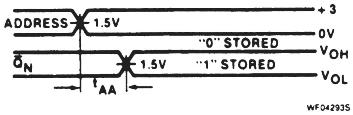

ALL INPUT PULSES
+3.0V
0V
90%
10%
2.5ns
2.5ns
+3.0V
0V
10%
90%
2.5ns
2.5ns
WF04282S

MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and output.

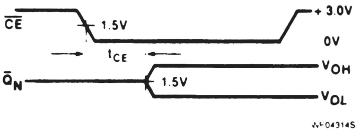
Input Pulses

TIMING DIAGRAMS

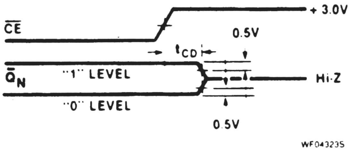
Read Cycle


ADDRESS
1.5V
+3
0V
"0" STORED
$\overline{Q}_N$
1.5V
"1" STORED
V_{OH}
V_{OL}
t_{AA}
WF04293S

Address Access Time

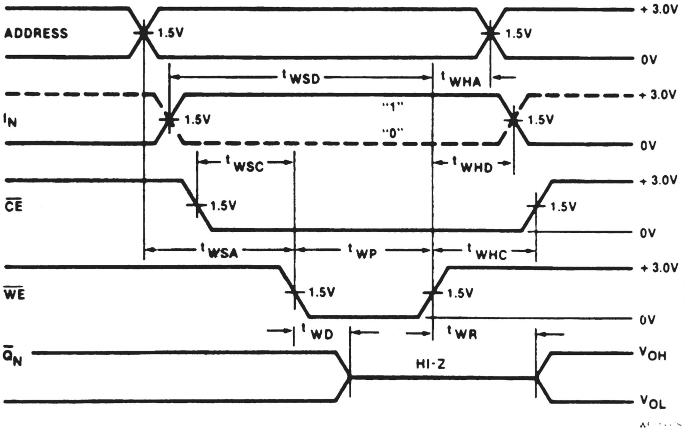

$\overline{CE}$
1.5V
+3.0V
0V
t_{CE}
$\overline{Q}_N$
1.5V
V_{OH}
V_{OL}
WF04314S

Chip Enable


$\overline{CE}$
+3.0V
0.5V
t_{CD}
$\overline{Q}_N$
"1" LEVEL
Hi-Z
"0" LEVEL
0.5V
WF04323S

Chip Disable

Write Cycle


ADDRESS
1.5V
1.5V
+3.0V
0V
t_{WSD}
t_{WHA}
I_N
1.5V
"1"
"0"
1.5V
+3.0V
0V
t_{WSC}
t_{WHD}
$\overline{CE}$
1.5V
1.5V
+3.0V
0V
t_{WSA}
t_{WP}
t_{WHC}
$\overline{WE}$
1.5V
1.5V
+3.0V
0V
t_{WD}
t_{WR}
$\overline{Q}_N$
HI-Z
V_{OH}
V_{OL}

All AC parameters are measured at 1.5V unless otherwise specified.

FAST 74F198

Shift Register

8-Bit Bidirectional Universal Shift Register
Product Specification

FEATURES

- **Buffered clock and control inputs**
- **Shift right, shift left, and parallel load capability**
- **Asynchronous Master Reset**

DESCRIPTION

The 74F198, Bidirectional Universal Shift Register is designed to incorporate virtually all of the features a system designer may want in a shift register. This circuit features parallel inputs and outputs, shift right and shift left serial inputs, operating mode select inputs, and a direct overriding master reset input. The register has four distinct modes of operation:

Parallel (broadside) load
Shift right (in the direction Q_0 toward Q_7)
Shift left (in the direction Q_7 toward Q_0)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the 8 bits of data and taking both mode control inputs, S_0 and S_1, High. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F198	95MHz	73mA

ORDERING INFORMATION

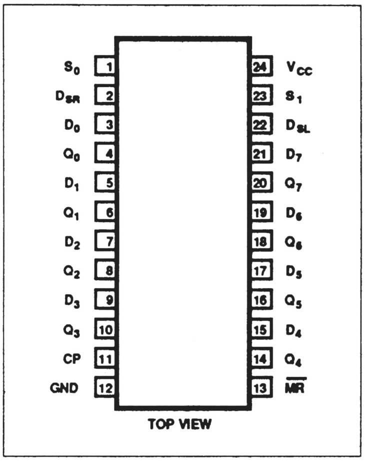
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F198N
24-Pin Plastic SOL	N74F198D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Parallel data inputs	1.0/1.0	20µA/0.6mA
D_{SR}	Serial data input (Shift Right)	1.0/1.0	20µA/0.6mA
D_{SL}	Serial data input (Shift Left)	1.0/1.0	20µA/0.6mA
S_0 - S_1	Mode Select inputs	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (Active rising edge)	1.0/1.0	20 A/0.6mA
$\overline{MR}$	Master Reset input (Active Low)	1.0/1.0	20µA/0.6mA
Q_0 - Q_7	Data outputs	50/33	1.0mA/20mA

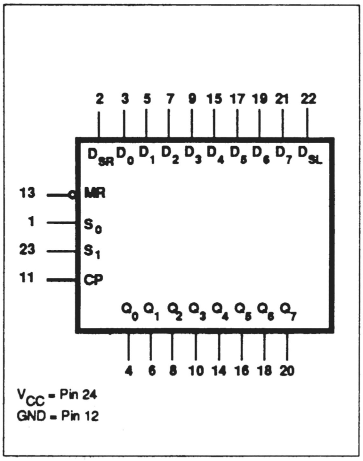
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



S0 1
DSR 2
D0 3
Q0 4
D1 5
Q1 6
D2 7
Q2 8
D3 9
Q3 10
CP 11
GND 12
24 VCC
23 S1
22 DSL
21 D7
20 Q7
19 D6
18 Q6
17 D5
16 Q5
15 D4
14 Q4
13 MR
TOP VIEW

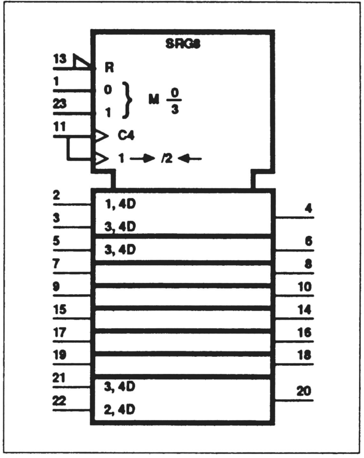
LOGIC SYMBOL



2 3 5 7 9 15 17 19 21 22
DSR D0 D1 D2 D3 D4 D5 D6 D7 DSL
13 MR
1 S0
23 S1
11 CP
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
4 6 8 10 14 16 18 20

V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

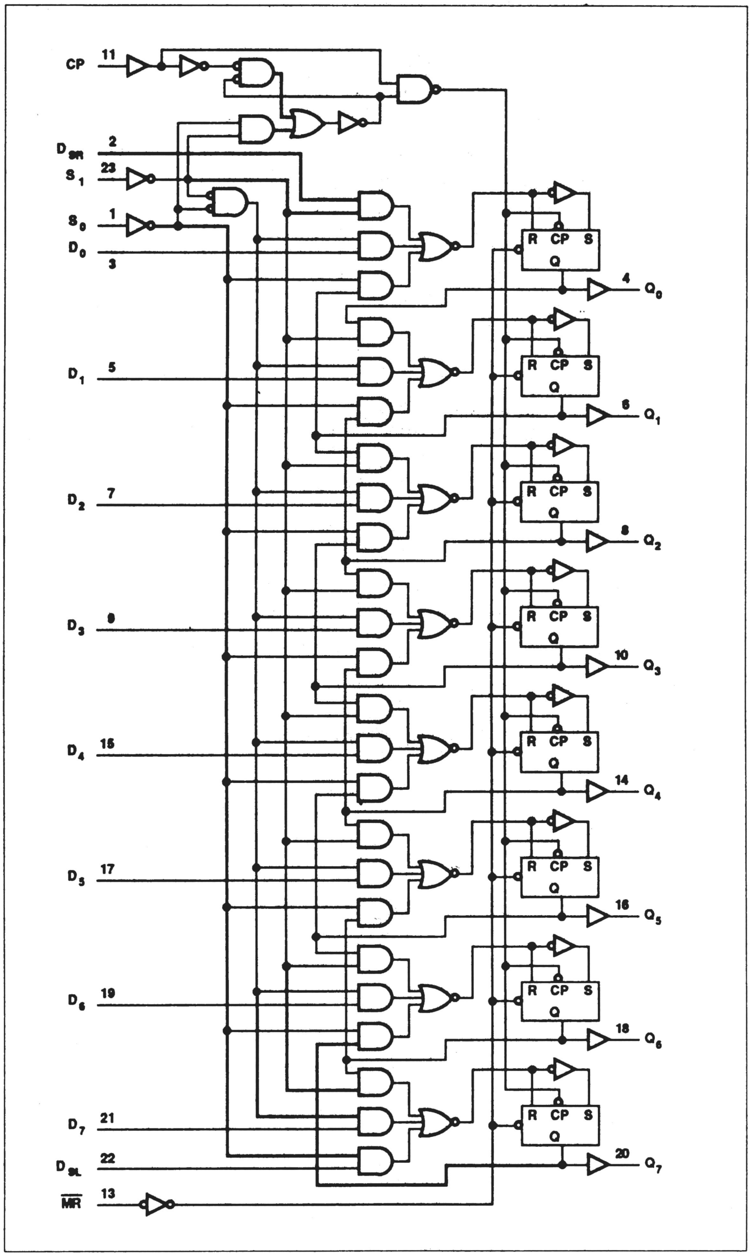


SRG8
13 R
1 0
23 1
M 0/3
11 C4
1 → /2 ←
2 1, 4D
3 3, 4D
5 3, 4D
7
9
15
17
19
21 3, 4D
22 2, 4D
4
6
8
10
14
16
18
20

Shift right is accomplished synchronously, with the rising edge of the clock pulse when S_0 is High and S_1 is Low. Serial data for this mode is entered at the right data input (D_{SR}). When S_0 is Low and S_1 is High, data shifts left synchronously and new data is entered at the shift-left serial input (D_{SL}).

Clocking of the flip-flops is inhibited when both mode control inputs are Low.

LOGIC DIAGRAM


CP
11
D_{SR}
2
S_1
23
S_0
1
D_0
3
D_1
5
D_2
7
D_3
9
D_4
15
D_5
17
D_6
19
D_7
21
D_{SL}
22
$\overline{MR}$
13
R CP S
Q
4 Q_0
6 Q_1
8 Q_2
10 Q_3
14 Q_4
16 Q_5
18 Q_6
20 Q_7

FUNCTION TABLE

INPUTS							OUTPUTS				
$\overline{MR}$	Mode		CP	Serial		Parallel	Q_0	Q_1	...	Q_6	Q_7
	S_0	S_1		Left	Right	0...7					
L	X	X	X	X	X	X	L	L		L	L
H	X	X	L	X	X	X	Q_{00}	Q_{10}		Q_{60}	Q_{70}
H	H	H	↑	X	X	0...7	0	1		6	7
H	H	L	↑	X	H	X	H	Q_{0n}		Q_{5n}	Q_{6n}
H	H	L	↑	X	L	X	L	Q_{0n}		Q_{5n}	Q_{6n}
H	L	H	↑	H	X	X	Q_{1n}	Q_{2n}		Q_{7n}	H
H	L	H	↑	L	X	X	Q_{1n}	Q_{2n}		Q_{7n}	L
H	L	L	X	X	X	X	Q_{00}	Q_{10}		Q_{60}	Q_{70}

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High transition of designated input
0...7 = The level of steady input at inputs 0 through 7, respectively.
Q_{00}, Q_{10}, Q_{60}, Q_{70} = The level of Q_0, Q_1, Q_6, Q_7, respectively, before the indicated steady state input conditions were established.
Q_{0n}, Q_{1n}, Q_{6n}, Q_{7n} = The level of Q_0, Q_1, Q_6, Q_7, respectively, before the most recent Low-to-High clock transition.

ABSOLUTE MAXIMUM RATINGS

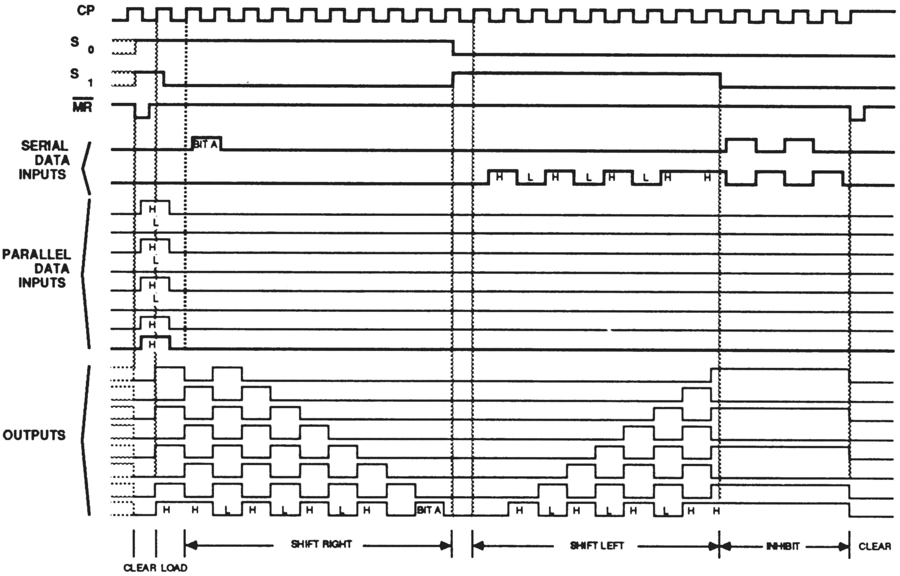
(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

TYPICAL TIMING DIAGRAM


CP
S_0
S_1
$\overline{MR}$
SERIAL DATA INPUTS
BIT A
H L H L H L H H
PARALLEL DATA INPUTS
H L H L H L H H
OUTPUTS
H H L H L H L H BIT A
H L H L H L H H
SHIFT RIGHT
SHIFT LEFT
INHIBIT
CLEAR
CLEAR LOAD

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input clamp current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			70	100	mA
		I_{CCL}				75	110	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

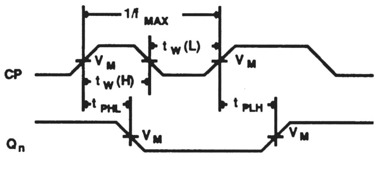
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	95		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	5.0 6.0	7.5 8.5	10.0 11.0	4.5 5.5	11.0 12.0	ns
t_{PHL}	Propagation delay	Waveform 3	5.0	7.5	10.0	4.5	11.0	ns

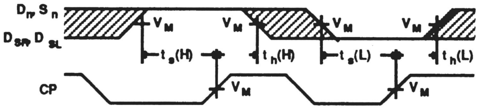
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_n to CP	Waveform 2	0.0 3.0			0.0 3.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_n to CP	Waveform 2	0.0 3.5			1.0 4.0		ns
t_s(H) t_s(L)	Setup time, High or Low D_{SR}, D_{SL} to CP	Waveform 2	0.0 3.0			0.0 3.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_{SR}, D_{SL} to CP	Waveform 2	0.0 2.5			0.0 3.0		ns
t_s(H) t_s(L)	Setup time, High or Low S_n to CP	Waveform 2	9.0 6.0			10.0 7.0		ns
t_h(H) t_h(L)	Hold time, High or Low S_n to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
t_w(H) t_w(L)	CP Pulse width, High or Low	Waveform 1	5.0 5.0			6.0 6.0		ns
t_w(L)	$\overline{MR}$ Pulse width, Low	Waveform 3	5.0			5.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 3	5.0			6.0		ns

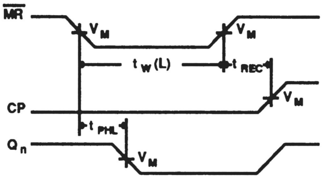
AC WAVEFORMS


1/f MAX
CP
V_M
$t_W(H)$
$t_W(L)$
t_{PHL}
t_{PLH}
Q_n

Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths, and Maximum Clock Frequency


D_n, S_n
D_{SR}, D_{SL}
V_M
$t_s(H)$
$t_h(H)$
$t_s(L)$
$t_h(L)$
CP

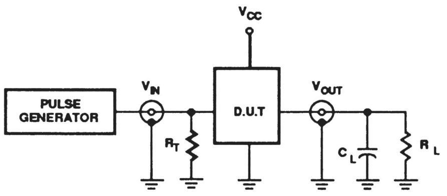
Waveform 2. Setup Time and Hold Time


$\overline{MR}$
V_M
$t_W(L)$
t_{REC}
CP
t_{PHL}
Q_n

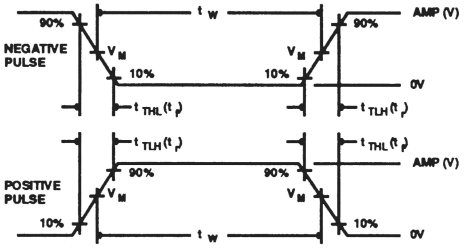
Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
R_T
D.U.T
V_{OUT}
C_L
R_L

Test Circuit For Totem-Pole Outputs


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
V_M
t_W
AMP (V)
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAST 74F199
Shift Register

8-Bit Parallel-Access Shift Register
Product Specification

FEATURES

- **Buffered clock and control inputs**
- **Shift right and parallel load capability**
- **Fully synchronous data transfers**
- **J - $\overline{K}$(D) inputs to first stage**
- **Clock enable for hold (do nothing) mode**
- **Asynchronous Master Reset**

DESCRIPTION

The 74F199 is an 8-bit Parallel Access Shift Register and its functional characteristics are indicated in the Logic diagram and Function Table. The device is useful in a variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The 74F199 operates in two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is High, and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2$ following each Low-to-High clock transition.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F199	95MHz	70mA

ORDERING INFORMATION

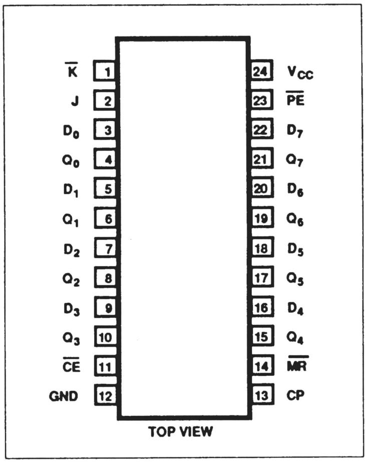
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F199N
24-Pin Plastic SOL	N74F199D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

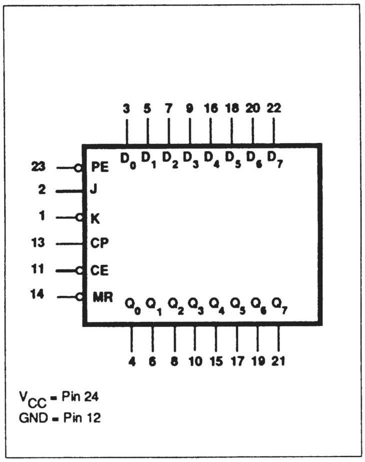
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Parallel data inputs	1.0/1.0	20μA/0.6mA
J, $\overline{K}$	J and K inputs	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel Enable input	1.0/1.0	20μA/0.6mA
$\overline{CE}$	Mode Select inputs	1.0/1.0	20μA/0.6mA
CP	Clock Pulse input (Active rising edge)	1.0/1.0	20 A/0.6mA
$\overline{MR}$	Master Reset input (Active Low)	1.0/1.0	20μA/0.6mA
Q_0 - Q_7	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

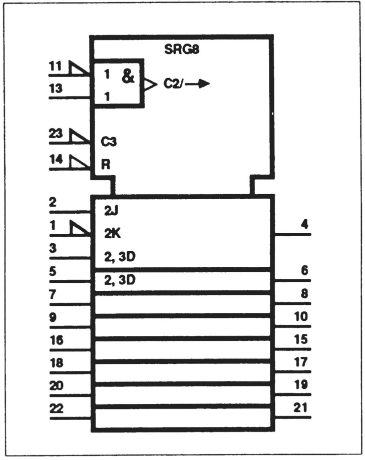

K̄ 1
J 2
D0 3
Q0 4
D1 5
Q1 6
D2 7
Q2 8
D3 9
Q3 10
CE̅ 11
GND 12
24 VCC
23 PE̅
22 D7
21 Q7
20 D6
19 Q6
18 D5
17 Q5
16 D4
15 Q4
14 MR̅
13 CP
TOP VIEW

LOGIC SYMBOL


3 5 7 9 16 18 20 22
D0 D1 D2 D3 D4 D5 D6 D7
23 PE
2 J
1 K
13 CP
11 CE
14 MR
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
4 6 8 10 15 17 19 21

VCC = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)


SRG8
11
13
1 &
1
C2/→
23
C3
14
R
2
2J
1
2K
4
3
2, 3D
5
2, 3D
6
7
8
9
10
16
15
18
17
20
19
22
21

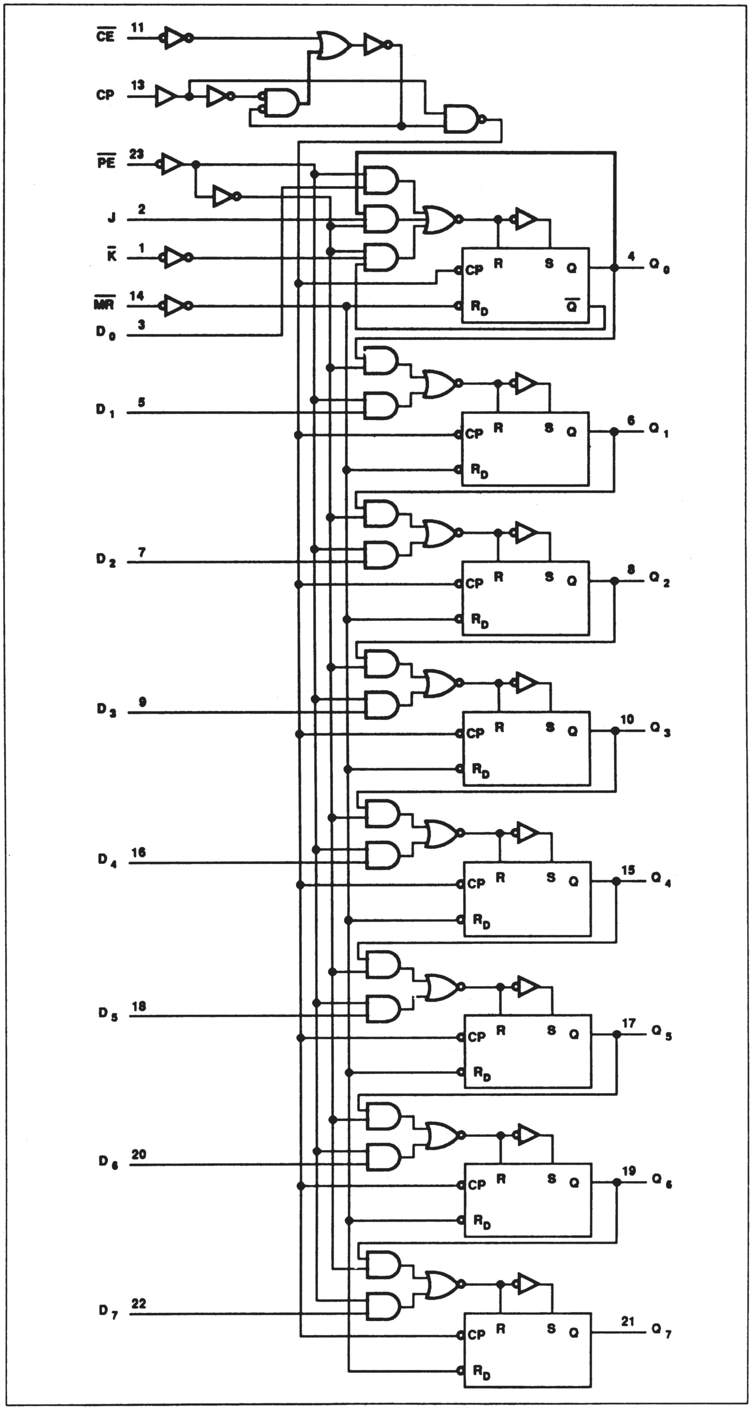
The J and $\overline{K}$ inputs provide the flexibility of the J-$\overline{K}$ type input for special applications, and by tying the two together the simple D-type input is made for general applications.

The device appears as eight common clocked D flip-flops when the $\overline{PE}$ input is Low. After the Low-to-High clock transition, data on the parallel inputs (D_0 - D_7) is transferred to the respective Q_0 - Q_7 outputs.

All parallel and serial data transfers are synchronous, occurring after each Low-to-High clock transition. The 74F199 utilizes edge-triggered, therefore there is no restriction on the activity of the J, $\overline{K}$, Dn, and $\overline{PE}$ inputs for logic operation, other than the set-up and hold time requirements.

A Low on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously forcing all bit positions to a Low state.

LOGIC DIAGRAM


$\overline{CE}$ 11
CP 13
$\overline{PE}$ 23
J 2
$\overline{K}$ 1
$\overline{MR}$ 14
D_0 3
D_1 5
D_2 7
D_3 9
D_4 16
D_5 18
D_6 20
D_7 22
CP
R
S
Q
R_D
$\overline{Q}$
4 Q_0
6 Q_1
8 Q_2
10 Q_3
15 Q_4
17 Q_5
19 Q_6
21 Q_7

FUNCTION TABLE

INPUTS							OUTPUTS					OPERATING MODES
$\overline{MR}$	CP	$\overline{CE}$	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0	Q_1	...	Q_6	Q_7	
L	X	X	X	X	X	X	L	L	...	L	L	Reset (clear)
H	↑	l	h	h	h	X	H	q_0	...	q_5	q_6	Shift, set First stage
H	↑	l	h	l	l	X	L	q_0	...	q_5	q_6	Shift, reset First stage
H	↑	l	h	h	l	X	$\overline{q}_0$	q_0	...	q_5	q_6	Shift, toggle First stage
H	↑	l	h	l	h	X	q_0	q_0	...	q_5	q_6	Shift, retain First stage
H	↑	l	l	X	X	d_n	d_0	d_1	...	d_6	d_7	Parallel load
H	↑	h	X	X	X	X	q_0	q_1	...	q_6	q_7	Hold (do nothing)

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

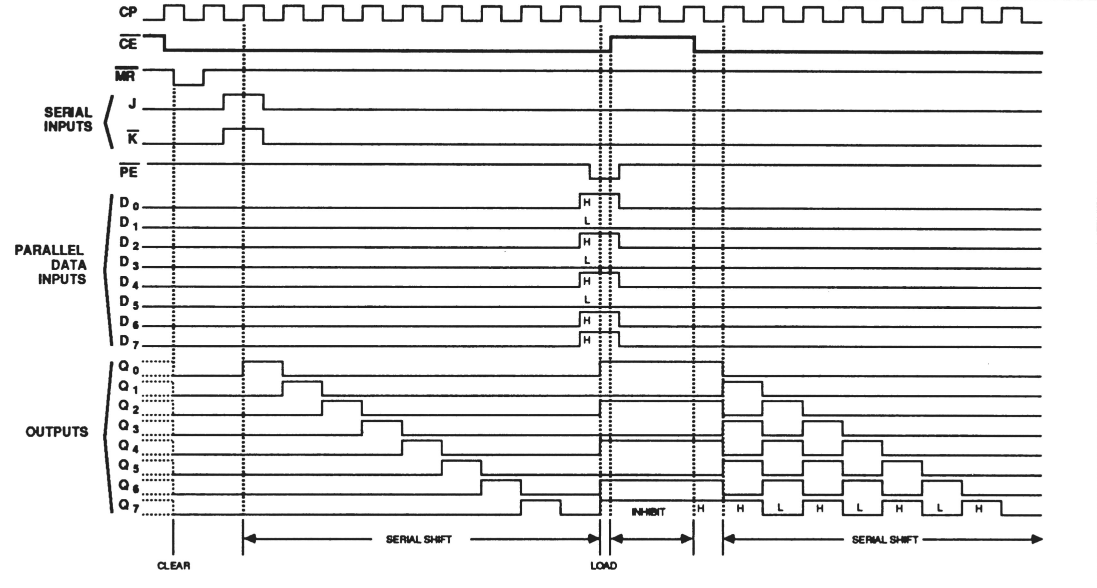
(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

TYPICAL TIMING DIAGRAM



Typical Clear, Load, Serial-Shift, Inhibit And Clear Sequences

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = -1mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = 20mA	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input clamp current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			65	90	mA
		I_{CCL}				75	105	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

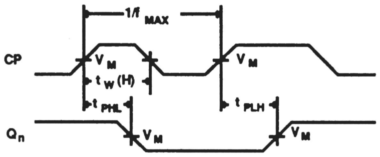
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	95		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	5.5 6.5	8.0 9.5	11.0 12.5	4.5 5.5	12.0 13.5	ns
t_{PHL}	Propagation delay, $\overline{MR}$ to Q_n	Waveform 2	5.5	8.0	10.5	5.0	12.0	ns

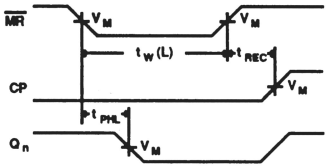
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 3	0.0 1.5			0.0 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 3	2.0 4.5			2.5 5.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low J, $\overline{K}$ to CP	Waveform 3	0.0 2.5			0.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J, $\overline{K}$ to CP	Waveform 3	0.0 3.5			0.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CE}$ to CP	Waveform 3	0.0 2.5			0.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP	Waveform 3	0.0 4.5			0.0 5.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 3	8.0 5.5			9.0 6.5		ns
$t_h(H)$ $t_h(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_w(H)$	CP Pulse width, High	Waveform 1	4.5			5.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	4.0			4.5		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 2	3.5			4.5		ns

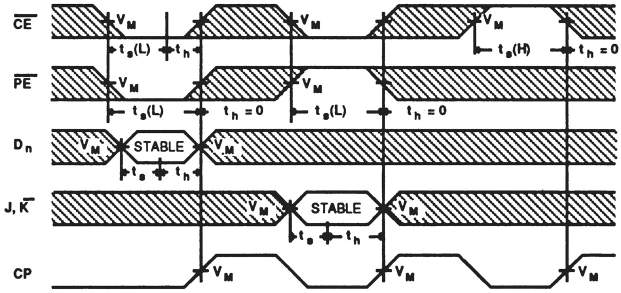
AC WAVEFORMS


1/f MAX
CP
V_M
$t_W(H)$
t_{PHL}
t_{PLH}
Q_n
V_M

Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths, and Maximum Clock Frequency


$\overline{MR}$
V_M
$t_W(L)$
t_{REC}
CP
V_M
t_{PHL}
Q_n
V_M

Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

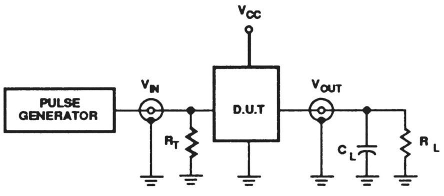

$\overline{CE}$
V_M
$t_s(L)$
t_h
$t_s(H)$
$t_h = 0$
$\overline{PE}$
$t_s(L)$
$t_h = 0$
D_n
STABLE
t_s
t_h
J, $\overline{K}$
STABLE
CP
V_M

Waveform 3. Setup Time and Hold Time

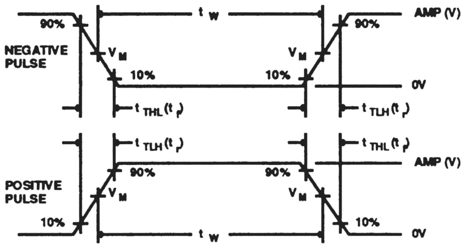
NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
R_T
D.U.T
V_{OUT}
C_L
R_L

Test Circuit For Totem-Pole Outputs


t_W
90%
AMP (V)
NEGATIVE PULSE
V_M
10%
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
POSITIVE PULSE
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
t_W

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F219A
64-Bit TTL Bipolar RAM

Product Specification

FAST Products

DESCRIPTION

The 74F219A is a high-speed, 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-State and are in the High-impedance state whenever the Chip Select ($\overline{CE}$) input is High. The outputs are active only in the Read mode and are of the same polarity as of the stored data.

Ordering information can be found on the following page.

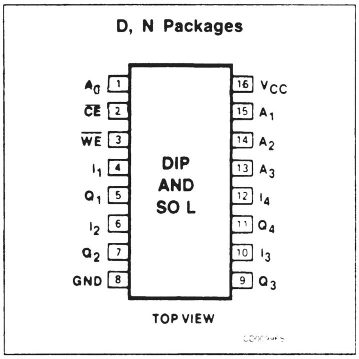
FEATURES

- **Address access time: 10ns max**
- **Power dissipation: 4.3mW/bit typ**
- **Schottky clamped TTL**
- **One chip enable input**
- **Non-inverting data outputs. (For inverting see 74F189A)**
- **I/O**
  - **Inputs: PNP Buffered**
  - **Outputs: 3-State**

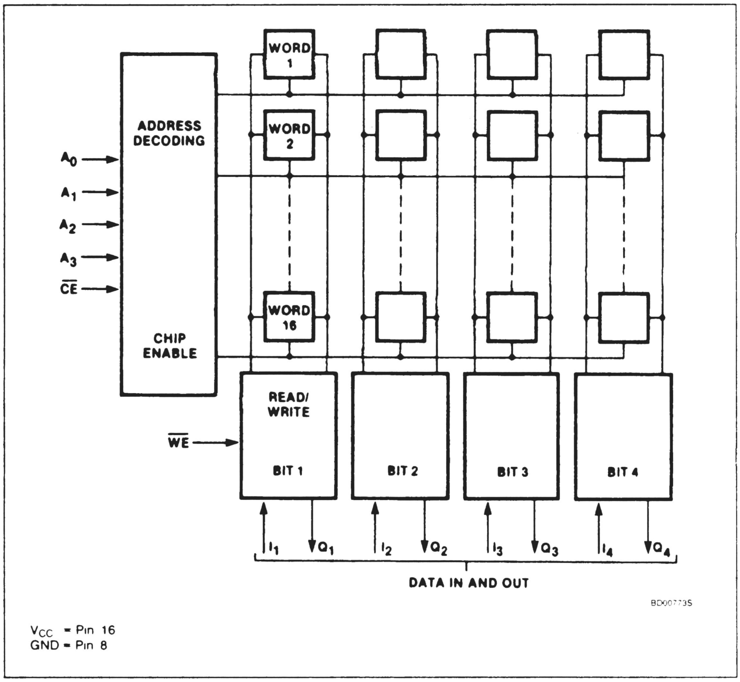
APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Push down stacks**
- **Control store**

PIN CONFIGURATION


D, N Packages
A_0 1
$\overline{CE}$ 2
$\overline{WE}$ 3
I_1 4
Q_1 5
I_2 6
Q_2 7
GND 8
16 V_{CC}
15 A_1
14 A_2
13 A_3
12 I_4
11 Q_4
10 I_3
9 Q_3
DIP AND SO L
TOP VIEW

BLOCK DIAGRAM


WORD 1
WORD 2
WORD 16
ADDRESS DECODING
CHIP ENABLE
A_0
A_1
A_2
A_3
$\overline{CE}$
$\overline{WE}$
READ/ WRITE
BIT 1
BIT 2
BIT 3
BIT 4
I_1
Q_1
I_2
Q_2
I_3
Q_3
I_4
Q_4
DATA IN AND OUT
BD00773S
V_{CC} = Pin 16
GND = Pin 8

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Plastic Dual-In-Line 300mil-wide	N74F219N
16-Pin Plastic Small Outline 300mil-wide	N74F219D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V_{DC}
V_{IN}	Input voltage	−0.5 to +7.0	V_{DC}
V_{OH}	Output voltage High	−0.5 to +5.5	V_{DC}
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +70°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input voltage[2]						
V_{IC}[7]	Clamp	$V_{CC} = 5.25V$, $I_I = -18mA$			−1.2	V
Output voltage						
		$V_{CC} = 4.75V$, $V_{IH} = 2.0V$, $V_{IL} = 0.8V$				V
V_{OH}	High	$I_{OH} = -3.0mA$	2.4			
V_{OL}[2,3]	Low	$I_{OL} = 20mA$		0.35	0.5	
Input current						
		$V_{CC} = 5.25V$				μA
I_{IH}	High	$V_{IN} = 5.5V$			40	
I_{IL}	Low	$V_{IN} = 0.5V$			0.6	
Output current						
		$V_{CC} = 5.25V$				
I_{OZ}	Off-state	$V_{IH} = 2.0V$, $2.4V \geqslant V_{OUT} \geqslant 0.5V$			±50	μA
I_{OS}[11]	Short circuit	(See Note)	−60		−150	mA
Supply current[6]						
I_{CC}		$V_{CC} = 5.25V$, $\overline{WE}$, $\overline{CE}$ = GND			70	mA
Capacitance						
		$V_{CC} = 5.0V$				pF
C_{IN}	Input	$V_{IN} = 2.0V$		5		
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	I_n	Q_n
Read	0	1	X	Same polarity as stored data
Write "0"	0	0	0	Hi-Z
Write "1"	0	0	1	Hi-Z
Disable	1	X	X	Hi-Z

X = Don't care

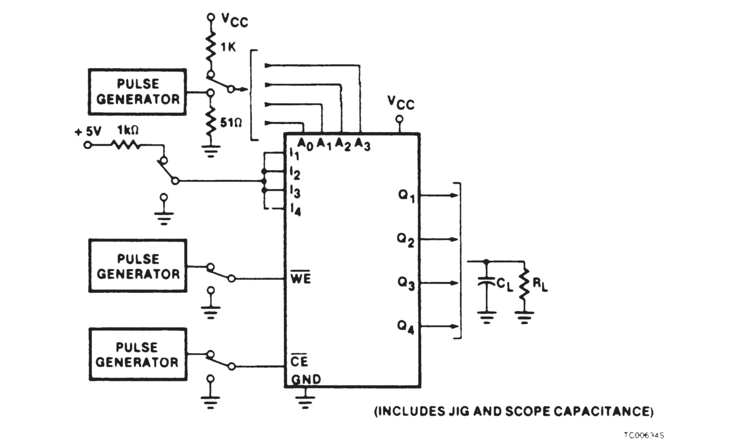
AC ELECTRICAL CHARACTERISTICS $R_L = 500\Omega$, $C_L = 50pF$, $0°C \leq T_A \leq +70°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
Access time							
t_{AA}	Address	Output	Address			10.5	ns
t_{CE}	Chip enable	Output	Chip enable			7.5	ns
Disable time[8]							
t_{CD}		Output	Chip enable			7.5	ns
Response time[8]							
t_{WD}		Output	Write enable			8.5	ns
Write recovery time							
t_{WR}		Output	Write enable			7.5	ns
Setup and hold time							
t_{WSA}[9] t_{WHA}	Setup time Hold time	Write enable	Address	0.5 0			ns
t_{WSD} t_{WHD}	Setup time Hold time	Write enable	Data in	5 0			
t_{WSC} t_{WHC}	Setup time Hold time	Write enable	$\overline{CE}$	4.5 4.5			
Pulse width							
t_{WP}[10]	Write enable			6.5			ns

NOTES:

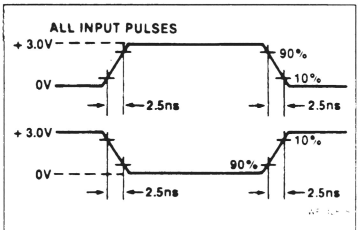
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Output sink current is supplied through a resistor to V_{CC}.
3. All sense outputs in Low state.
4. To guarantee a Write into the slowest bit.
5. Positive current is defined as into the terminal referenced.
6. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 0.45V, and the output open.
7. Test each input one at a time.
8. Measured at a delta of 0.3V from the logic level with $R_1 = 500\Omega$, $R_2 = 500\Omega$ and $C_L = 50pF$.
9. Measured with minimum t_{WP}.
10. Measured with minimum t_{WSA}.
11. For I_{OS} test: V_{CC} = 5.75 V V_{OUT} = 0.5 V

TEST LOAD CIRCUIT


VCC
1K
51Ω
PULSE GENERATOR
+5V 1kΩ
VCC
A0 A1 A2 A3
I1
I2
I3
I4
Q1
Q2
Q3
Q4
CL
RL
PULSE GENERATOR
WE
PULSE GENERATOR
CE
GND
(INCLUDES JIG AND SCOPE CAPACITANCE)
TC00634S

Loading Conditions

VOLTAGE WAVEFORM

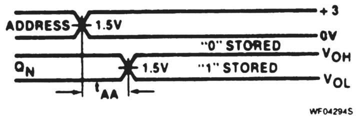

ALL INPUT PULSES
+3.0V
0V
90%
10%
2.5ns
2.5ns
+3.0V
0V
10%
90%
2.5ns
2.5ns

MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and output.

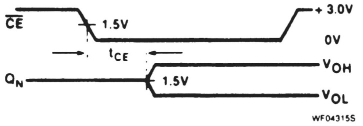
Input Pulses

TIMING DIAGRAMS

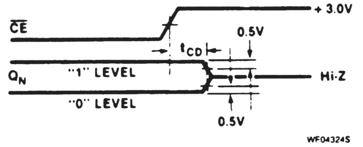
Read Cycle


ADDRESS
1.5V
+3
0V
"0" STORED
V_{OH}
Q_N
1.5V
"1" STORED
V_{OL}
t_{AA}
WF04294S

Address Access Time

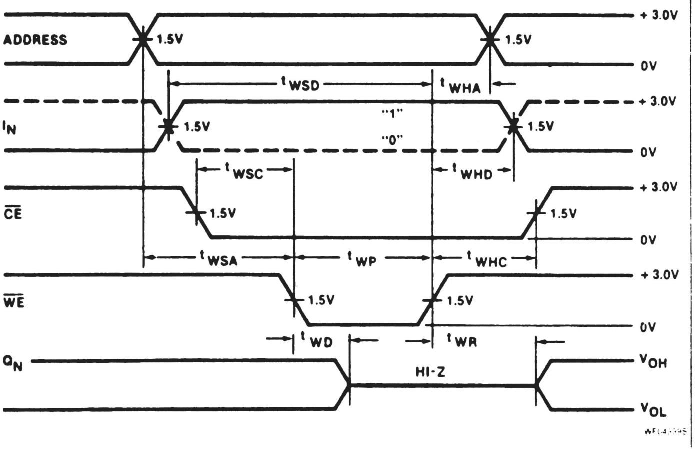

$\overline{CE}$
1.5V
+ 3.0V
0V
t_{CE}
V_{OH}
Q_N
1.5V
V_{OL}
WF04315S

Chip Enable


$\overline{CE}$
+ 3.0V
0.5V
t_{CD}
Q_N
"1" LEVEL
Hi-Z
"0" LEVEL
0.5V
WF04324S

Chip Disable

Write Cycle


ADDRESS
1.5V
1.5V
+ 3.0V
0V
t_{WSD}
t_{WHA}
I_N
1.5V
"1"
"0"
1.5V
+ 3.0V
0V
t_{WSC}
t_{WHD}
$\overline{CE}$
1.5V
1.5V
+ 3.0V
0V
t_{WSA}
t_{WP}
t_{WHC}
$\overline{WE}$
1.5V
1.5V
+ 3.0V
0V
t_{WD}
t_{WR}
Q_N
HI-Z
V_{OH}
V_{OL}

All AC parameters are measured at 1.5V unless otherwise specified.

FAST 74F222

16X4 Synchronous FIFO (3-State)

Preliminary Specification

FEATURES

- Independent synchronous inputs and outputs
- Organized as 16-words of 4 bits
- DC to 50Mhz data rate
- 3-state outputs
- Cascadable in word-width and depth direction

DESCRIPTION

This 64-bit active element First-In-First-Out (FIFO) is a monolithic Schottky-clamped transistor-transistor logic (STTL) array organized as 16-words of 4-bits each. A memory system using the 'F222 can be easily expanded in multiples of 15m+1 words or of 4n bits, or both, (where n is the number of packages in the vertical array and m is the number of packages in the horizontal array) and no external gating is required (see in Figure 2). The 3-state outputs controlled by a single enable input (OE) make bus connection and multiplexing easy. The 'F222 processes data in a parallel format at any desired clock rate from DC to 50Mhz.

Reading or writing is done independently utilizing separate synchronous data clocks. Data may be written into the array on the high-to-low transition of the load clock (LDCK) input. Data may be read out of the array on the low-to-high transition of the unload clock (UNCK). The FIFO is full when the number of words clocked in exceeds the number of words clocked out by 16. When the FIFO is full, LDCK signals have no effect. When the FIFO is empty, UNCK signals have no effect.

Status of the 'F222 is provided by two outputs. Input Ready (IR) monitors the status of the last word location and signifies when the FIFO is full. This output is high whenever the FIFO is available to accept new data and LDCK input is low. Output Ready (OR), is high when the first word location contains valid data and UNCK is high. Both IR and OR outputs are enabled by Input Ready Enable (IRE) and Output Ready Enable (ORE) inputs respectively. The first word location is defined as the location from which data is provided to the outputs.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F222	50MHz	90mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	74F222N
20-Pin Plastic SOL	74F222D

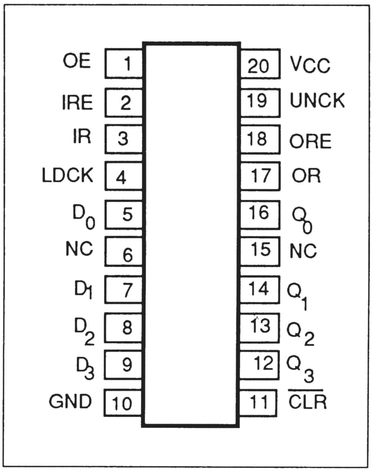
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
LDC	Load clock input	1.0/1.0	20µA/0.6mA
D_0-D_3	Data inputs	1.0/1.0	20µA/0.6mA
OE	Output enable input (active High)	1.0/1.0	20µA/0.6mA
UNCK	Unload clock input	1.0/1.0	20µA/0.6mA
$\overline{CLR}$	Clear (active Low) input	1.0/1.0	20µA/0.6mA
IRE/ORE	Input Ready and Output Ready enable	1.0/1.0	20µA/0.6mA
IR	Input Ready output	55/33	1.0mA/20mA
Q_0-Q_3	Data outputs	55/33	1.0mA/20mA
OR	Output Ready	55/33	1.0mA/20mA

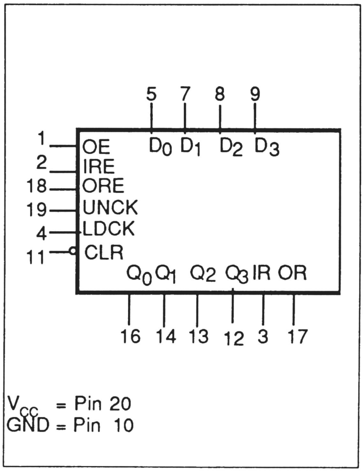
NOTE:

One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



LOGIC SYMBOL



FAST 74F224

16X4 Synchronous FIFO (3-State)

Preliminary Specification

FEATURES

- **Independent synchronous inputs and outputs**
- **Organized as 16-words of 4 bits**
- **DC to 50Mhz data rate**
- **3-state outputs**
- **Cascadable in word-width and depth direction**

DESCRIPTION

This 64-bit active element First-In-First-Out (FIFO) is a monolithic Schottky-clamped transistor-transistor logic (STTL) array organized as 16-words of 4-bits each. A memory system using the 'F224 can be easily expanded in multiples of 15m+1 words or of 4n bits, or both, (where n is the number of packages in the vertical array and m is the number of packages in the horizontal array) however some external gating is required (see in Figure 2). For longer words using the 'F224, the IR signals of the first-rank packages and OR signals of the last-rank packages must be ANDed for proper synchronization. The 3-state outputs controlled by a single enable input (OE) make bus connection and multiplexing easy. The 'F224 processes data in a parallel format at any desired clock rate from DC to 50Mhz.

Reading or writing is done independently utilizing separate synchronous data clocks. Data may be written into the array on the high-to-low transition of the load clock (LDCK) input. Data may be read out of the array on the low-to-high transition of the unload clock (UNCK). The FIFO is full when the number of words clocked in exceeds the number of words clocked out by 16. When the FIFO is full, LDCK signals have no effect. When the FIFO is empty, UNCK signals have no effect.

Status of the 'F224 is provided by two outputs. Input Ready (IR) monitors the status of the last word location and signifies when the FIFO is full. This output is high whenever the FIFO is available to accept new data and LDCK input is low. Output Ready (OR), is high when the first word location contains valid data and UNCK is high. The first word location is defined as the location from which data is provided to the outputs.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F224	50MHz	90mA

ORDERING INFORMATION

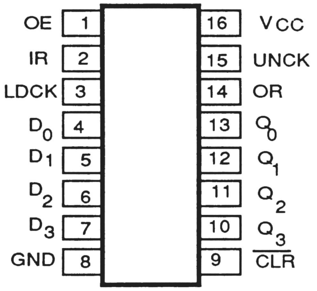
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	74F224N
16-Pin Plastic SOL	74F224D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

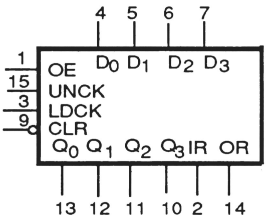
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
LDC	Load clock input	1.0/1.0	20μA/0.6mA
D_0-D_3	Data inputs	1.0/1.0	20μA/0.6mA
OE	Output enable input (active High)	1.0/1.0	20μA/0.6mA
UNCK	Unload clock input	1.0/1.0	20μA/0.6mA
$\overline{CLR}$	Clear (active Low) input	1.0/1.0	20μA/0.6mA
IR	Input Ready output	55/33	1.0mA/20mA
Q_0-Q_3	Data outputs	55/33	1.0mA/20mA
OR	Output Ready	55/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FAST 74F225

16X5 Asynchronous FIFO (3-State)

Preliminary Specification

FEATURES

- Independent synchronous inputs and outputs
- Organized as 16-words of 5 bits
- DC to 50Mhz data rate
- 3-state outputs
- Cascadable in word-width and depth direction

DESCRIPTION

This 80-bit active element First-In-First-Out (FIFO) is a monolithic Schottky-clamped transistor-transistor logic (STTL) array organized as 16-words of 5-bits each. A memory system using the 'F225 can be easily expanded in multiples of 16-words or of 5-bits as shown in Figure 2. The 3-state outputs controlled by a single enable input ($\overline{OE}$) make bus connection and multiplexing easy. The 'F225 processes data in a parallel format at any desired clock rate from DC to 50Mhz.

Reading or writing is done independently utilizing separate synchronous data clocks. Data may be written into the array on the low-to-high transition of either load clock (CP_A or CP_B) input. Data may be read out of the array on the low-to- high transition of the unload clock (CP_{IN}).When writing data into the FIFO, one of the load clock inputs must be held high while the other strobes data into the FIFO. This arrangement allows either load clock to function as an inhibit for the other. Status of the 'F225 is provided by three outputs. Input Ready (IR) monitors the status of the last word location and signifies when the FIFO is full. This output is high whenever the FIFO is available to accept new data. The unload clock output (CP_{OUT}) also monitors the last word location. This output generates a low-logic-level pulse (synchronized to the internal clock pulse) when the location is vacant. The third status output, Output Ready (OR), is high when the first word location contains valid data and unload clock input is high. When unload clock input goes low, OR will go low and remain low until new valid data is in the first word location. The first word location is defined as the location from which data is provided to the outputs.

The data outputs are noninverting with

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F225	50MHz	95mA

ORDERING INFORMATION

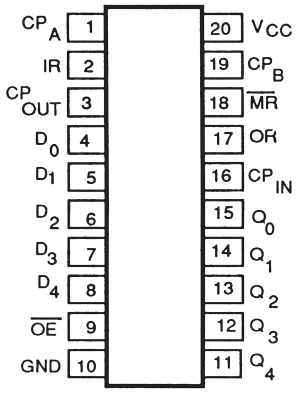
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	74F225N
20-Pin Plastic SOL	74F225D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

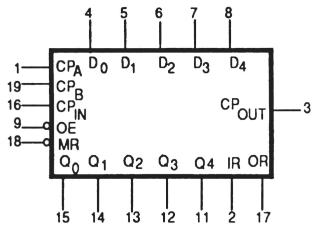
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
CP_A, CP_B	Load clock A and Load clock B inputs	1.0/1.0	20µA/0.6mA
D_0-D_4	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20µA/0.6mA
CP_{IN}	Unload clock input	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
IR	Input Ready output	55/33	1.0mA/20mA
CP_{OUT}	Unload clock output (active Low)	55/33	1.0mA/20mA
Q_0-Q_4	Data outputs	55/33	1.0mA/20mA
OR	Output Ready	55/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



LOGIC SYMBOL

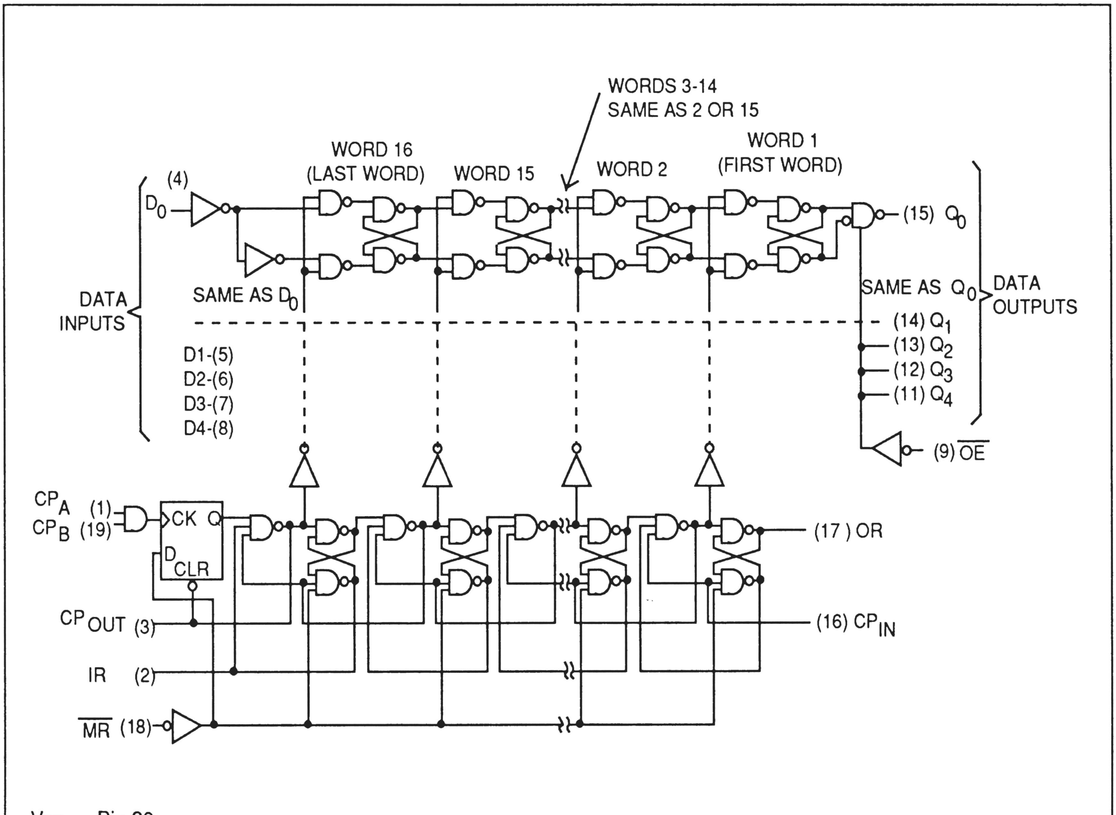


V_{CC} = Pin 20
GND = Pin 10

respect to the data inputs and are 3-stated when $\overline{\text{OE}}$ input is high. When $\overline{\text{OE}}$ is low, the data outputs are enabled to function as totem-pole outputs.

A high-to-low transition on the Master Reset ($\overline{\text{MR}}$) input invalidates all data stored in the FIFO by clearing the control logic and setting OR low. This high-to-low transition on the $\overline{\text{MR}}$ input does not effect the data outputs but since OR is driven low, it signifies invalid data on the outputs.

LOGIC DIAGRAM


WORDS 3-14
SAME AS 2 OR 15
WORD 16
(LAST WORD)
WORD 15
WORD 2
WORD 1
(FIRST WORD)
(4)
D0
(15) Q0
DATA INPUTS
SAME AS D0
SAME AS Q0
DATA OUTPUTS
(14) Q1
(13) Q2
(12) Q3
(11) Q4
D1-(5)
D2-(6)
D3-(7)
D4-(8)
(9) OE
CPA (1)
CPB (19)
CK Q
D
CLR
(17) OR
CP OUT (3)
(16) CPIN
IR (2)
MR (18)

Vcc = Pin 20
GND = Pin 10

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	All inputs	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			55	80	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency CP_A	Waveform 3						MHz
f_{MAX}	Maximum clock frequency CP_B	Waveform 3						MHz
f_{MAX}	Maximum clock frequency CP_{IN}	Waveform 2						MHz
IW	CP_{OUT}	Waveform 4						ns
t_{PLH}/t_{PHL}	Propagation delay CP_{IN} to Q_n	Waveform 2						ns
t_{PLH}	Propagation delay CP_A OR CP_B to OR	Waveform 4						ns
t_{PLH}/t_{PHL}	Propagation delay CP_{IN} to OR	Waveform 2						ns
t_{PHL}	Propagation delay $\overline{MR}$ to OR	Waveform 3						ns
t_{PHL}	Propagation delay CP_A OR CP_B to CP_{OUT}	Waveform 4						ns
t_{PHL}	Propagation delay CP_A OR CP_B to IR	Waveform 3						ns
t_{PLH}	Propagation delay CP_{IN} to IR	Waveform 2						ns
t_{PLH}	Propagation delay $\overline{MR}$ to IR	Waveform 3						ns
t_{PLH}/t_{PHL}	Propagation delay Q_n to OR	Waveform 4						ns
t_{PZH}	Output enable time to HIGH level	Waveform 5						ns
t_{PZL}	Output enable time to LOW level	Waveform 5						ns
t_{PHZ}	Output disable time to HIGH level	Waveform 5, C_L=5.0pF						ns
t_{PLZ}	Output disable time to LOW level	Waveform 5, C_L=5.0pF						ns

AC SET-UP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	
t_W	Load clock CP_A or CP_B High pulse-width	Waveform 1						ns
t_W	Load clock CP_A or CP_B Low pulse-width	Waveform 1						ns
t_W	Master reset pulse width	Waveform 1						ns
t_S	D_0-D_4 set-up time to CP_A or CP_B	Waveform 1						ns
t_S	$\overline{MR}$ Set-up time to CP_A or CP_B	Waveform 1						ns
t_H	D_0-D_4 hold time after CP_A or CP_B	Waveform 1						ns

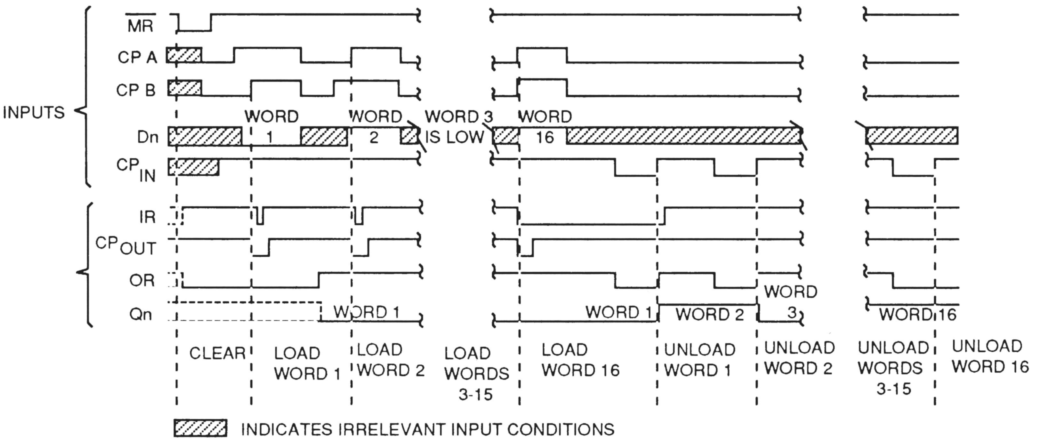

INPUTS
MR
CP A
CP B
Dn
CP IN
IR
CP OUT
OR
Qn
WORD 1
WORD 2
WORD 3 IS LOW
WORD 16
WORD 1
WORD 1
WORD 2
WORD 3
WORD 16
CLEAR
LOAD WORD 1
LOAD WORD 2
LOAD WORDS 3-15
LOAD WORD 16
UNLOAD WORD 1
UNLOAD WORD 2
UNLOAD WORDS 3-15
UNLOAD WORD 16
▨ INDICATES IRRELEVANT INPUT CONDITIONS

Figure 1: Typical Functional Waveforms for the 'F225 FIFO

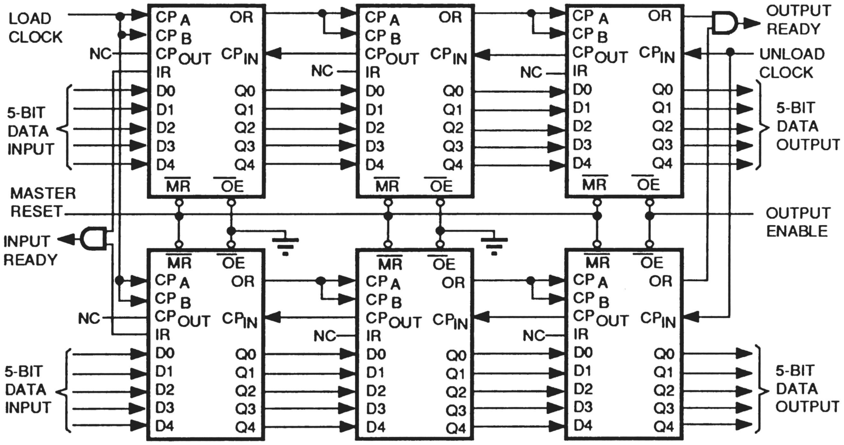
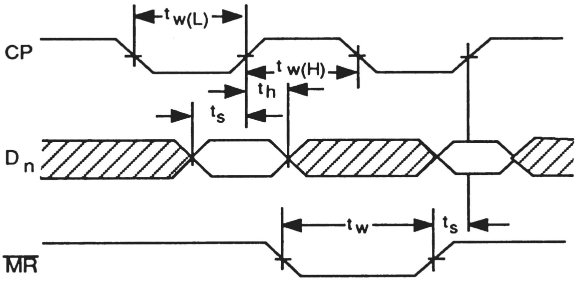
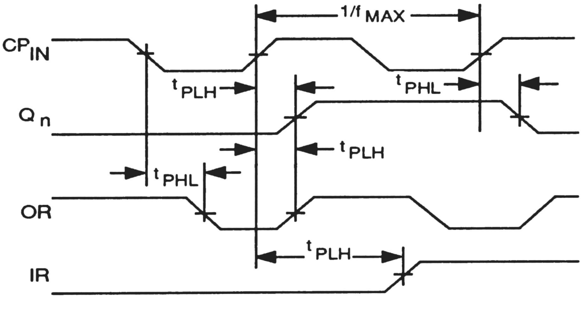

LOAD CLOCK
NC
5-BIT DATA INPUT
MASTER RESET
INPUT READY
CP A
CP B
CP OUT
CP IN
IR
D0
D1
D2
D3
D4
OR
Q0
Q1
Q2
Q3
Q4
MR
OE
OUTPUT READY
UNLOAD CLOCK
5-BIT DATA OUTPUT
OUTPUT ENABLE

Figure 2: Expanding The 'F225 FIFO (48 words of 10 bits)

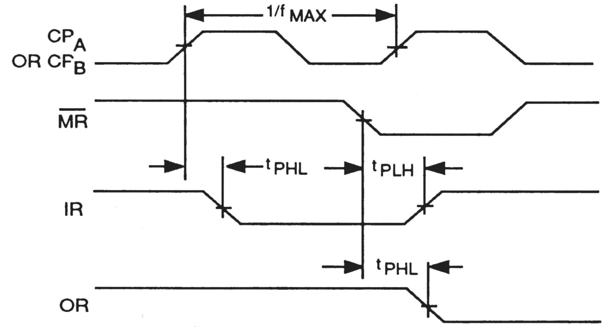
AC WAVEFORMS


CP
t w(L)
t w(H)
t h
t s
D n
t w
t s
MR

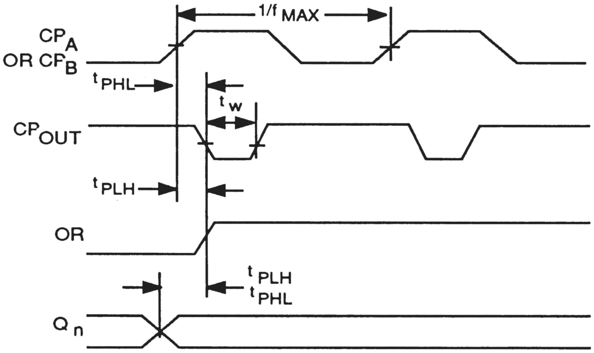
Waveform 1: $\overline{MR}$ and Clock Pulse Widths, Data Set-up and Hold Times and $\overline{MR}$ to Clock Set-up Time


CP IN
1/f MAX
t PLH
t PHL
Q n
t PLH
t PHL
OR
t PLH
IR

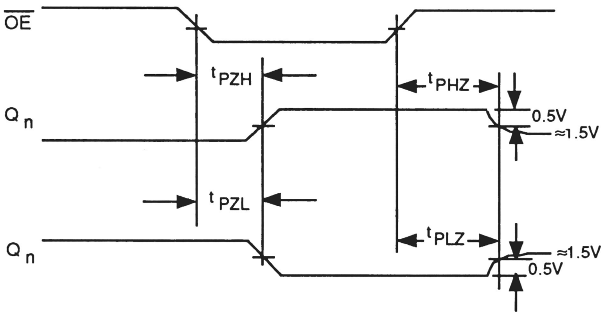
Waveform 2: CP_{IN} to Output Delays


1/f MAX
CPA OR CFB
MR
tPHL
tPLH
IR
tPHL
OR

Waveform 3: CP_A or CP_B to IR Delay and $\overline{MR}$ to IR and OR Delay

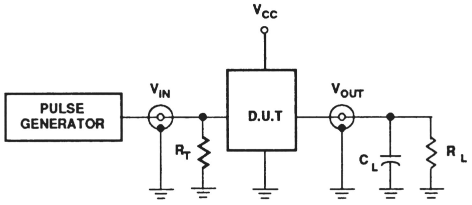

1/f MAX
CPA OR CFB
tPHL
tw
CPOUT
tPLH
OR
tPLH
tPHL
Qn

Waveform 4: CP_A or CP_B to CP_{OUT} and OR Delay, CP_{OUT} Pulse Width and Q_n to OR Delay

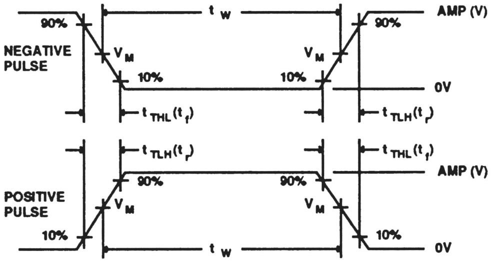

OE
tPZH
tPHZ
Qn
0.5V
≈1.5V
tPZL
tPLZ
Qn
≈1.5V
0.5V

Waveform 5: $\overline{OE}$ to Q_n Delay

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
R_T
D.U.T
V_{OUT}
C_L
R_L

Test Circuit For Totem-Pole Outputs


90%
t_W
AMP (V)
NEGATIVE PULSE
V_M
10%
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
POSITIVE PULSE

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F322

Register

8-Bit Serial/Parallel Register With Sign Extend (3-State)

Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F322	125 MHz	60mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F322N
20-Pin Plastic SOL	N74F322D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0, D_1	Serial data inputs	1.0/1.0	20μA/0.6mA
S	Serial data select input	1.0/2.0	20μA/1.2mA
$\overline{SE}$	Sign Extend input	1.0/3.0	20μA/1.8mA
CP	Clock Pulse input (Active rising edge)	1.0/1.0	20μA/0.6mA
S/$\overline{P}$	Serial (High) or Parallel (Low) mode control input	1.0/1.0	20μA/0.6mA
$\overline{RE}$	Register Enable input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Asynchronous Master Reset input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20μA/0.6mA
Q_7	Bi-state serial output	50/33	1.0mA/20mA
I/O_n	Multiplexed parallel data inputs or	3.5/1.0	70μA/0.6mA
	3-state parallel outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

FEATURES

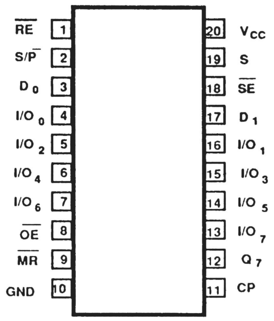
- **Multiplexed parallel I/O ports**
- **Separate serial input and output**
- **Sign extend function**
- **3-state outputs for bus applications**
- **Direct Overriding Clear**

DESCRIPTION

The 74F322 is an 8-bit shift register with provision for either serial or parallel loading and with 3-state parallel outputs plus a bi-state serial output. Parallel data inputs and outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store), shift right with serial entry, shift right with sign extend, and parallel load. An asynchronous Master Reset ($\overline{MR}$) input overrides clocked operation and clears the register.

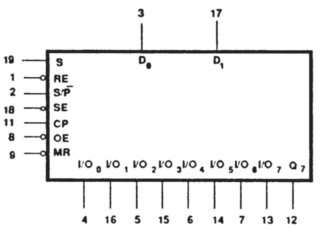
The 'F322 contains eight D-type edge triggered flip-flops and the interstage gating required to perform right shift and the intrastage gating necessary for hold and synchronous parallel load operations. A Low signal on $\overline{RE}$ enables shifting or parallel loading, while a High signal enables the hold mode. A High signal on S/$\overline{P}$ enables shift right, while a Low signal disables the 3-state output buffers and enables parallel loading. In the shift right mode a High signal on $\overline{SE}$ enables serial entry from either D_0 or D_1, as determined by the S input. A Low signal on $\overline{SE}$ enables shift right but Q_7 reloads its contents thus performing the sign extend function. A High signal on $\overline{OE}$ disables the 3-state output buffers, regardless of the other control inputs. In this condition the shifting and loading operations can still be performed.

PIN CONFIGURATION



RE 1
S/P 2
D0 3
I/O0 4
I/O2 5
I/O4 6
I/O6 7
OE 8
MR 9
GND 10
20 VCC
19 S
18 SE
17 D1
16 I/O1
15 I/O3
14 I/O5
13 I/O7
12 Q7
11 CP

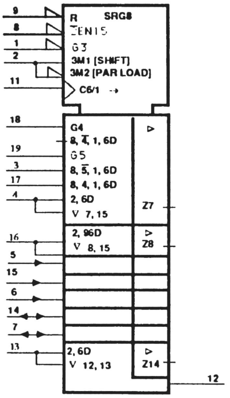
LOGIC SYMBOL



3
17
19
1
2
18
11
8
9
S
RE
S/P
SE
CP
OE
MR
D0
D1
I/O0 I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7 Q7
4 16 5 15 6 14 7 13 12

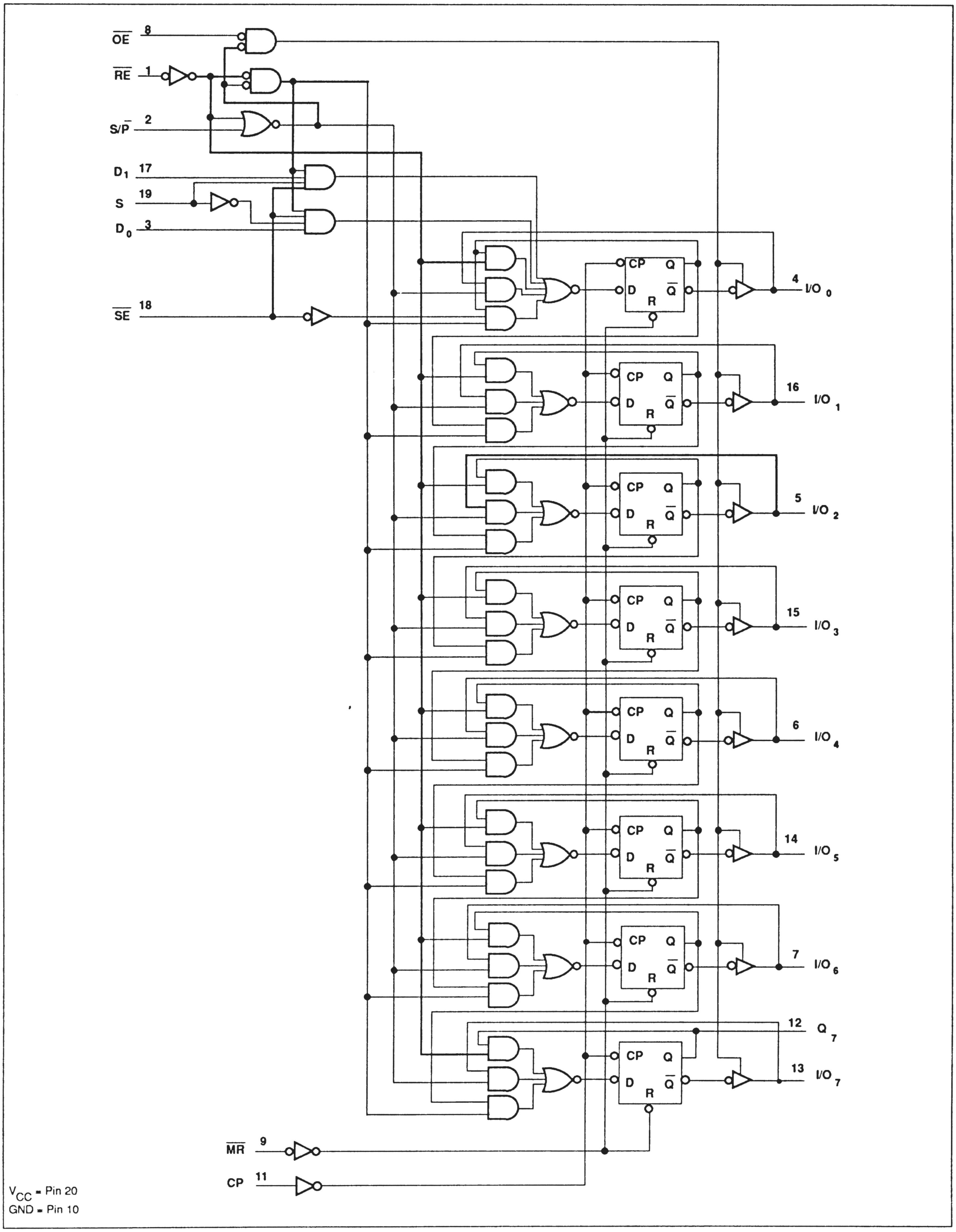
V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)



9
8
1
2
11
R
SRG8
ĒN15
G3
3M1 [SHIFT]
3M2 [PAR LOAD]
C6/1 →
18
19
3
17
4
G4
8, 4̄, 1, 6D
G5
8, 5̄, 1, 6D
8, 4, 1, 6D
2, 6D
V 7, 15
Z7
16
5
15
6
14
7
13
2, 96D
V 8, 15
Z8
2, 6D
V 12, 13
Z14
12

LOGIC DIAGRAM


OE 8
RE 1
S/P 2
D1 17
S 19
D0 3
SE 18
CP
D
Q
Q
R
4 I/O0
16 I/O1
5 I/O2
15 I/O3
6 I/O4
14 I/O5
7 I/O6
12 Q7
13 I/O7
MR 9
CP 11
VCC = Pin 20
GND = Pin 10

FUNCTION TABLE

INPUTS							OUTPUTS									OPERATING MODE
$\overline{MR}$	$\overline{RE}$	$S/\overline{P}$	$\overline{SE}$	S	$\overline{OE}$*	CP	I/O_0	I/O_1	I/O_2	I/O_3	I/O_4	I/O_5	I/O_6	I/O_7	Q_7	
L L	H X	X H	X X	X X	L L	X X	L L	L L	L L	L L	L L	L L	L L	L L	L L	Clear
H	L	L	X	X	X	↑	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_7	Parallel load
H H	L L	H H	H H	L H	L L	↑ ↑	D_0 D_1	O_0 O_0	O_1 O_1	O_2 O_2	O_3 O_3	O_4 O_4	O_5 O_5	O_6 O_6	O_6 O_6	Shift right
H	L	H	L	X	L	↑	O_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_6	Sign extend
H	H	X	X	X	L	X	NC	NC	NC	NC	NC	NC	NC	NC	NC	Hold
X X	L X	L X	X X	X X	X H	X $\not\uparrow$	Z Z	Z Z	Z Z	Z Z	Z Z	Z Z	Z Z	Z Z	NC NC	3-State

H = High voltage level
L = Low voltage level
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
I_0-I_7 = The level of the steady state input at the respective I/O terminal is loaded into the flip-flop while the flip-flop outputs (except Q_7) are isolated from the I/O terminal.
D_0-D_7 = The level of the steady state inputs to the serial multiplexer input.
O_0-O_7 = The level of the respective Q_n flip-flop prior to the last clock Low-to-High transition.
* = When the input is High, all I/O terminals are at the high impedance state, sequential operation or clearing of the register is not affected.
$\not\uparrow$ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	Q_7	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_7			-1	mA
		I/O_n			-3	mA
I_{OL}	Low-level output current	Q_7			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	Q_7	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O_n		I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}		0.38	0.55	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = MAX, V_I = 7.0V					100	μA
		I/O_n	V_{CC} = MAX, V_I = 5.5V					1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	$\overline{SE}$	V_{CC} = MAX, V_I = 0.5V					-1.8	mA
		S						-1.2	mA
		others						-0.6	mA
$I_{IH}+I_{OZH}$	Off-state output current High-level voltage applied		V_{CC} = MAX, V_I = 2.7V					70	μA
$I_{IL}+I_{OZL}$	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				50	75	mA
		I_{CCL}					60	90	mA
		I_{CCZ}					65	95	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

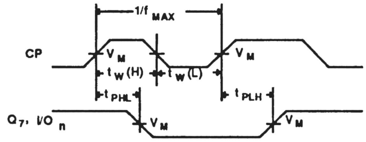
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	110	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	4.0 4.5	6.0 7.0	9.0 9.5	4.0 4.5	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_7	Waveform 1	4.5 5.0	6.5 6.5	9.0 9.0	4.5 5.0	10.0 9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/O_n	Waveform 2	5.0	6.5	9.5	4.5	10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_7	Waveform 2	5.0	6.5	9.5	4.5	10.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to I/O_n	Waveform 4 Waveform 5	3.0 5.5	5.0 7.5	8.0 10.5	3.0 5.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to I/O_n	Waveform 4 Waveform 5	2.0 1.0	4.0 2.5	6.5 5.5	2.0 1.0	7.5 6.0	ns
t_{PZH} t_{PZL}	Output Enable time S/$\overline{P}$ to I/O_n	Waveform 4 Waveform 5	4.0 6.0	6.0 8.0	9.0 11.0	3.5 5.5	10.0 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time S/$\overline{P}$ to I/O_n	Waveform 4 Waveform 5	4.0 2.0	6.0 4.0	9.0 7.0	3.5 2.0	10.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{RE}$ to I/O_n	Waveform 4 Waveform 5	8.0 9.0	9.5 11.0	12.5 14.0	7.0 8.0	14.0 16.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{RE}$ to I/O_n	Waveform 4 Waveform 5	6.5 4.5	8.5 6.5	11.5 9.5	5.5 4.0	13.0 10.5	ns

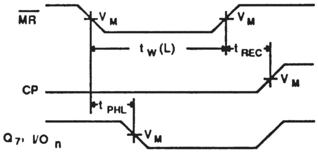
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{RE}$ to CP	Waveform 3	8.0 12.5			9.5 14.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{RE}$ to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_0, D_1 or I/O_n to CP	Waveform 3	4.0 4.5			6.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_0, D_1 or I/O_n to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{SE}$ to CP	Waveform 3	5.5 5.0			7.0 5.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{SE}$ to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S/$\overline{P}$ to CP	Waveform 3	10.5 9.5			11.0 10.5		ns
$t_s(H)$ t_sL)	Setup time, High or Low S to CP	Waveform 3	4.0 8.5			4.5 9.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S or S/$\overline{P}$ to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 3	5.0 5.0			5.0 5.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 3	5.0			5.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 2	4.0			4.5		ns

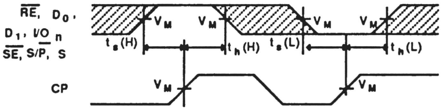
AC WAVEFORMS


1/f MAX
CP
V_M
t_W(H)
t_W(L)
t_{PHL}
t_{PLH}
Q_7, I/O n

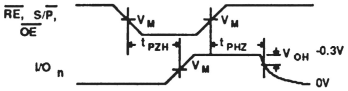
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency


MR
V_M
t_W(L)
t_{REC}
CP
t_{PHL}
Q_7, I/O n

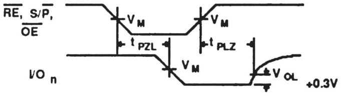
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time


RE, D_0, D_1, I/O n
SE, S/P, S
V_M
t_s(H)
t_h(H)
t_s(L)
t_h(L)
CP

Waveform 3. Data Setup And Hold Times


RE, S/P, OE
V_M
t_{PZH}
t_{PHZ}
V_{OH} -0.3V
I/O n
0V

Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level

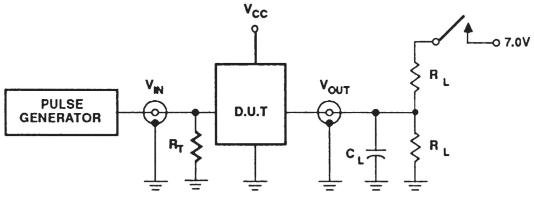

RE, S/P, OE
V_M
t_{PZL}
t_{PLZ}
I/O n
V_{OL}
+0.3V

Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

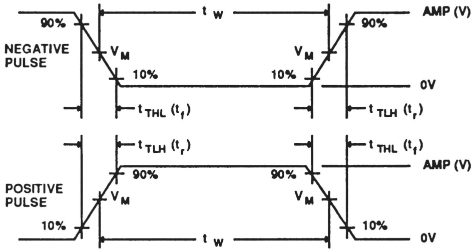
NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
7.0V
PULSE GENERATOR
V_{IN}
D.U.T
V_{OUT}
R_L
R_T
C_L
R_L

Test Circuit For 3-State Outputs


t_W
AMP (V)
90%
NEGATIVE PULSE
V_M
10%
0V
t_{THL} (t_f)
t_{TLH} (t_r)
POSITIVE PULSE

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F410

Register Stack — 16 X 4 RAM 3-State Output Register

Product Specification

FEATURES

- **Edge-triggered output register**
- **Typical access time of 24ns**
- **3-State outputs**
- **Optimized for register stack operation**
- **18-pin package**

DESCRIPTION

The 'F410 is a register-oriented high-speed 64-bit Read/Write Memory organized as 16-words by 4-bits. An edge-triggered 4-bit output register allows new input data to be written while previous data is held. 3-State outputs are provided for maximum versatility. The 'F410 is fully compatible with all TTL families.

TYPE	TYPICAL ACCESS TIME	TYPICAL SUPPLY CURRENT (TOTAL)
74F410	24ns	47mA

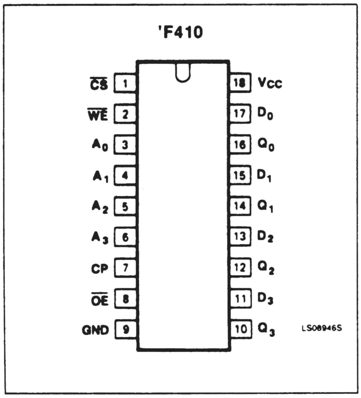
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
18-Pin Plastic Dual-In-Line 300mil-wide	N74F410N

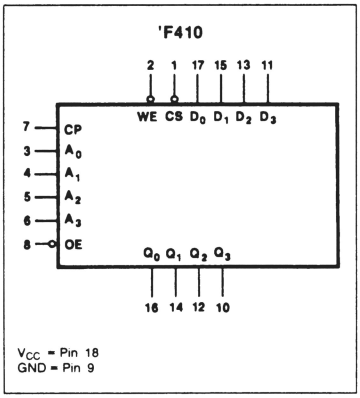
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_3$	Address Inputs	1.0/1.0	20μA/0.6μA
$D_0 - D_3$	Data Inputs	1.0/1.0	20μA/0.6μA
$\overline{CS}$	Chip Select Input (Active Low)	1.0/2.0	20μA/1.2μA
$\overline{OE}$	Output Enable Input (Active Low)	1.0/1.0	20μA/0.6μA
$\overline{WE}$	Write Enable Input (Active Low)	1.0/1.0	20μA/0.6μA
CP	Clock Input (Outputs change on Low-to-High Transition)	1.0/2.0	20μA/1.2μA
$Q_0 - Q_3$	Outputs	150/40	3mA/24mA

PIN CONFIGURATION


'F410
CS 1
WE 2
A0 3
A1 4
A2 5
A3 6
CP 7
OE 8
GND 9
18 Vcc
17 D0
16 Q0
15 D1
14 Q1
13 D2
12 Q2
11 D3
10 Q3
LS08946S

LOGIC SYMBOL


'F410
2 1 17 15 13 11
WE CS D0 D1 D2 D3
7 CP
3 A0
4 A1
5 A2
6 A3
8 OE
Q0 Q1 Q2 Q3
16 14 12 10
VCC = Pin 18
GND = Pin 9

Register Stack — 16 × 4 RAM 3-State Output Register

FAST 74F410

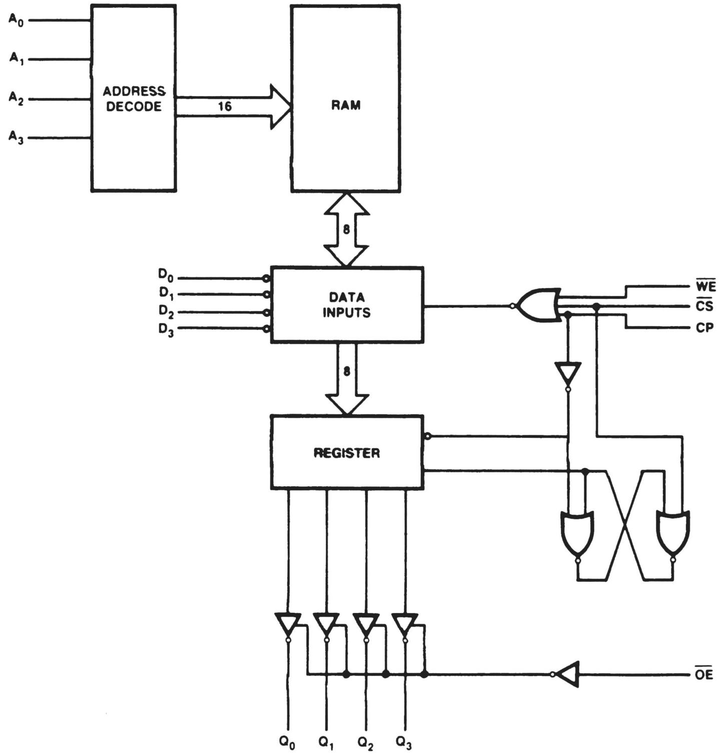
FUNCTIONAL DESCRIPTION

Write Operation — When the three control inputs, Write Enable ($\overline{WE}$), Chip Select ($\overline{CS}$), and Clock (CP), are Low the information on the data inputs ($D_0 - D_3$) is written *into the* memory location selected by the address inputs ($A_0 - A_3$). If the input data changes while $\overline{WE}$, $\overline{CS}$, and CP are Low, the contents of the selected memory location follow these changes, provided setup and hold time criteria are met.

Read Operation — Whenever $\overline{CS}$ is Low, $\overline{WE}$ is High, and CP goes from Low-to-High, the contents of the memory location selected by the address inputs ($A_0 - A_3$) are edge-triggered into the Output Register.

The ($\overline{OE}$) input controls the output buffers. When $\overline{OE}$ is High the four outputs ($Q_0 - Q_3$) are in a high impedance or OFF state; when $\overline{OE}$ is Low, the outputs are determined by the state of the Output Register.

BLOCK DIAGRAM



A_0
A_1
A_2
A_3
ADDRESS DECODE
16
RAM
8
D_0
D_1
D_2
D_3
DATA INPUTS
$\overline{WE}$
$\overline{CS}$
CP
8
REGISTER
$\overline{OE}$
Q_0
Q_1
Q_2
Q_3

BD00000S

Register Stack — 16 × 4 RAM 3-State Output Register

FAST 74F410

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OH} = MAX	± 10% V_{CC}	2.4			V
					± 5% V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OL} = MAX	± 10% V_{CC}		0.35	0.5	V
					± 5% V_{CC}		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$					-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	$A_0 - A_3$, $D_0 - D_3$, $\overline{WE}$, $\overline{OE}$	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		CP, $\overline{CS}$						-1.2	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_{OUT} = 2.7V					50	μA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_{OUT} = 0.5V					-50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX					70	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

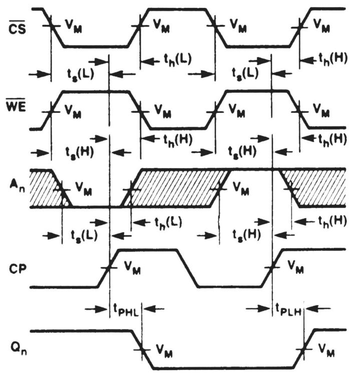
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F410					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay CP ↑ to Q	See Waveforms	3.0 3.5	6.5 7.0	8.5 9.0	2.5 3.0	9.5 10.0	ns
t_{PZH} t_{PZL}	Enable time $\overline{OE}$ to Q	See Waveforms	3.0 3.5	6.0 7.0	8.0 9.0	2.5 3.0	9.0 10.0	ns
t_{PHZ} t_{PLZ}	Disable time $\overline{OE}$ to Q	See Waveforms	2.5 2.5	4.5 5.0	6.5 7.5	2.0 2.0	7.5 8.0	

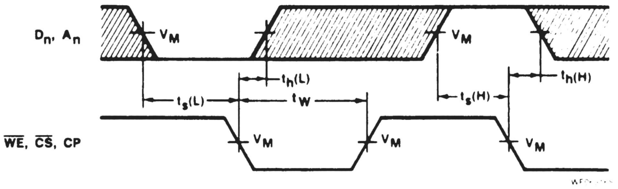
AC SETUP AND HOLD REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F410					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
READ MODE								
$t_s(L)$	Setup time Low $\overline{CS}$ to CP ↑							ns
$t_h(L)$	Hold time Low $\overline{CS}$ to CP ↑							ns
$t_s(H)$ $t_s(L)$	Setup time High or Low A_n to CP ↑	See Waveforms	15.0 15.0			17.0 17.0		ns
$t_h(H)$ $t_h(L)$	Hold time High or Low A_n to CP ↑	See Waveforms	0 0			0 0		
$t_s(H)$	Setup time High $\overline{WE}$ to CP ↑	See Waveforms						ns
$t_h(H)$	Hold time High $\overline{WE}$ to CP ↑	See Waveforms						ns
WRITE MODE								
$t_s(H)$ $t_s(L)$	Setup time High or Low A_n to $\overline{WE}$, $\overline{CS}$, CP	See Waveforms	0 0			0 0		ns
$t_h(H)$ $t_h(L)$	Hold time High or Low A_n to $\overline{WE}$, $\overline{CS}$, CP	See Waveforms	0 0			0 0		
$t_s(H)$ $t_s(L)$	Setup time High or Low D_n to $\overline{WE}$, $\overline{CS}$, CP	See Waveforms	5.0 5.0			6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time High or Low D_n to $\overline{WE}$, $\overline{CS}$, CP	See Waveforms	0 0			0 0		
t_w	$\overline{WE}$ pulse width required to write	See Waveforms	7.5			8.5		ns
t_w	$\overline{CS}$ pulse width required to write	See Waveforms	7.5			8.5		ns
t_w	CP pulse width required to write	See Waveforms	7.5			8.5		ns

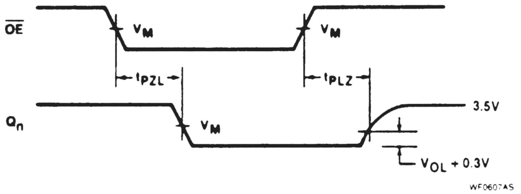
AC WAVEFORMS


CS
WE
A_n
CP
Q_n
V_M
$t_s(L)$
$t_h(L)$
$t_s(H)$
$t_h(H)$
t_{PHL}
t_{PLH}

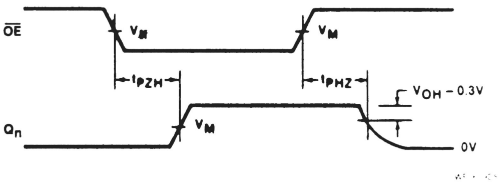
Waveform 1. Read Cycle Timing


D_n, A_n
WE, CS, CP
V_M
$t_h(L)$
$t_s(L)$
t_W
$t_s(H)$
$t_h(H)$

Waveform 2. Write Cycle Timing

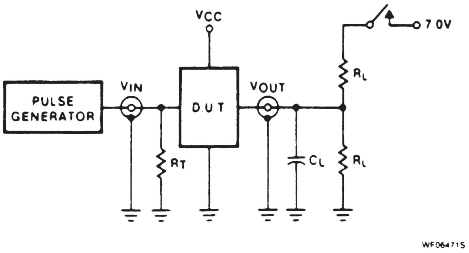

OE
Q_n
V_M
t_{PZL}
t_{PLZ}
3.5V
V_{OL} + 0.3V
WF06074S

Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

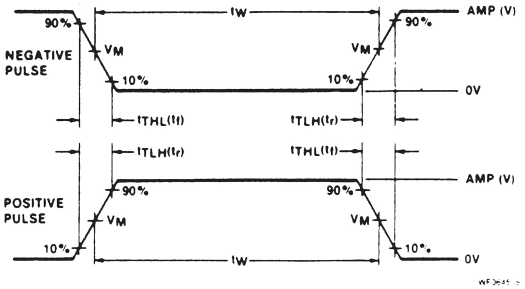

OE
Q_n
V_M
t_{PZH}
t_{PHZ}
V_{OH} - 0.3V
0V

Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tw
AMP (V)
90%
NEGATIVE PULSE
VM
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
POSITIVE PULSE
90%
VM
10%
0V
tw

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ} t_{PZL} All other	closed closed open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAST 74F547

Decoder/Demultiplexer

Octal Decoder/Demultiplexer With Address Latches And Acknowledge
Product Specification

- **3-to-8 line address decoder**
- **Address storage latches**
- **Multiple enables for address extension**
- **Open collector Acknowledge output**

DESCRIPTION

The 74F547 is a 3-to-8 line address decoder withn latches for address storage. Designed primarily to simplify multiple-chip selection in a microprocessor system, it contains one active Low and two active High Enables to conserve address space. Also included is an active Low Acknowledge output that responds to either a Read or Write input signal when the Enables are active.

For applications in which the separation of latch enable and chip enable functions is not required, LE and $\overline{E}_0$ can be tied together such that when High the outputs are OFF and the latches are transparent, and when Low the latches are storing and the selected output is enabled. The open-collector Acknowledge ($\overline{\text{ACK}}$) output is normally High (i.e.OFF) and goes Low when $\overline{E}_0$, E_1 and E_2 are all active and either the Read ($\overline{\text{RD}}$) or Write ($\overline{\text{WR}}$) input is Low, as indicated in the Acknowlege Function Table.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N74F547	8.0 ns	17mA

ORDERING INFORMATION

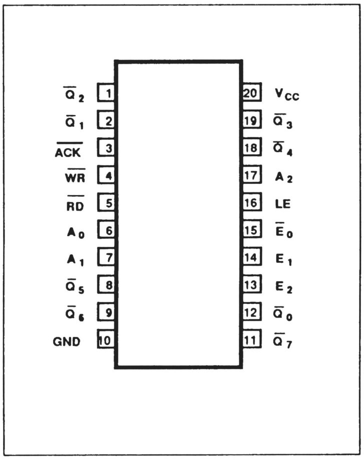
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F547N
20-Pin Plastic SOL	N74F547D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	Output select address input	1.0/1.0	20µA/0.6mA
$\overline{E}_0$	Chip enable input (active Low)	1.0/1.0	20µA/0.6mA
E_1 , E_2	Chip enable inputs	1.0/1.0	20µA/0.6mA
LE	Latch enable input	1.0/1.0	20µA/0.6mA
$\overline{\text{RD}}$	Read ackowledge input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{\text{WR}}$	Write ackowledge input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{Q}_0$-$\overline{Q}_7$	Decoder outputs (active Low)	50/33	1.0mA/20mA
$\overline{\text{ACK}}$	Open collector Acknowledge output (active Low)	OC/33	OC/20mA

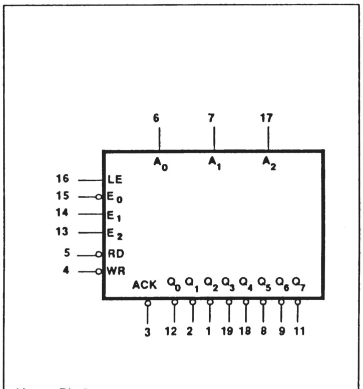
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC=Open collector

PIN CONFIGURATION



$\overline{Q}_2$ 1
$\overline{Q}_1$ 2
$\overline{\text{ACK}}$ 3
$\overline{\text{WR}}$ 4
$\overline{\text{RD}}$ 5
A_0 6
A_1 7
$\overline{Q}_5$ 8
$\overline{Q}_6$ 9
GND 10
$\overline{Q}_7$ 11
$\overline{Q}_0$ 12
E_2 13
E_1 14
$\overline{E}_0$ 15
LE 16
A_2 17
$\overline{Q}_4$ 18
$\overline{Q}_3$ 19
V_{CC} 20

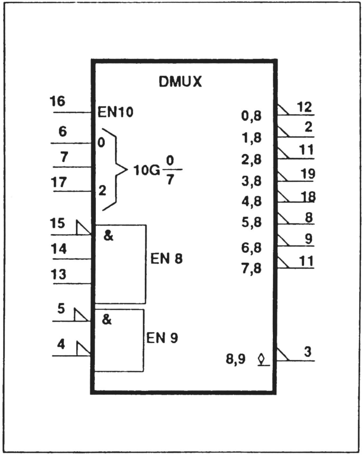
LOGIC SYMBOL



6
7
17
A_0
A_1
A_2
16 LE
15 E_0
14 E_1
13 E_2
5 RD
4 WR
ACK Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
3 12 2 1 19 18 8 9 11

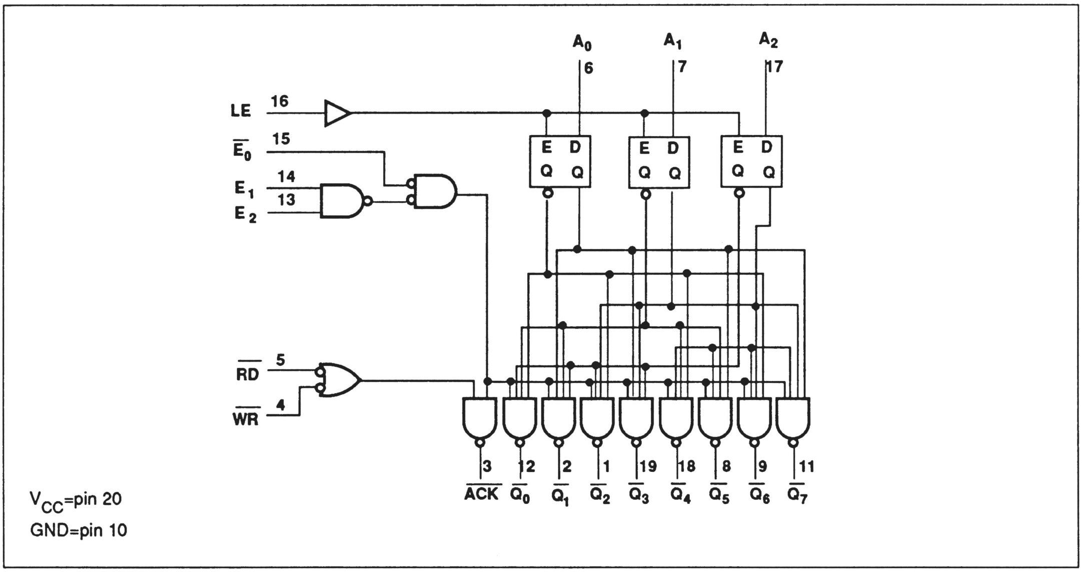
V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)



DMUX
16
EN10
6
0
7
17
2
10G $\frac{0}{7}$
15
14
13
&
EN 8
5
4
&
EN 9
0,8 12
1,8 2
2,8 11
3,8 19
4,8 18
5,8 8
6,8 9
7,8 11
8,9 3

LOGIC DIAGRAM


A0
6
A1
7
A2
17
LE
16
$\overline{E}_0$
15
E_1
14
E_2
13
E D
Q Q
$\overline{RD}$
5
$\overline{WR}$
4
3
12
2
1
19
18
8
9
11
$\overline{ACK}$
$\overline{Q}_0$
$\overline{Q}_1$
$\overline{Q}_2$
$\overline{Q}_3$
$\overline{Q}_4$
$\overline{Q}_5$
$\overline{Q}_6$
$\overline{Q}_7$

V_{CC}=pin 20
GND=pin 10

DECODER FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_0$	E_1	E_2	A_2	A_1	A_0	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$
L	H	H	L	L	L	L	H	H	H	H	H	H	H
L	H	H	L	L	H	H	L	H	H	H	H	H	H
L	H	H	L	H	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	H	L	L	H	H	H	H	L	H	H	H
L	H	H	H	L	H	H	H	H	H	H	L	H	H
L	H	H	H	H	L	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ACKNOWLEDGE FUNCTION TABLE

INPUTS					OUTPUT
$\overline{E}_0$	E_1	E_2	$\overline{RD}$	$\overline{WR}$	$\overline{ACK}$
H	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
L	H	H	H	H	H
L	H	H	L	X	L
L	H	H	X	L	L

H = High voltage level
L = Low voltage level
X = Don't care

LATCH and OUTPUT STATUS FUNCTION TABLE

INPUTS				LATCH STATUS	DECODER OUTPUTS
$\overline{E}_0$	E_1	E_2	LE		
L	H	H	H	Transparent	Address inputs decoded
L	H	H	↓	Storing	Latched address latched
L	X	X	X	Storing hold	No change
H	X	X	X	Transparent	Outputs disabled
X	L	X	X	Storing	
X	X	L	H	Transparent	

H = High voltage level
L = Low voltage level
X = Don't care
↓ = High to Low transition
A_n data must be stable one setup time before transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_K	Input clamp current				-18	mA
V_{OH}	High level output voltage	$\overline{ACK}$ only			4.5	V
I_{OH}	High-level output current	Except $\overline{ACK}$			-1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current	$\overline{ACK}$ only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OH}	High-level output voltage	Except $\overline{ACK}$	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=MAX	±10%VCC	2.5			V
					±5%VCC	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=MAX	±10%VCC		0.35	0.50	V
					±5%VCC		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Short-circuit output current[3]	Except $\overline{ACK}$	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX				17	25	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

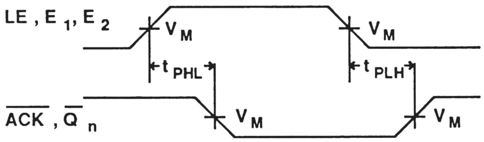
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Q}_n$	Waveform 3	2.0 4.5	4.5 7.0	9.0 12.0	1.5 4.0	10.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_0$ to $\overline{Q}_n$	Waveform 2	2.5 3.0	4.5 5.5	8.5 8.5	2.0 3.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to $\overline{Q}_n$	Waveform 1	3.5 5.0	6.0 10.5	10.0 14.0	3.0 5.0	11.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay E_1 or E_2 to $\overline{Q}_n$	Waveform 1	4.0 4.0	6.0 6.0	10.0 10.0	3.0 4.0	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_0$, $\overline{RD}$, or $\overline{WR}$ to $\overline{ACK}$	Waveform 2	6.5 3.5	9.0 5.5	13.0 9.5	6.5 3.0	14.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay E_1 or E_2 to $\overline{ACK}$	Waveform 1	7.5 4.5	11.0 6.5	14.0 10.0	7.0 4.0	15.0 11.0	ns

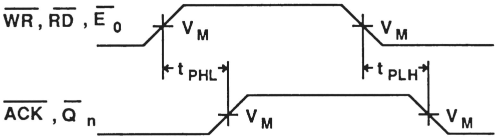
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n to LE	Waveform 4	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n to LE	Waveform 4	6.0 6.0			6.0 6.0		ns
$t_w(H)$	LE Pulse width, High	Waveform 4	6.0			6.0		ns

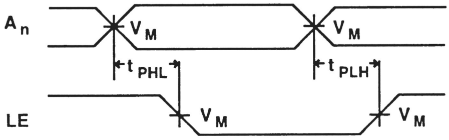
AC WAVEFORMS


LE , E 1, E 2
V M
V M
t PHL
t PLH
ACK , Q n
V M
V M

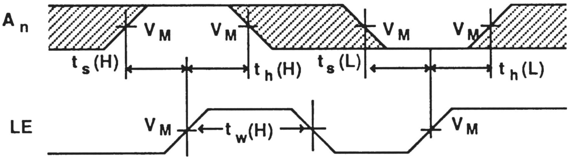
Waveform 1. Propagation Delay for Enable inputs and Latch Enable input to Acknowledge and decoder outputs


WR, RD , E 0
V M
V M
t PHL
t PLH
ACK , Q n
V M
V M

Waveform 2. Propagation Delay for Enable input to decoder outputs and Write and Read inputs to Acknowledge output


A n
V M
V M
t PHL
t PLH
LE
V M
V M

Waveform 3. Propagation Delay for output select Address input to decoder outputs

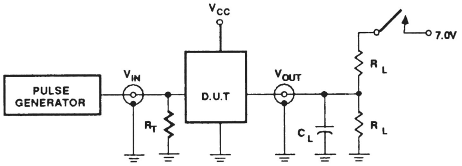

A n
V M
V M
V M
V M
t s (H)
t h (H)
t s (L)
t h (L)
LE
V M
t w(H)
V M

Waveform 4. Data Setup And Hold Times and Latch Enable pulse width

NOTE: For all waveforms, $V_M = 1.5V$.

The shaded area indicate when the input is permitted to change for predictable ouput.

TEST CIRCUIT AND WAVEFORMS


V CC
7.0V
PULSE GENERATOR
V IN
R T
D.U.T
V OUT
C L
R L
R L

Test Circuit For Open Collector Outputs

SWITCH POSITION

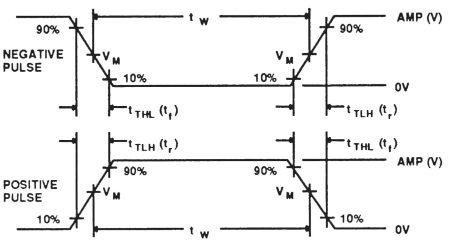
TEST	SWITCH
Open Collector	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


t w
90%
NEGATIVE PULSE
V M
10%
t THL (t f)
V M
10%
90%
AMP (V)
0V
t TLH (t r)
t TLH (t r)
t THL (t f)
AMP (V)
90%
90%
POSITIVE PULSE
V M
V M
10%
10%
0V
t w

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F552
Transceiver

Octal Registered Transceiver With Parity and Flags (3-State)

Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F552	85MHz	120mA

- **8-Bit bidirectional I/O port with handshake**
- **Register status flag flip-flops**
- **Separate clock enable and output enable**
- **Parity generation and parity check**
- **B outputs and parity output sink 64mA**

DESCRIPTION

The 74F552 Octal Registered Transceiver contains two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock (CPR, CPS) and Clock Enable ($\overline{CER}$, $\overline{CES}$) inputs, as well as a flag flip-flop that is set automatically as the register is loaded. The flag output will be reset when the Output Enable returns to High after reading the output port. Each register has a separate Output Enable ($\overline{OEAS}$, $\overline{OEBR}$) for its 3-state buffer. The separate Clocks, Flags and Enables provide considerable flexibility as I/O ports for demand-response data transfer. When data is transferred from the A port to the B port, a parity bit is generated. On the other hand, when data is transferred from the B port to the A port, the parity of input data on B_0-B_7 is checked.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP (600mil)	N74F552N
28-Pin Plastic SOL[1]	N74F552D

NOTE:

[1] Thermal mounting technique are recommended. See AN SMD-100 Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

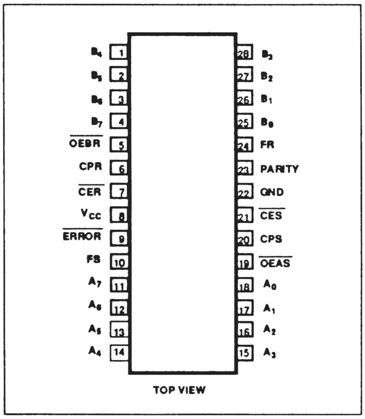
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A-to-B Data inputs	3.5/1.0	70µA/0.6mA
B_0 - B_7	B-to-A Data inputs	3.5/1.0	70µA/0.6mA
CPR	R registers clock input (active rising edge)	1.0/1.0	20µA/0.6mA
CPS	S registers clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{CER}$	R registers clock Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CES}$	S registers clock Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OEAS}$	A-to-B Output Enable input (active Low) and clear FS input (active Low)	1.0/2.0	20µA/1.2mA
$\overline{OEBR}$	B-to-A Output Enable input (active Low) and clear FS input (active Low)	1.0/2.0	20µA/1.2mA
PARITY	Parity bit transceiver input	3.5/1.0	70µA/0.6mA
	Parity bit transceiver output	750/106.7	15mA/64mA
$\overline{ERROR}$	Parity check output (active Low)	50/33.3	1.0mA/20mA
A_0 - A_7	A-to-B Data outputs	150/40	3.0mA/24mA
B_0 - B_7	B-to-A Data outputs	750/106.7	15mA/64mA
FR	A-to-B Status Flag output (active High)	50/33.3	1.0mA/20mA
FS	B-to-A Status Flag output (active High)	50/33.3	1.0mA/20mA

NOTE:

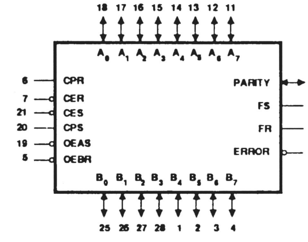
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



B4 1
B5 2
B6 3
B7 4
OEBR 5
CPR 6
CER 7
Vcc 8
ERROR 9
FS 10
A7 11
A6 12
A5 13
A4 14
28 B3
27 B2
26 B1
25 B0
24 FR
23 PARITY
22 GND
21 CES
20 CPS
19 OEAS
18 A0
17 A1
16 A2
15 A3
TOP VIEW

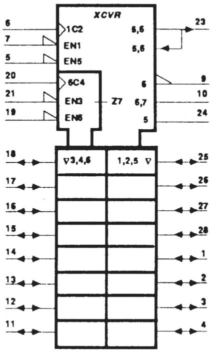
LOGIC SYMBOL



18 17 16 15 14 13 12 11
A0 A1 A2 A3 A4 A5 A6 A7
6 CPR
7 CER
21 CES
20 CPS
19 OEAS
5 OEBR
PARITY 23
FS 10
FR 24
ERROR 9
B0 B1 B2 B3 B4 B5 B6 B7
25 26 27 28 1 2 3 4

V_{CC} = Pin 8
GND = Pin 22

LOGIC SYMBOL(IEEE/IEC)



XCVR
6
7
5
20
21
19
1C2
EN1
EN5
6C4
EN3
EN6
Z7
5,6
5,6
6
6,7
5
23
9
10
24
18
17
16
15
14
13
12
11
▽3,4,6
1,2,5 ▽
25
26
27
28
1
2
3
4

FUNCTIONAL DESCRIPTION

Data applied to the A inputs are entered and stored on the rising edge of the CPR clock pulse, provided that the $\overline{\text{CER}}$ is Low; simultaneously, the status flip-flop is set and the A-to-B flag (FR) output goes High. As the $\overline{\text{CER}}$ returns to High, the data will be held in R register. This data entered from the A inputs will appear at the B port I/O pins after the $\overline{\text{OEBR}}$ has gone Low. When $\overline{\text{OEBR}}$ is Low, a parity bit appears at the PARITY pin, which will be set High when there is an even number of 1s or all 0s at the Q outputs of the R register. After the data is assimilated, the receiving system clears the flag FR, by changing the signal at the $\overline{\text{OEBR}}$ pin from Low to High. Data flow from B-to-A proceeds in the same manner described for A-to-B flow. A Low at the $\overline{\text{CES}}$ pin and a Low-to-High transition at the CPS pin enters the B input data and the parity input data into the S register and the parity register respectively and set the flag output FS to High. A Low signal at the $\overline{\text{OEAS}}$ pin enables the A port I/O pins and a Low-to-High transition of the $\overline{\text{OEAS}}$ signal clears the FS flag. When $\overline{\text{OEAS}}$ is Low, the parity check output $\overline{\text{ERROR}}$ will be High if there is an odd number of 1s at the Q outputs of the S registers and the parity register.

R or S REGISTER FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
A_n or B_n	CPX	$\overline{\text{CEX}}$	INTERNAL Q	
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	
X	$\not\uparrow$	L	NC	Keep old data

H= High voltage level
L= Low voltage level
NC=No change
X=Don't care
X=R or S for CPX and $\overline{\text{CEX}}$
↑ =Low-to-High transition
$\not\uparrow$ =Not Low-to-High transition

OUTPUT CONTROL TABLE

INPUT	OUTPUTS		OPERATING MODE
$\overline{\text{OEXX}}$	INTERNAL Q	A_n or B_n	
H	X	Z	Disable outputs
L	L	L	Enable outputs
L	H	H	

H= High voltage level
L= Low voltage level
X=Don't care
XX=AS or BR
Z =High impedance "off" state

R or S FLAG FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{\text{CEX}}$	CPX	$\overline{\text{OEXX}}$	FR or FS	
H	X	$\not\uparrow$	NC	Hold flag
L	↑	$\not\uparrow$	H	Set flag
X	X	↑	L	Clear flag

H= High voltage level
L= Low voltage level
NC=No change
X=Don't care
X=R or S for CPX and $\overline{\text{CEX}}$
XX=AS or BR
↑ =Low-to-High transition
$\not\uparrow$ =Not Low-to-High transition

PARITY GENERATION FUNCTION TABLE

INPUTS		OUTPUTS		OPERATING MODE
$\overline{\text{OEBR}}$	CPR	Number of Highs in the Q outputs of the R register	PARITY	
H	↑	X	Z	Hold data
L	↑	0,2,4,6,8	H	Load data
L	↑	1,3,5,7	L	

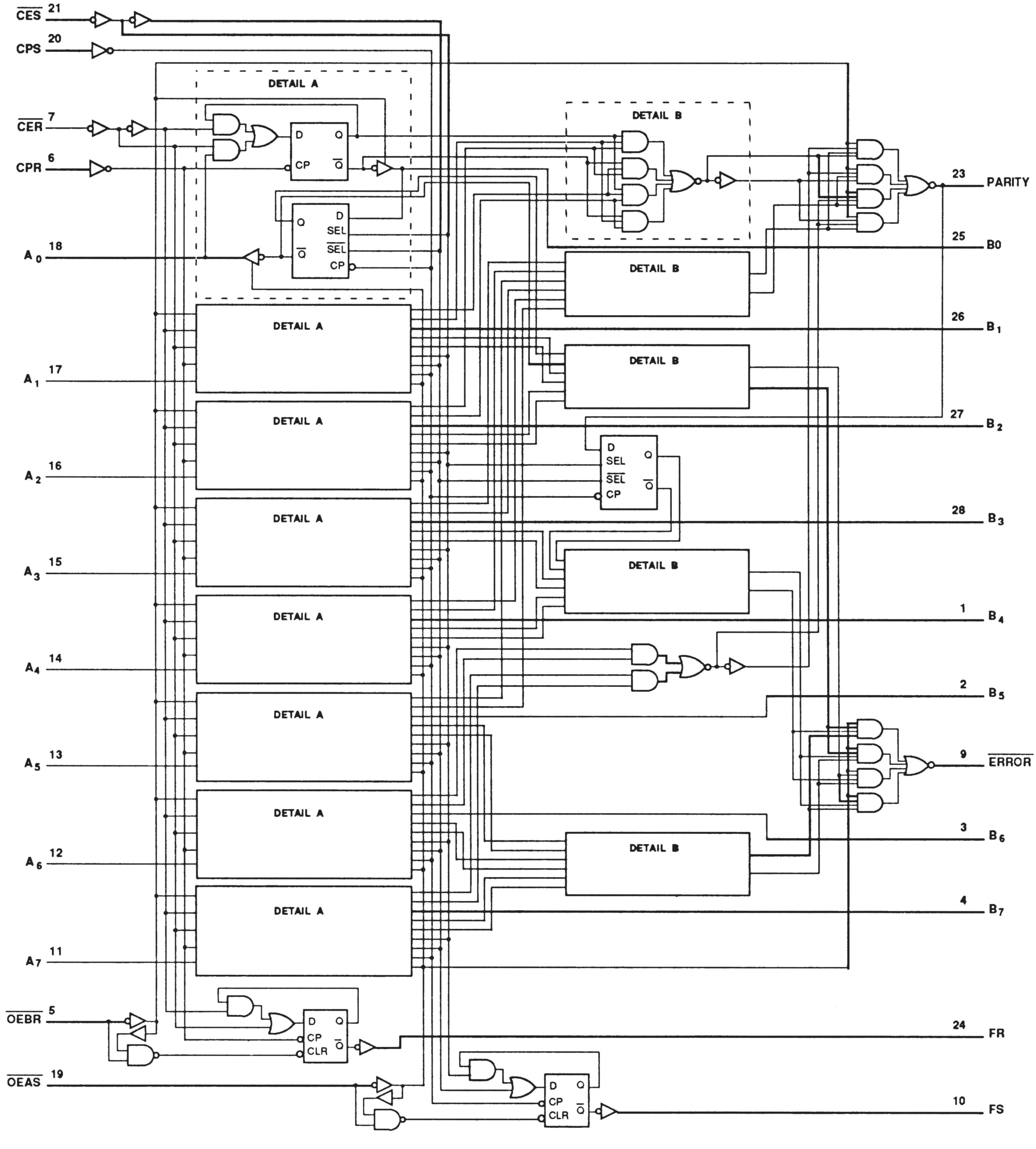
H= High voltage level
L= Low voltage level
X=Don't care
Z =High impedance "off" state
↑ =Low-to-High transition

PARITY CHECK FUNCTION TABLE

INPUTS			OUTPUTS		OPERATING MODE
$\overline{\text{OEAS}}$	CPS	PARITY	Number of Highs in the Q outputs of the R register	$\overline{\text{ERROR}}$	
H	↑	X	X	H	Parity check
L	↑	L	0,2,4,6,8	L	
L	↑	L	1,3,5,7	H	
L	↑	H	0,2,4,6,8	H	
L	↑	H	1,3,5,7	L	

H= High voltage level
L= Low voltage level
X=Don't care
↑ =Low-to-High transition

LOGIC DIAGRAM



CES 21
CPS 20
CER 7
CPR 6
A0 18
A1 17
A2 16
A3 15
A4 14
A5 13
A6 12
A7 11
OEBR 5
OEAS 19
DETAIL A
DETAIL B
D
Q
CP
SEL
CLR
23 PARITY
25 B0
26 B1
27 B2
28 B3
1 B4
2 B5
9 ERROR
3 B6
4 B7
24 FR
10 FS

V_{CC}=Pin 8
GND=Pin 22

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to $+V_{CC}$	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	FR, FS, $\overline{ERROR}$	40	mA
		A_0- A_7	48	mA
		B_0- B_7, PARITY	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	FR, FS, $\overline{ERROR}$			-1	mA
		A_0- A_7			-3	mA
		B_0- B_7, PARITY			-15	mA
I_{OL}	Low-level output current	FR, FS, $\overline{ERROR}$			20	mA
		A_0- A_7			24	mA
		B_0- B_7, PARITY			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	FR, FS, $\overline{\text{ERROR}}$	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		A_0- A_7		I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
		B_0- B_7, PARITY		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	FR, FS, $\overline{\text{ERROR}}$	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=20mA	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
		A_0- A_7		I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0- B_7, PARITY		I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = MAX, V_I = 7.0V					100	μA
		A_0- A_7, B_0- B_7, PARITY	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	others except A_0- A_7, B_0- B_7, PARITY	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	others	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		$\overline{\text{OEAS}}$, $\overline{\text{OEBA}}$						-1.2	mA
$I_{IH}+I_{OZH}$	Off-state output current High level voltage applied	A_0- A_7, B_0- B_7, PARITY	V_{CC} = MAX, V_O= 2.7V					70	μA
$I_{IL}+I_{OZL}$	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-600	μA
I_O	Output current[3]	A0-A7, FS, FR, $\overline{\text{ERROR}}$	V_{CC} = MAX, V_O= 2.25V			-20		-80	mA
		B_0-B_7, PARITY				-50		-160	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				115	170	mA
		I_{CCL}					125	185	mA
		I_{CCZ}					120	180	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

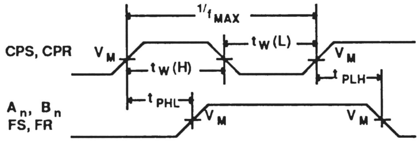
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	Waveform 1	70	85		60		MHz
t_{PLH} t_{PHL}	Propagation delay CPS to A_n or CPR to B_n	Waveform 1	3.5 4.0	5.0 6.0	8.0 9.0	3.0 3.5	8.5 9.0	ns
t_{PLH}	Propagation delay CPS to FS or CPR to FR	Waveform 1	3.0	5.0	7.5	2.5	8.5	ns
t_{PHL}	Propagation delay $\overline{\text{OEAS}}$ to FS or $\overline{\text{OEBR}}$ to FR	Waveform 2	4.0	6.0	8.5	3.5	9.0	ns
t_{PLH} t_{PHL}	Propagation delay CPS to $\overline{\text{ERROR}}$	Waveform 4	6.5 7.5	13.0 11.5	16.5 15.0	6.0 7.0	18.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay CPR to PARITY	Waveform 4	6.5 10.5	8.5 13.5	11.0 17.0	5.5 10.0	12.5 18.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{OEAS}}$ to $\overline{\text{ERROR}}$	Waveform 3	3.5 3.0	5.5 5.0	8.0 7.0	3.0 2.5	8.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{\text{OEAS}}$ to A_n or $\overline{\text{OEBR}}$ to B_n	Waveform 7 Waveform 8	2.5 4.0	4.0 6.5	7.0 9.5	2.0 4.0	8.0 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{\text{OEAS}}$ to An or $\overline{\text{OEBR}}$ to B_n	Waveform 7 Waveform 8	2.0 2.0	4.0 3.5	7.0 7.0	1.5 1.5	8.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{\text{OEBR}}$ to PARITY	Waveform 7 Waveform 8	2.0 4.0	4.0 5.5	7.0 8.0	2.0 3.0	7.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{\text{OEBR}}$ to PARITY	Waveform 7 Waveform 8	2.0 2.0	4.0 4.0	7.0 7.5	2.0 2.0	7.5 8.0	ns

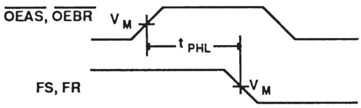
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n or PARITY to CPS or CPR	Waveform 5	7.5 4.5			8.5 5.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n or PARITY to CPS or CPR	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{\text{CES}}$ to CPS or $\overline{\text{CER}}$ to CPR	Waveform 5	7.0 7.0			7.5 7.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{\text{CES}}$ to CPS or $\overline{\text{CER}}$ to CPR	Waveform 5	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CPS or CPR Pulse width, High or Low	Waveform 1	5.0 6.5			6.5 7.5		ns
t_{rec}	Recovery time $\overline{\text{OEBR}}$ to CPR or $\overline{\text{OEAS}}$ to CPS	Waveform 6	14.5			16.5		ns

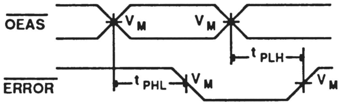
AC WAVEFORMS


1/fMAX
CPS, CPR
VM
tW(H)
tW(L)
VM
tPLH
An, Bn
FS, FR
tPHL
VM
VM

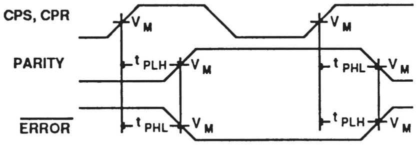
Waveform 1. Propagation Delay, Clock input to output and maximum clock frequency


OEAS, OEBR
VM
tPHL
FS, FR
VM

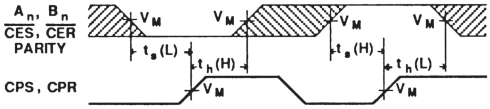
Waveform 2. Propagation Delay, Output Enable to Flag output


OEAS
VM
VM
tPLH
ERROR
tPHL
VM
VM

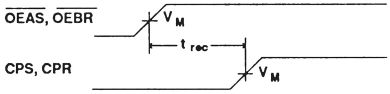
Waveform 3. Propagation Delay, Output Enable to ERROR


CPS, CPR
VM
VM
PARITY
tPLH
VM
tPHL
VM
ERROR
tPHL
VM
tPLH
VM

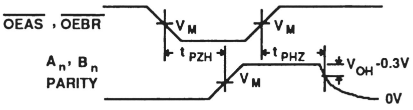
Waveform 4. Propagation Delay, Clock to PARITY and ERROR


An, Bn
CES, CER
PARITY
VM
VM
VM
VM
ts(L)
th(H)
ts(H)
th(L)
CPS, CPR
VM
VM

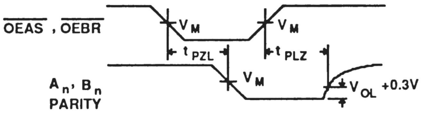
Waveform 5. Data Setup And Hold Times


OEAS, OEBR
VM
trec
CPS, CPR
VM

Waveform 6. Recovery time from Output Enable to Clock


OEAS, OEBR
VM
VM
An, Bn
PARITY
tPZH
tPHZ
VOH -0.3V
VM
0V

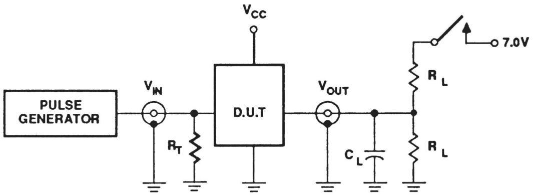
Waveform 7. 3-State Output Enable Time To High Level And Output Disable Time From High Level


OEAS, OEBR
VM
VM
tPZL
tPLZ
An, Bn
PARITY
VM
VOL +0.3V

Waveform 8. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded area indicate when the input is permitted to change for predictable output

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
RT
D.U.T
VOUT
CL
RL
RL
7.0V

Test Circuit For 3-State Outputs

SWITCH POSITION

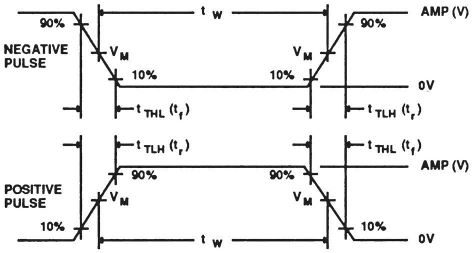
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


NEGATIVE PULSE
90%
VM
10%
tW
tTHL (tf)
tTLH (tr)
AMP (V)
0V
POSITIVE PULSE
90%
VM
10%
tTLH (tr)
tTHL (tf)
tW
AMP (V)
0V

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F563, 74F564

Latch/Flip-Flop

74F563 Octal Transparent Latch (3-State)
74F564 Octal D Flip-Flop (3-State)
Product Specification

FEATURES

- **74F563 is broadside pinout version of 74F533**
- **74F564 is broadside pinout version of 74F534**
- **Inputs and Outputs on opposite side of package allow easy interface to Microprocessors**
- **Useful as an Input or Output port for Microprocessors**
- **3-State Outputs for Bus interfacing**
- **Common Output Enable**
- **74F573 and 74F574 are non-inverting versions of 74F563 and 74F564 respectively**
- **These are High-Speed replacements for N8TS807 and N8TS808**

DESCRIPTION

The 74F563 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F563	5.0ns	55mA
74F564	4.5ns	50mA

ORDERING INFORMATION

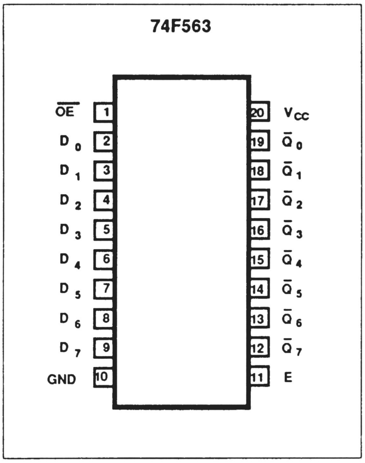
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic Slim DIP (300mil)	N74F563N, N74F564N
20-Pin Plastic SOL	N74F563D, N74F564D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

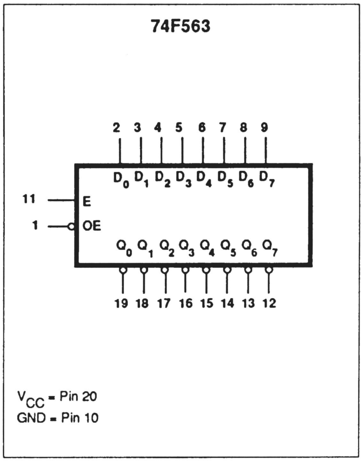
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/1.0	20µA/0.6mA
E ('F563)	Latch enable input (active High)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20µA/0.6mA
CP ('F574)	Clock Pulse input (Active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{Q}_0$ - $\overline{Q}_7$	3-State outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

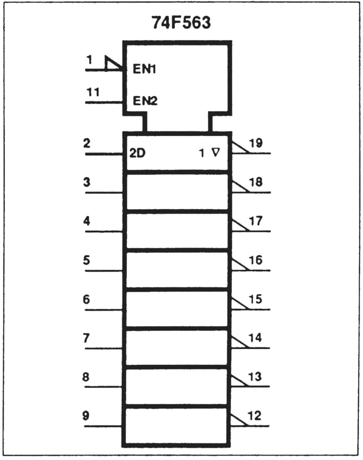

74F563
$\overline{OE}$ 1
D_0 2
D_1 3
D_2 4
D_3 5
D_4 6
D_5 7
D_6 8
D_7 9
GND 10
20 V_{CC}
19 $\overline{Q}_0$
18 $\overline{Q}_1$
17 $\overline{Q}_2$
16 $\overline{Q}_3$
15 $\overline{Q}_4$
14 $\overline{Q}_5$
13 $\overline{Q}_6$
12 $\overline{Q}_7$
11 E

LOGIC SYMBOL

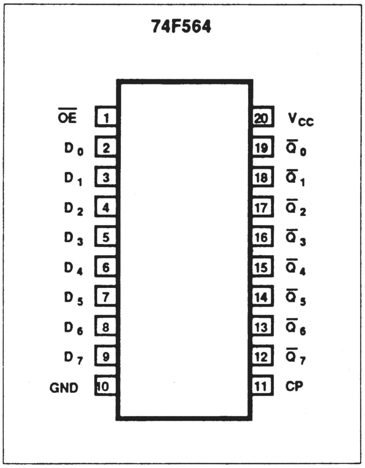

74F563
2 3 4 5 6 7 8 9
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
11 E
1 OE
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
19 18 17 16 15 14 13 12

V_{CC} = Pin 20
GND = Pin 10

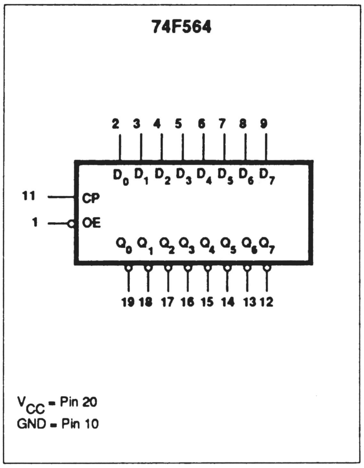
LOGIC SYMBOL(IEEE/IEC)


74F563
1 EN1
11 EN2
2 2D 1 ∇ 19
3 18
4 17
5 16
6 15
7 14
8 13
9 12

PIN CONFIGURATION

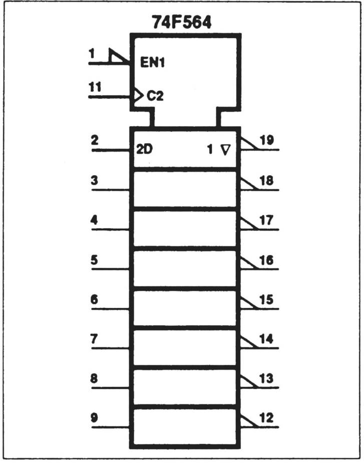

74F564
$\overline{OE}$ 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
GND 10
20 VCC
19 $\overline{Q}_0$
18 $\overline{Q}_1$
17 $\overline{Q}_2$
16 $\overline{Q}_3$
15 $\overline{Q}_4$
14 $\overline{Q}_5$
13 $\overline{Q}_6$
12 $\overline{Q}_7$
11 CP

LOGIC SYMBOL


74F564
2 3 4 5 6 7 8 9
D0 D1 D2 D3 D4 D5 D6 D7
11 CP
1 OE
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
19 18 17 16 15 14 13 12

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)


74F564
1 EN1
11 C2
2 2D 1 ▽ 19
3 18
4 17
5 16
6 15
7 14
8 13
9 12

The 74F563 is functionally identical to the 74F533 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High and stores the data that is present one set-up time before the High-to-Low enable transition.

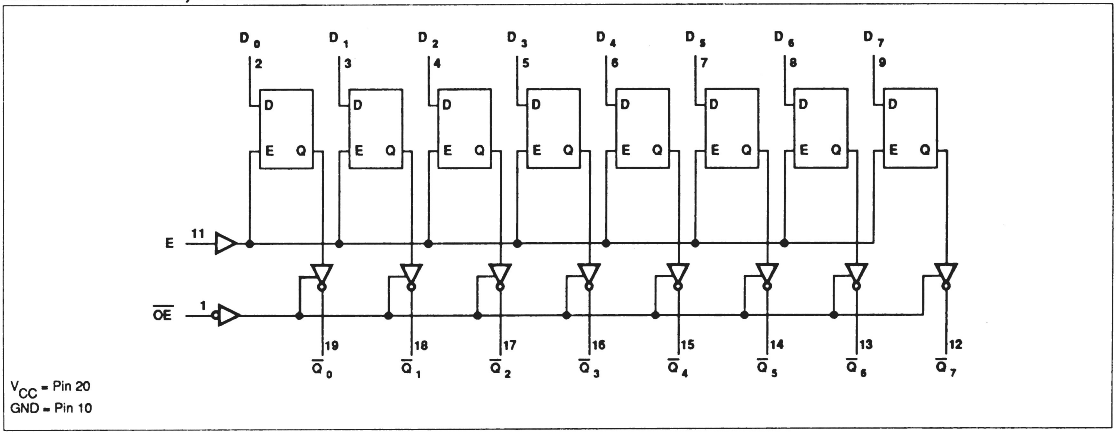
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independently of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74F564 is functionally identical to the 74F534 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

It is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates. The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's $\overline{Q}$ output.

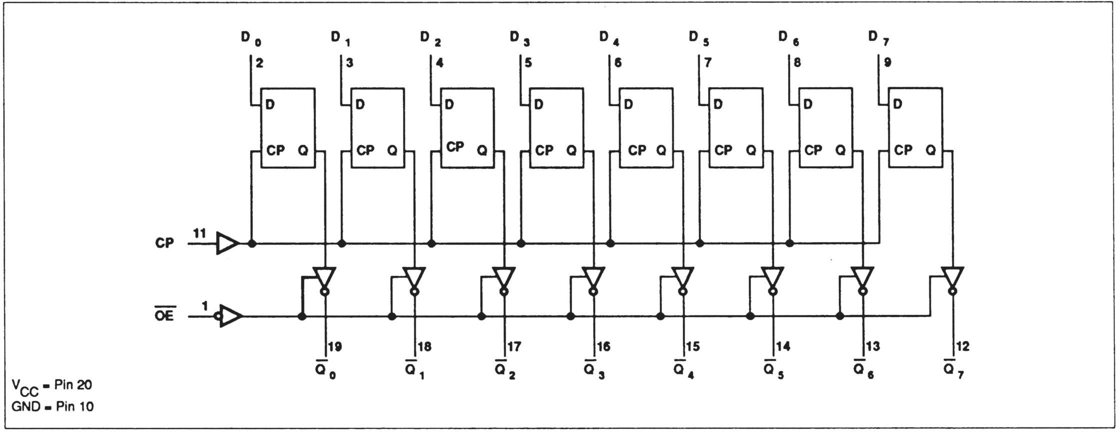
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, 74F563


D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
D E Q
E 11
$\overline{OE}$ 1
19 $\overline{Q}_0$
18 $\overline{Q}_1$
17 $\overline{Q}_2$
16 $\overline{Q}_3$
15 $\overline{Q}_4$
14 $\overline{Q}_5$
13 $\overline{Q}_6$
12 $\overline{Q}_7$

V_{CC} = Pin 20
GND = Pin 10

LOGIC DIAGRAM, 74F564



FUNCTION TABLE, 74F563

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	D_n	REGISTER	$\overline{Q}_0$ - $\overline{Q}_7$	
L L	H H	L H	L H	H L	Enable and read register
L L	↓ ↓	l h	L H	H L	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X D_n	NC D_n	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

FUNCTION TABLE, 74F564

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	D_n	REGISTER	$\overline{Q}_0$ - $\overline{Q}_7$	
L L	↑ ↑	l h	L H	H L	Load and read register
L	↟	X	NC	NC	Hold
H H	↟ ↑	X D_n	NC D_n	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↟ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
				V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
				V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input clamp current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V				50	μA
I_{OZL}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 0.5V				-50	μA
I_{OS}	Short circuit output current[3]			V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	74F563	V_{CC} = MAX			30	45	mA
		I_{CCL}					40	60	mA
		I_{CCZ}					45	65	mA
		I_{CCH}	74F564	V_{CC} = MAX			45	65	mA
		I_{CCL}					50	75	mA
		I_{CCZ}					55	80	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

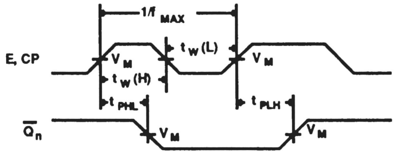
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	74F563	Waveform 2	4.0 2.5	6.5 4.5	9.0 7.0	3.5 2.0	10.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay E to $\overline{Q}_n$		Waveform 1	5.0 3.0	7.0 5.0	10.0 7.5	4.5 3.0	11.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	3.5 4.0	6.0 6.0	10.5 8.0	3.0 3.5	11.5 9.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	1.5 1.0	3.0 2.5	6.0 5.5	1.0 1.0	7.0 6.0	ns ns
f_{MAX}	Maximum Clock frequency	74F564	Waveform 1	110	125		100		ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_n$		Waveform 1	3.5 3.5	5.5 5.5	8.5 8.5	3.0 3.0	9.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	2.5 4.0	4.5 6.0	7.5 8.5	1.5 3.5	8.5 9.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	1.0 1.0	3.0 2.5	6.0 5.5	1.0 1.0	7.0 6.0	ns ns

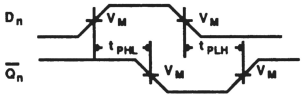
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Set-up time D_n to E	74F563	Waveform 3	1.0 1.0			1.0 1.0		ns
t_h(H) t_h(L)	Hold time D_n to E		Waveform 3	3.0 2.5			3.0 2.5		ns
t_w(H)	E Pulse width, High		Waveform 1	3.5			3.5		ns
t_s(H) t_s(L)	Set-up time D_n to CP	74F564	Waveform 3	2.0 2.0			2.0 2.0		ns
t_h(H) t_h(L)	Hold time D_n to CP		Waveform 3	2.0 2.0			2.0 2.0		ns
t_w(H) t_w(L)	CP Pulse width, High or Low		Waveform 1	4.5 4.5			4.5 4.5		ns

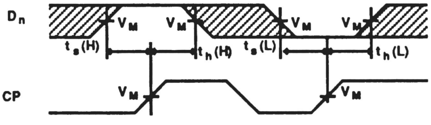
AC WAVEFORMS


1/f MAX
E, CP
V M
t w (L)
V M
t w (H)
t PHL
t PLH
Q̄n
V M
V M

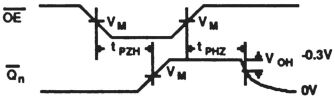
Waveform 1. Propagation Delay, Clock And Enable Inputs To Output, Enable, and Clock Pulse Widths, and Maximum Clock Frequency


Dn
V M
V M
t PHL
t PLH
Q̄n
V M
V M

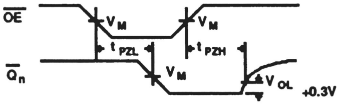
Waveform 2. Propagation Delay For Data To Outputs


Dn
V M
V M
V M
V M
t s (H)
t h (H)
t s (L)
t h (L)
E, CP
V M
V M

Waveform 3. Data Setup And Hold Times


OE
V M
V M
t PZH
t PHZ
V OH -0.3V
Q̄n
V M
0V

Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level

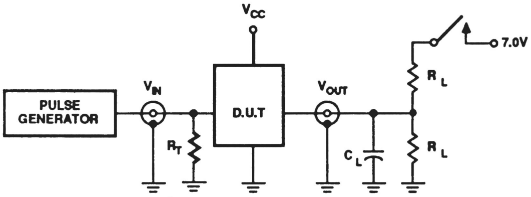

OE
V M
V M
t PZL
t PZH
Q̄n
V M
V OL +0.3V

Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

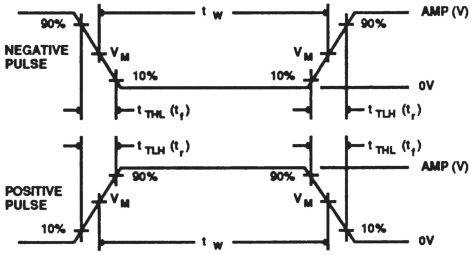
NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V CC
7.0V
R L
PULSE GENERATOR
V IN
R T
D.U.T
V OUT
C L
R L

Test Circuit For 3-State Outputs


t w
AMP (V)
90%
90%
NEGATIVE PULSE
V M
V M
10%
10%
0V
t THL (t f)
t TLH (t r)
t TLH (t r)
t THL (t f)
AMP (V)
90%
90%
POSITIVE PULSE
V M
V M
10%
10%
0V
t w

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F573, 74F574

Latch/Flip-Flops

74F573 Octal Transparent Latch (3-State)
74F574 Octal D Flip-Flop (3-State)
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F573	5.0ns	35mA
74F574	4.5ns	50mA

FEATURES

- **74F573 is broadside pinout version of 74F373**
- **74F574 is broadside pinout version of 74F374**
- **Inputs and Outputs on opposite side of package allow easy interface to Microprocessors**
- **Useful as an Input or Output port for Microprocessors**
- **3-State Outputs for Bus interfacing**
- **Common Output Enable**
- **74F563 and 74F564 are inverting version of 74F573 and 74F574 respectively**
- **These are High-Speed replacements for N8TS805 and N8TS806**

DESCRIPTION

The 74F573 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

ORDERING INFORMATION

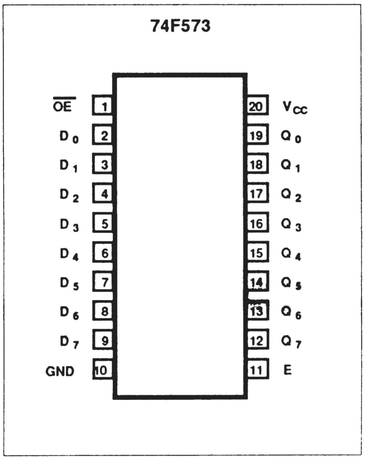
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F573N, N74F574N
20-Pin Plastic SOL	N74F573D, N74F574D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

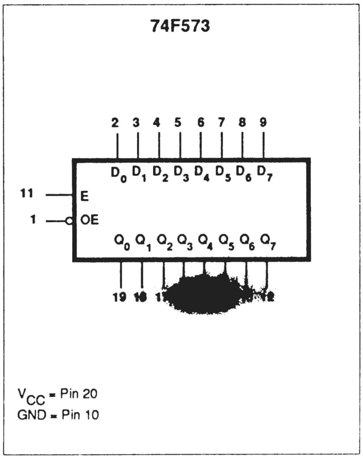
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/1.0	20μA/0.6mA
E ('F573)	Latch enable input (active High)	1.0/1.0	20 A/0.6mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20μA/0.6mA
CP ('F574)	Clock Pulse input (Active rising edge)	1.0/1.0	20 A/0.6mA
Q_0 - Q_7	3-State outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

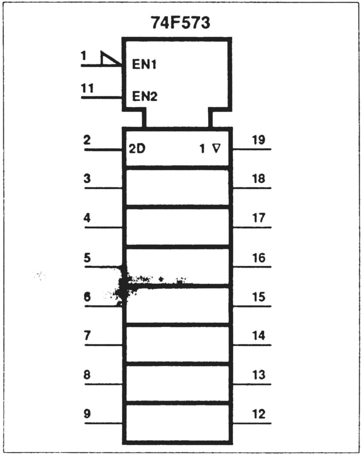

74F573
OE 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
GND 10
20 Vcc
19 Q0
18 Q1
17 Q2
16 Q3
15 Q4
14 Q5
13 Q6
12 Q7
11 E

LOGIC SYMBOL

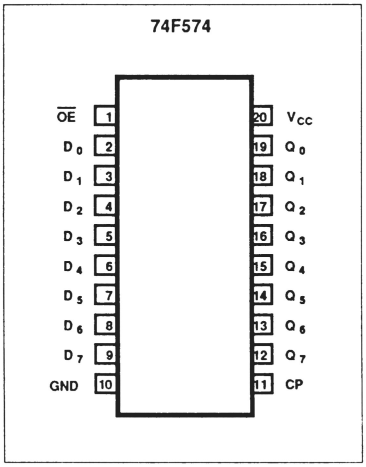

74F573
2 3 4 5 6 7 8 9
D0 D1 D2 D3 D4 D5 D6 D7
11 E
1 OE
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
19 18 1
12

V_{CC} = Pin 20
GND = Pin 10

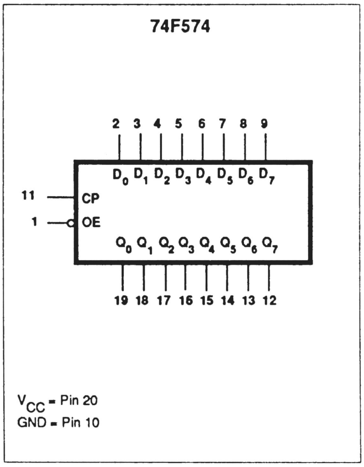
LOGIC SYMBOL(IEEE/IEC)


74F573
1
EN1
11
EN2
2
2D
1 ∇
19
3
18
4
17
5
16
6
15
7
14
8
13
9
12

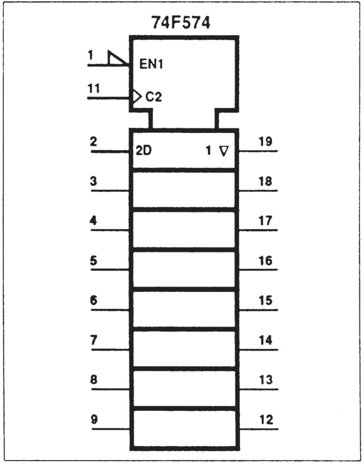
PIN CONFIGURATION


74F574
$\overline{OE}$ 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
GND 10
20 Vcc
19 Q0
18 Q1
17 Q2
16 Q3
15 Q4
14 Q5
13 Q6
12 Q7
11 CP

LOGIC SYMBOL


74F574
2 3 4 5 6 7 8 9
D0 D1 D2 D3 D4 D5 D6 D7
11 CP
1 OE
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
19 18 17 16 15 14 13 12
VCC = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)


74F574
1
EN1
11
C2
2
2D
1 ∇
19
3
18
4
17
5
16
6
15
7
14
8
13
9
12

The 74F573 is functionally identical to the 74F373 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High and stores the data that is present one set-up time before the High-to-Low enable transition.

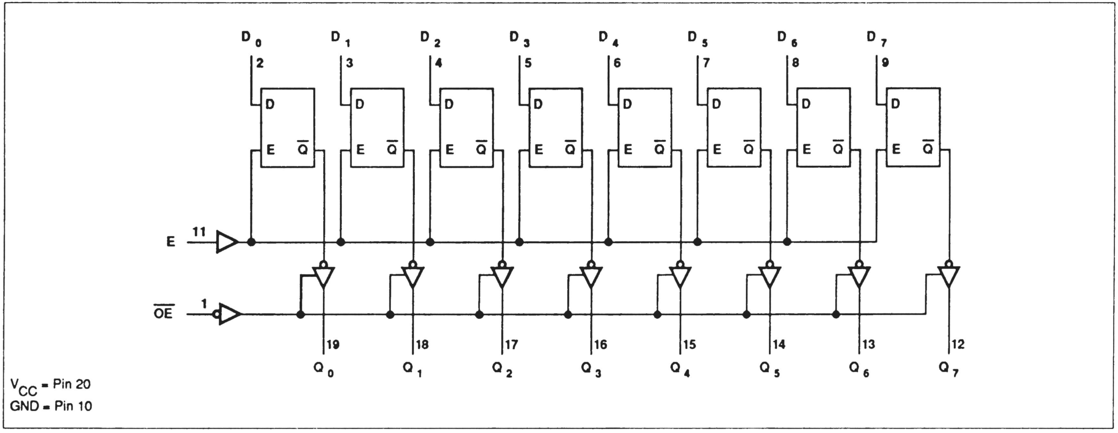
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74F574 is functionally identical to the 74F374 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

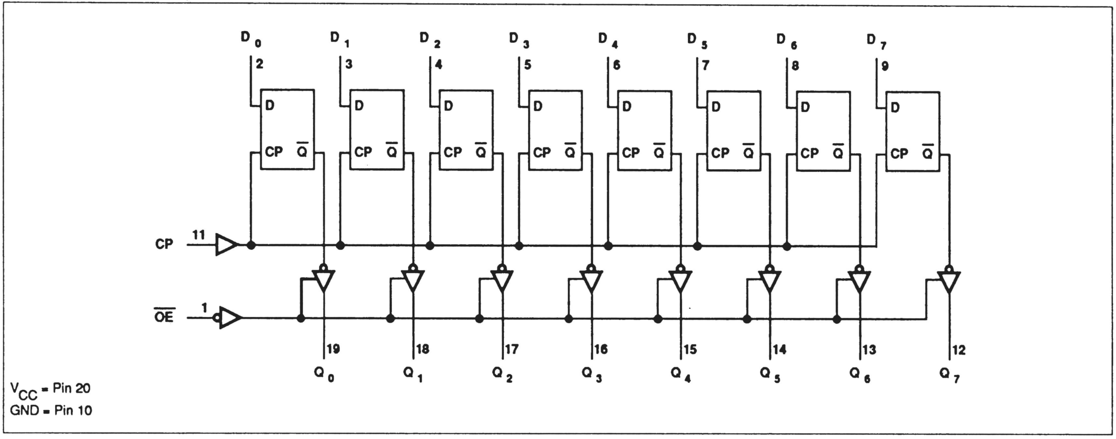
It is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates. The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, 74F573


D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
D
E
$\overline{Q}$
E 11
$\overline{OE}$ 1
19 Q0
18 Q1
17 Q2
16 Q3
15 Q4
14 Q5
13 Q6
12 Q7
VCC = Pin 20
GND = Pin 10

LOGIC DIAGRAM, 74F574



V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE, 74F573

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	D_n	REGISTER	Q_0 - Q_7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X D_n	NC D_n	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

FUNCTION TABLE, 74F574

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	D_n	REGISTER	Q_0 - Q_7	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↑̄	X	NC	NC	Hold
H H	↑ X	D_n X	D_n X	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↑̄ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
				V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
				V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input clamp current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V				50	μA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V				-50	μA
I_{OS}	Short circuit output current[3]			V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	74F573	V_{CC} = MAX			30	40	mA
		I_{CCL}					35	50	mA
		I_{CCZ}					40	60	mA
		I_{CCH}	74F574	V_{CC} = MAX			45	65	mA
		I_{CCL}					50	70	mA
		I_{CCZ}					55	90	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

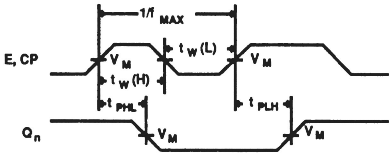
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F573	Waveform 2	3.0 1.0	5.5 3.5	8.0 6.0	2.5 1.0	9.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n		Waveform 1	4.5 3.0	8.5 5.0	11.5 7.0	4.0 2.5	12.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	2.5 2.5	5.5 5.5	9.5 8.0	2.0 2.0	10.5 8.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	1.0 1.0	3.0 2.5	6.0 5.5	1.0 1.0	6.5 5.5	ns ns
f_{MAX}	Maximum Clock frequency	74F574	Waveform 1	110	125		100		ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	4.0 4.0	5.5 6.0	8.5 8.5	3.0 3.0	9.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	2.5 3.0	4.5 6.0	8.0 8.5	2.0 3.0	8.0 9.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	1.0 1.0	3.0 2.5	6.0 5.5	1.0 1.0	7.0 6.0	ns ns

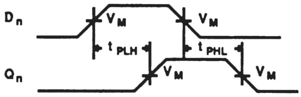
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Set-up time D_n to E	74F573	Waveform 3	0.0 0.0			0.0 0.0		ns
t_h(H) t_h(L)	Hold time D_n to E		Waveform 3	2.5 4.0			2.5 4.0		ns
t_w(H) t_w(L)	E Pulse width, High or Low		Waveform 1	4.0 4.0			4.0 4.0		ns
t_s(H) t_s(L)	Set-up time D_n to CP	74F574	Waveform 3	2.0 2.0			2.0 2.0		ns
t_h(H) t_h(L)	Hold time D_n to CP		Waveform 3	1.5 1.5			1.5 1.5		ns
t_w(H) t_w(L)	CP Pulse width, High or Low		Waveform 1	3.0 4.5			3.0 4.5		ns

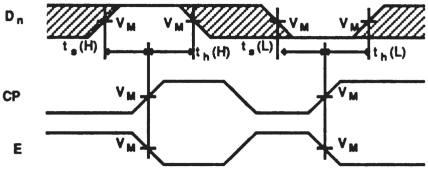
AC WAVEFORMS


1/f MAX
E, CP
V M
t w (L)
t w (H)
t PHL
t PLH
Q n
V M

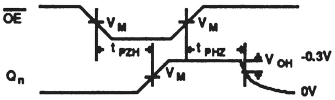
Waveform 1. Propagation Delay, Clock And Enable Inputs To Output, Enable, and Clock Pulse Widths, and Maximum Clock Frequency


D n
V M
t PLH
t PHL
Q n
V M

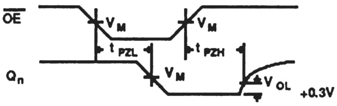
Waveform 2. Propagation Delay For Data To Outputs


D n
V M
t s (H)
t h (H)
t s (L)
t h (L)
CP
E
V M

Waveform 3. Data Setup And Hold Times


OE
V M
t PZH
t PHZ
V OH -0.3V
Q n
0V

Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level

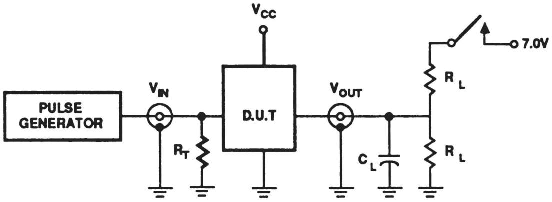

OE
V M
t PZL
t PZH
Q n
V OL
+0.3V

Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

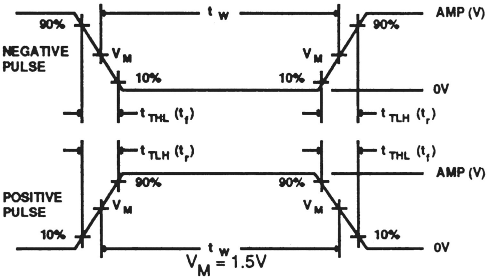
NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V CC
7.0V
R L
V IN
V OUT
PULSE GENERATOR
D.U.T
R T
C L
R L

Test Circuit For 3-State Outputs


t w
AMP (V)
90%
NEGATIVE PULSE
V M
10%
0V
t THL (t f)
t TLH (t r)
POSITIVE PULSE
V M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F595

Shift Register

8-Bit Shift Register with Output Latches (3-state)
Product Specification

FEATURES

- High impedance NPN base input for reduced loading (20µA in High and Low states)
- 8-bit serial-in, serial-out shift register with storage
- 3-state outputs
- Shift register has direct clear
- Guaranteed shift frequency-DC to 120MHz

DESCRIPTION

The 74F595 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs.Separate clocks are provided for both the shift register and the storage register. The shift register and storage register clocks are positive edge-triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F595	120MHz	75mA

ORDERING INFORMATION

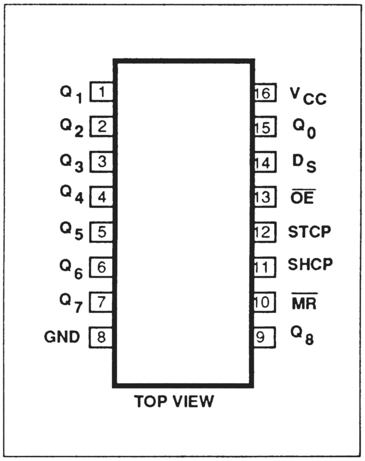
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic Slim DIP (300mil)	N74F595N
16-Pin Plastic SO	N74F595D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_S	Serial data input	1.0/0.033	20µA/20µA
SHCP	Shift register clock pulse input	1.0/0.033	20µA/20µA
$\overline{\text{STCP}}$	Storage register clock pulse input	1.0/0.033	20µA/20µA
$\overline{\text{MR}}$	Master reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{\text{OE}}$	Output enable input (active Low)	1.0/1.0	20µA/0.6mA
Q_8	Serial expansion output	50/33	1.0mA/20mA
Q_0 - Q_7	Data outputs	150/40	3.0mA/24mA

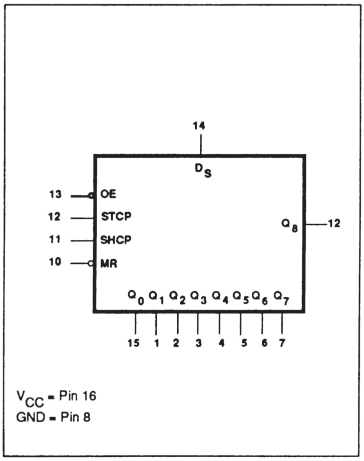
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



Q1 1
Q2 2
Q3 3
Q4 4
Q5 5
Q6 6
Q7 7
GND 8
16 VCC
15 Q0
14 DS
13 OE
12 STCP
11 SHCP
10 MR
9 Q8
TOP VIEW

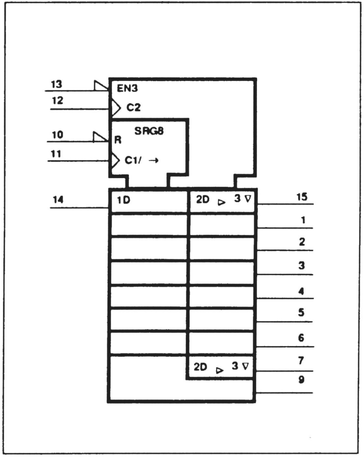
LOGIC SYMBOL



14
DS
13 OE
12 STCP
11 SHCP
10 MR
Q8 12
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
15 1 2 3 4 5 6 7

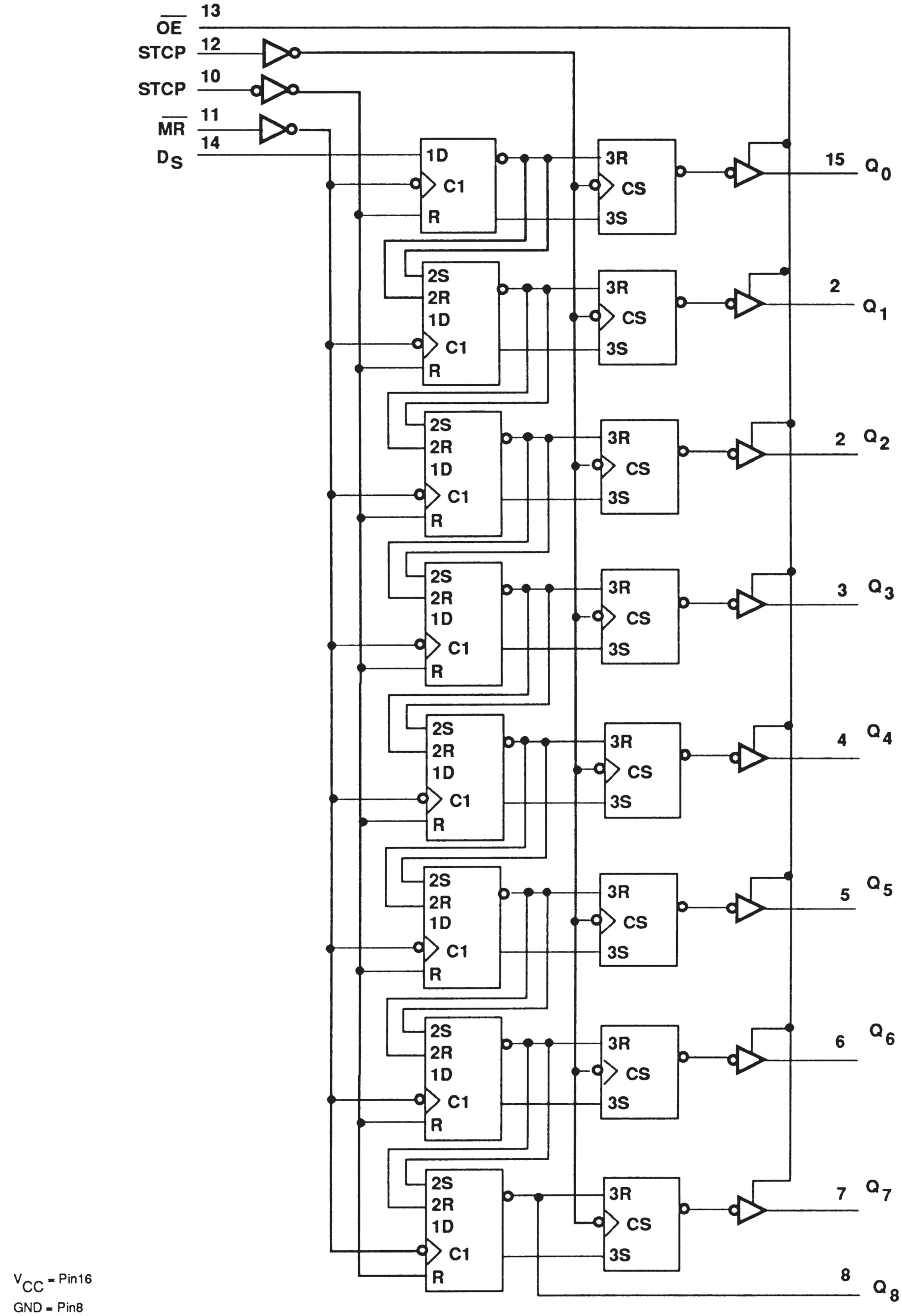
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



13
EN3
12
C2
10
R
SRG8
11
C1/ →
14
1D
2D ▷ 3∇
15
1
2
3
4
5
6
2D ▷ 3∇
7
9

LOGIC DIAGRAM


OE
13
STCP
12
STCP
10
MR
11
DS
14
1D
C1
R
2S
2R
3R
CS
3S
15
Q0
2
Q1
Q2
3
Q3
4
Q4
5
Q5
6
Q6
7
Q7
8
Q8
VCC = Pin16
GND = Pin8

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	Q_8	40	mA
		Q_0- Q_7	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_8			-1	mA
		Q_0- Q_7			-3	mA
I_{OL}	Low-level output current	Q_8			20	mA
		Q_0- Q_7			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	Q_8	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		Q_0- Q_7		I_{OH}=-3mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	μA
		Q_0- Q_7	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	others	V_{CC} = MAX, V_I = 0.5V					-20	μA
		$\overline{MR}$, $\overline{OE}$						-0.6	mA
I_{OZH}	Off-state output current High-level voltage applied	Q_0- Q_7 only	V_{CC} = MAX, V_O= 2.7V					50	μA
I_{OZL}	Off-state output current Low-level voltage applied	Q_0- Q_7 only	V_{CC} = MAX, V_O= 0.5V					-50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				60	75	mA
		I_{CCL}					70	85	mA
		I_{CCZ}					80	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

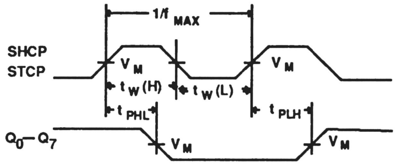
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		80		MHz
t_{PLH} t_{PHL}	Propagation delay SHCP to Q_8	Waveform 1	4.0 4.0	6.5 7.0	8.5 9.0	4.0 4.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay STCP to Q_0- Q_7	Waveform 1	4.0 4.0	6.5 7.0	9.0 9.0	4.0 4.0	9.5 10.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_8	Waveform 2	4.0	7.0	9.0	4.0	10.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 5 Waveform 6	2.0 2.0	6.5 5.5	8.0 7.0	2.0 2.0	9.5 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 5 Waveform 6	2.0 2.0	6.5 5.5	7.0 7.0	2.0 2.0	9.5 8.0	ns

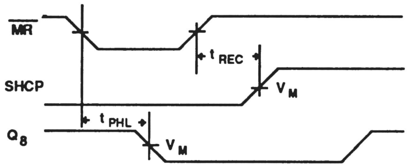
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_S to SHCP	Waveform 3	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_S to SHCP	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_s(L)$	Setup time, Low $\overline{MR}$ to STCP	Waveform 3	5.0			5.0		ns
$t_h(H)$	Setup time, High SHCP to STCP	Waveform 4	6.0			6.0		ns
$t_w(H)$ $t_w(L)$	SHCP Pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(H)$ $t_w(L)$	$\overline{STCP}$ Pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to SHCP	Waveform 2	6.0			7.0		ns

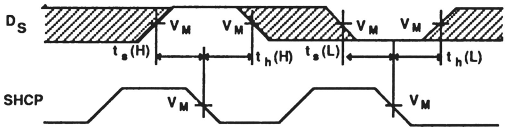
AC WAVEFORMS


1/f MAX
SHCP
STCP
V M
t W (H)
t W (L)
t PHL
t PLH
Q0—Q7
V M

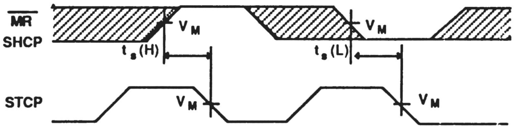
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency


MR
t REC
SHCP
V M
Q8
t PHL
V M

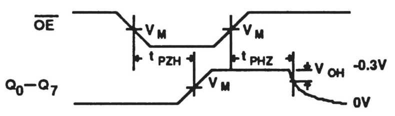
**Waveform 2.
Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time**


DS
V M
t s (H)
t h (H)
t s (L)
t h (L)
SHCP
V M

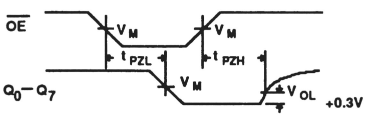
Waveform 3. Data Setup And Hold Times


MR
SHCP
V M
t s (H)
t s (L)
STCP
V M

Waveform 4. Data Setup And Hold Times


OE
V M
t PZH
t PHZ
V OH
-0.3V
Q0—Q7
V M
0V

Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level

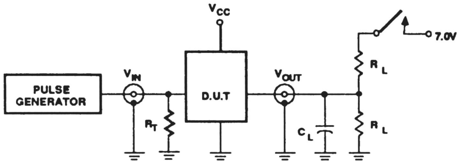

OE
V M
t PZL
t PZH
Q0—Q7
V M
V OL
+0.3V

Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
PULSE GENERATOR
VIN
RT
D.U.T
VOUT
CL
RL
RL

Test Circuit For 3-State Outputs

SWITCH POSITION

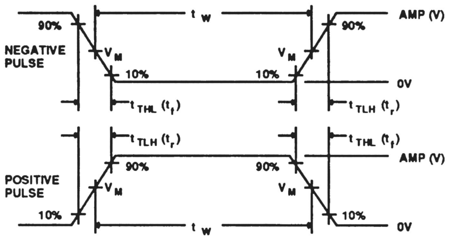
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


t W
AMP (V)
90%
NEGATIVE PULSE
V M
10%
0V
t THL (t f)
t TLH (t r)
POSITIVE PULSE
90%
AMP (V)
V M
10%
0V
t W

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F646, 74F646A
74F648, 74F648A
Transceivers/Registers

74F646/646A Octal Transceiver/Register, Non-Inverting (3-State)
74F648/648A Octal Transceivers/Register, Inverting (3-State)
Preliminary Specification for 74F646A and 74F648A
Product Specification for 74F646 and 74F648

FEATURES

- **Combines 'F245 and 'F374 type functions in one chip**
- **High impedance base inputs for reduced loading (70μA in High and Low states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **Controlled ramp outputs for 'F646A/'F648A**
- **3-state outputs**
- **300 mil wide 24-pin Slim Dip package**

DESCRIPTION

The 74F646/646A and 74F648/648A Transceivers/Registers consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will clocked into the registers as the appropriate clock pin goes High. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F646/648	115MHz	140mA
74F646A/648A	115MHz	120mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F646N, N74F646AN, N74F648N, N74F648AN
24-Pin Plastic SOL[1]	N74F646D, N74F646AD, N74F648D, N74F648AD

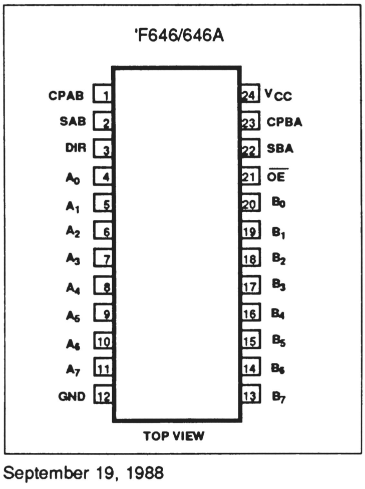
NOTE 1: Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

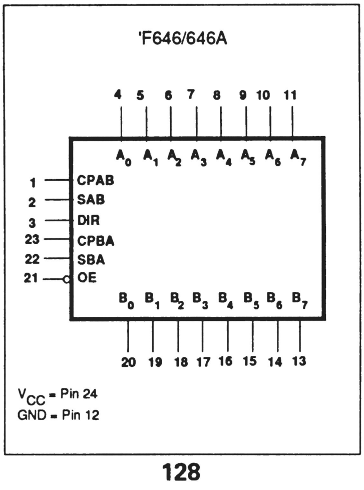
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7, B_0 - B_7	A and B inputs for 'F646/'F648	3.5/0.166	70μA/70μA
A_0 - A_7, B_0 - B_7	A and B inputs for 'F646A/'F648A	1.0/0.033	20μA/20μA
CPAB	A-to-B clock input	1.0/0.033	20μA/20μA
CPBA	B-to-A clock input	1.0/0.033	20μA/20μA
SAB	A-to-B select input	1.0/0.033	20μA/20μA
SBA	B-to-A select input	1.0/0.033	20μA/20μA
DIR	Data flow Directional control Enable input	1.0/0.033	20μA/20μA
$\overline{OE}$	Output enable input	1.0/0.033	20μA/20μA
A_0 - A_7	A outputs	750/106.7	15mA/64mA
B_0 - B_7	B outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

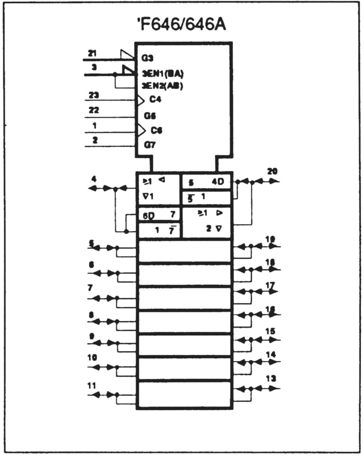
PIN CONFIGURATION


'F646/646A
CPAB 1
SAB 2
DIR 3
A0 4
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
GND 12
24 VCC
23 CPBA
22 SBA
21 OE
20 B0
19 B1
18 B2
17 B3
16 B4
15 B5
14 B6
13 B7
TOP VIEW

LOGIC SYMBOL


'F646/646A
4 5 6 7 8 9 10 11
A0 A1 A2 A3 A4 A5 A6 A7
1 CPAB
2 SAB
3 DIR
23 CPBA
22 SBA
21 OE
B0 B1 B2 B3 B4 B5 B6 B7
20 19 18 17 16 15 14 13
VCC = Pin 24
GND = Pin 12

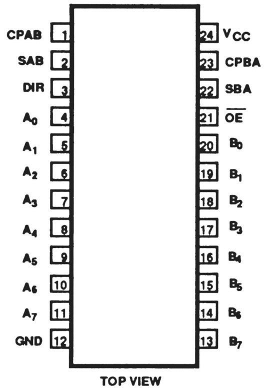
LOGIC SYMBOL(IEEE/IEC)


'F646/646A
21
3
23
22
1
2
G3
3EN1(BA)
3EN2(AB)
C4
G5
C6
G7
≥1
▽1
5 4D
5̄ 1
6D 7
1 7̄
≥1
2 ▽
4 5 6 7 8 9 10 11
20 19 18 17 16 15 14 13

FAST 74F646, 74F646A, 74F648, 74F648A

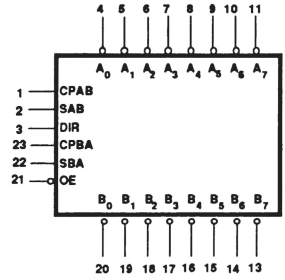
PIN CONFIGURATION

'F648/648A


CPAB 1
SAB 2
DIR 3
A0 4
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
GND 12
24 VCC
23 CPBA
22 SBA
21 OE
20 B0
19 B1
18 B2
17 B3
16 B4
15 B5
14 B6
13 B7
TOP VIEW

LOGIC SYMBOL

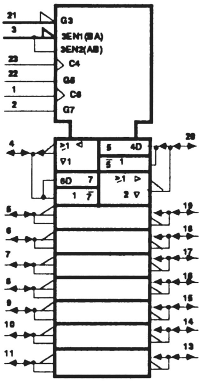
'F648/648A


4 5 6 7 8 9 10 11
A0 A1 A2 A3 A4 A5 A6 A7
1 CPAB
2 SAB
3 DIR
23 CPBA
22 SBA
21 OE
B0 B1 B2 B3 B4 B5 B6 B7
20 19 18 17 16 15 14 13

V_{CC} = Pin 24
GND = Pin 12

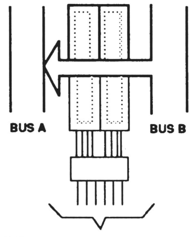
LOGIC SYMBOL(IEEE/IEC)

'F648/648A


21
3
23
22
1
2
G3
3EN1(BA)
3EN2(AB)
C4
G5
C6
G7
≥1 ◁
∇1
5 4D
5̄ 1
6D 7
1 7̄
≥1 ▷
2 ∇
4
5
6
7
8
9
10
11
20
19
18
17
16
15
14
13

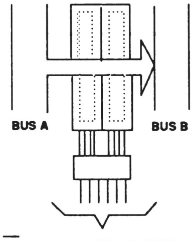
The select (SAB, SBA) pins determine whether data is stored or transfered through the device in real-time.The DIR determines which bus will receive data when the $\overline{OE}$ is active Low. In the isolation mode ($\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two busses , A or B may be driven at a time. The following examples demonstrates the four fundamental bus-management functions that can be performed with the 'F646/646A and 'F648/648A.

REAL TIME BUS TRANSFER
BUS B TO BUS A



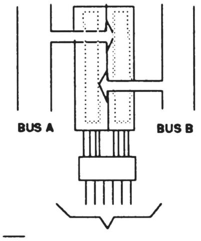
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER
BUS A TO BUS B



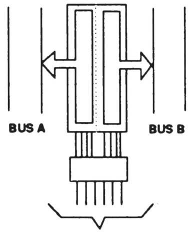
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	H	X	X	L	X

STORAGE FROM
A, B, OR A AND B



$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
X	H	1	X	X	X
X	X	X	1	X	X
H	X	1	1	X	X

TRANSFER STORED DATA
TO A OR B



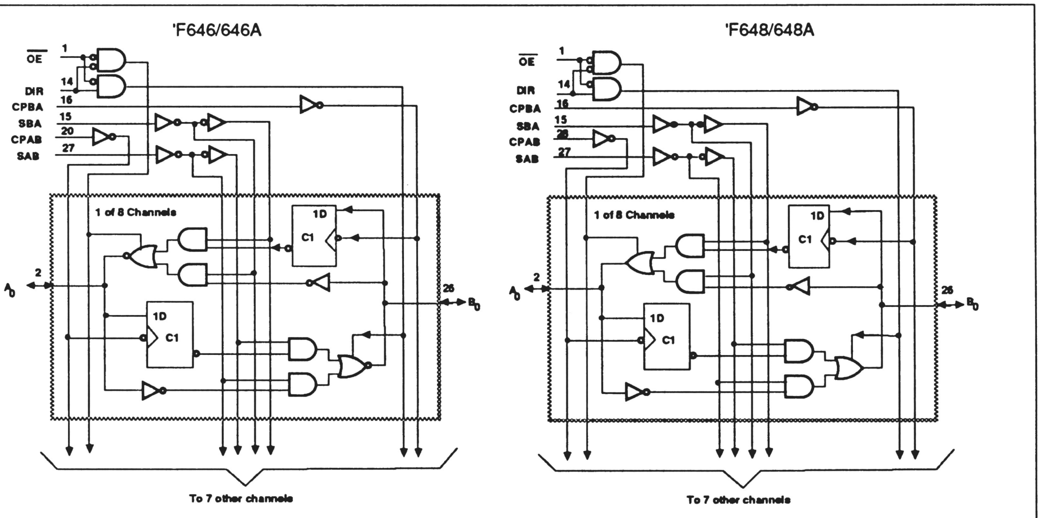
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	A_0-A_7	B_0-B_7	'F646/646A	'F648/648A
X	X	↑	X	X	X	input*	Unspecified	Store A, B unspecified*	Store A, B unspecified*
X	X	X	↑	X	X	Unspecified	Input*	Store B, A unspecified*	Store B, A unspecified*
H	X	↑	↑	X	X	Input	Input	Store A and B data	Store A and B data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real time B data to A bus	Real time $\overline{B}$ data to A bus
L	L	X	H or L	X	H			Store B data to A bus	Store $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real time A data to B bus	Real time $\overline{A}$ data to B bus
L	H	H or L	X	H	X			Store A data to B bus	Store $\overline{A}$ data to B bus

H= High voltage level
L= Low voltage level
X=Don't care
↑ =Low-to-High clock transition
*= The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enable, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

LOGIC DIAGRAM


'F646/646A
$\overline{OE}$
DIR
CPBA
SBA
CPAB
SAB
1
14
16
15
20
27
1 of 8 Channels
1D
C1
1D
C1
A_0
2
26
B_0
To 7 other channels
'F648/648A
$\overline{OE}$
DIR
CPBA
SBA
CPAB
SAB
1
14
16
15
20
27
1 of 8 Channels
1D
C1
1D
C1
A_0
2
26
B_0
To 7 other channels

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
					I_{OH}=-15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
					I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others		V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7		V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	$\overline{OE}$,DIR, CPAB, CPBA SAB, SBA		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-20	µA
$I_{IH}+I_{OZH}$	Off-state output current High level voltage applied	A_0-A_7, B_0-B_7		V_{CC} = MAX, V_O= 2.7V					70	µA
$I_{IL}+I_{OZL}$	Off-state output current Low level voltage applied			V_{CC} = MAX, V_O = 0.5V					-70	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F646 'F648	I_{CCH}	V_{CC} = MAX				125	165	mA
			I_{CCL}					160	210	mA
			I_{CCZ}					135	160	mA
		'F646A 'F648A	I_{CCH}					110	145	mA
			I_{CCL}					120	155	mA
			I_{CCZ}					130	170	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for 74F646

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.5 5.5	7.5 8.0	10.0 10.0	5.0 5.0	11.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 2,3	4.0 4.0	6.0 6.5	9.0 9.0	4.0 4.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2,3	5.0 5.0	7.0 6.5	8.5 8.5	4.5 4.5	10.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	5.0 6.5	7.0 8.5	10.0 11.0	4.5 6.0	11.0 12.5	ns
t_{PZH} t_{PZL}	Output Enable time DIR to A_n or B_n	Waveform 5 Waveform 6	4.5 6.0	6.5 8.5	9.0 11.0	4.0 5.5	10.0 12.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	6.5 6.5	9.0 9.0	11.5 11.5	6.0 6.0	12.5 13.5	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to A_n or B_n	Waveform 5 Waveform 6	5.5 5.5	8.5 8.5	11.0 11.0	4.5 5.0	13.0 12.5	ns

AC SETUP REQUIREMENTS for 74F646

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.0 6.0			4.0 6.0		ns

AC ELECTRICAL CHARACTERISTICS for 74F648

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.5 5.5	7.5 7.5	9.5 9.5	4.5 4.5	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 2,3	3.0 4.0	6.0 6.0	8.5 8.5	2.5 3.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2,3	4.5 4.5	7.0 6.5	8.5 8.5	4.5 4.5	10.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	4.5 6.0	7.0 8.5	10.0 11.0	4.5 5.5	11.0 12.5	ns
t_{PZH} t_{PZL}	Output Enable time DIR to A_n or B_n	Waveform 5 Waveform 6	4.5 6.0	7.0 8.5	10.0 11.0	4.0 5.5	11.0 12.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	6.0 6.0	9.0 8.5	11.5 12.0	6.0 6.0	12.5 13.5	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to A_n or B_n	Waveform 5 Waveform 6	5.0 6.0	9.0 9.0	12.5 12.5	4.5 5.0	14.0 14.0	ns

AC SETUP REQUIREMENTS for 74F648

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.0 4.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	3.5 6.5			4.0 7.0		ns

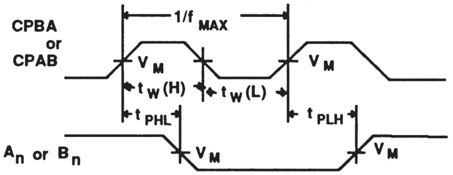
AC ELECTRICAL CHARACTERISTICS for 74F646A/74F648A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	3.0 3.0	4.0 4.5	8.0 8.0	4.5 4.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 2,3	2.0 2.0	3.5 3.0	7.5 7.5	2.5 2.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2,3	2.0 2.0	3.5 3.0	7.5 7.5	4.5 4.5	9.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	2.0 2.0	3.0 3.0	7.0 7.0	4.5 4.5	8.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time DIR to A_n or B_n	Waveform 5 Waveform 6	2.0 2.0	3.0 3.0	7.0 7.0	4.0 4.0	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	2.0 2.0	3.0 3.0	7.0 7.0	5.0 5.0	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to A_n or B_n	Waveform 5 Waveform 6	2.0 2.0	3.0 3.0	7.0 7.0	4.0 4.0	8.5 8.5	ns

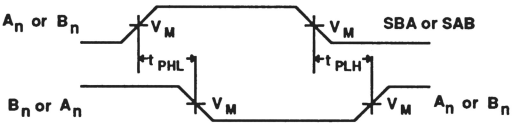
AC SETUP REQUIREMENTS for 74F646A/74F648A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.0 6.0			4.0 6.0		ns

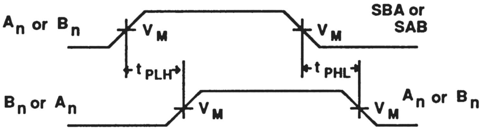
AC WAVEFORMS


CPBA
or
CPAB
1/f MAX
V M
V M
t W (H)
t W (L)
t PHL
t PLH
A n or B n
V M
V M

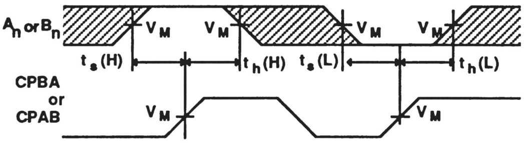
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency


A n or B n
V M
V M
SBA or SAB
t PHL
t PLH
B n or A n
V M
V M
A n or B n

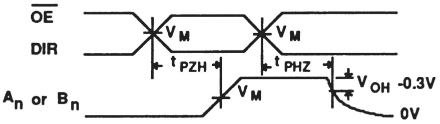
Waveform 2. Propagation Delay, An or Bn to Bn or An and SBA or SAB to An or Bn


A n or B n
V M
V M
SBA or SAB
t PLH
t PHL
B n or A n
V M
V M
A n or B n

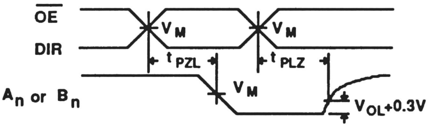
Waveform 3. Propagation Delay, An or Bn to Bn or An and SBA or SAB to An or Bn


A n or B n
V M
V M
V M
V M
t s (H)
t h (H)
t s (L)
t h (L)
CPBA
or
CPAB
V M
V M

Waveform 4. Data Setup And Hold Times


OE
DIR
V M
V M
t PZH
t PHZ
V OH -0.3V
A n or B n
V M
0V

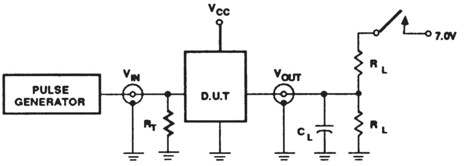
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level


OE
DIR
V M
V M
t PZL
t PLZ
A n or B n
V M
V OL+0.3V

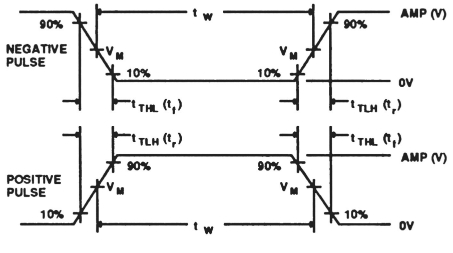
Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V CC
7.0V
PULSE GENERATOR
V IN
D.U.T
V OUT
R L
R T
C L
R L

Test Circuit For 3-State Outputs


t w
AMP (V)
90%
90%
NEGATIVE PULSE
V M
V M
10%
10%
0V
t THL (t f)
t TLH (t r)
t TLH (t r)
t THL (t f)
AMP (V)
90%
90%
POSITIVE PULSE
V M
V M
10%
10%
t w
0V

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F651, 74F651A
74F652, 74F652A
Transceivers/Registers

74F651/74F651A Octal Transceiver/Register, Inverting (3-State)
74F652/74F652A Octal Transceiver/Register, Non-Inverting (3-State)
Preliminary Specification for 74F651A and 74F652A
Product Specification for 74F651 and 74F652

FEATURES

- **High impedance base inputs for reduced loading (70μA in High and Low states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **3-state outputs**

DESCRIPTION

The 74F651/74F651A and 74F652/74F652A Transceivers/ Registers consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{\text{OEBA}}$) and Select (SAB, SBA) pins are provided for bus management.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F651/74F652	110MHz	140mA
74F651A/74F652A	110MHz	120mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim Dip (300mil)	N74F651N, N74F651AN, N74F652N, N74F651AN
24-Pin Plastic SOL[1]	N74F651D, N74F651AD, N74F652D, N74F652AD

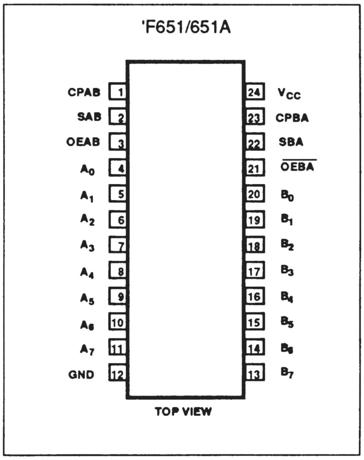
NOTE 1:
Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

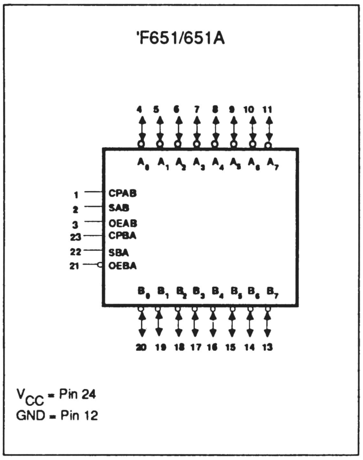
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A inputs	3.5/0.116	70μA/70μA
B_0 - B_7	B inputs	3.5/0.116	70μA/70μA
CPAB	A-to-B clock input	1.0/0.033	20μA/20μA
CPBA	B-to-A clock input	1.0/0.033	20μA/20μA
SAB	A-to-B select input	1.0/0.033	20μA/20μA
SBA	B-to-A select input	1.0/0.033	20μA/20μA
OEAB	A-to-B output enable input	1.0/0.033	20μA/20μA
$\overline{\text{OEBA}}$	B-to-A output enable input	1.0/0.033	20μA/20μA
A_0 - A_7	A outputs	750/106.7	15mA/64mA
B_0 - B_7	B outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

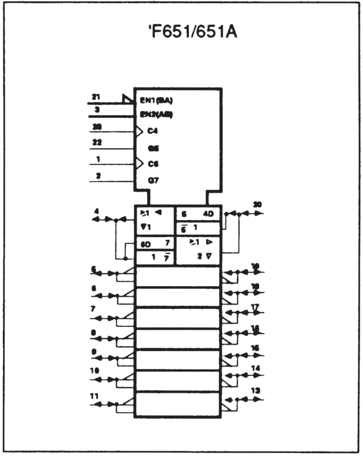

'F651/651A
CPAB 1
SAB 2
OEAB 3
A0 4
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
GND 12
24 Vcc
23 CPBA
22 SBA
21 OEBA
20 B0
19 B1
18 B2
17 B3
16 B4
15 B5
14 B6
13 B7
TOP VIEW

LOGIC SYMBOL


'F651/651A
4 5 6 7 8 9 10 11
A0 A1 A2 A3 A4 A5 A6 A7
1 CPAB
2 SAB
3 OEAB
23 CPBA
22 SBA
21 OEBA
B0 B1 B2 B3 B4 B5 B6 B7
20 19 18 17 16 15 14 13

V_{CC} = Pin 24
GND = Pin 12

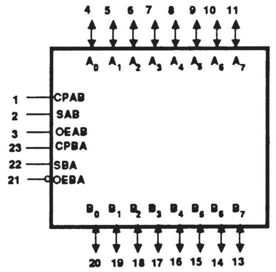
LOGIC SYMBOL(IEEE/IEC)


'F651/651A
21
3
23
22
1
2
EN1(BA)
EN2(AB)
C4
G5
C6
G7
4
5
6
7
8
9
10
11
20
19
18
17
16
15
14
13

The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'F651/651A and 'F652/652A. The select pins determine whether data is stored or transferred through the device in real time. The Output Enable pins determine the direction of the data flow.

LOGIC SYMBOL

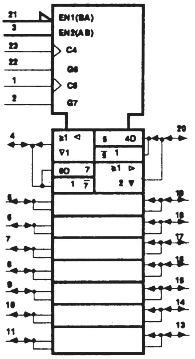
'F652/652A


4 5 6 7 8 9 10 11
A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7
1 CPAB
2 SAB
3 OEAB
23 CPBA
22 SBA
21 OEBA
B_0 B_1 B_2 B_3 B_4 B_5 B_6 B_7
20 19 18 17 16 15 14 13

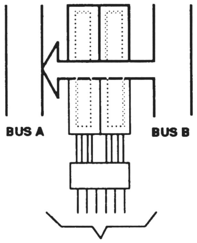
V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

'F652/652A

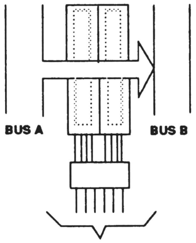

21
3
23
22
1
2
EN1(BA)
EN2(AB)
C4
G5
C6
G7
≥1
▽1
5 4D
3 1
6D 7
1 7
≥1
2 ▽
4 5 6 7 8 9 10 11
20 19 18 17 16 15 14 13

REAL TIME BUS TRANSFER BUS B TO BUS A



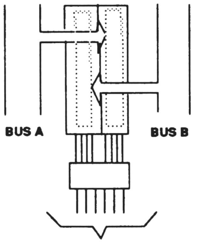
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER BUS A TO BUS B



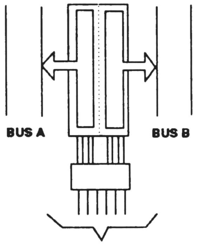
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

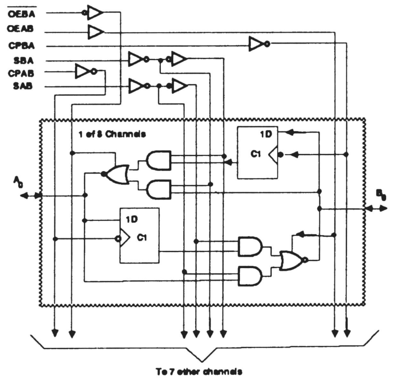
TRANSFER STORED DATA TO A OR B



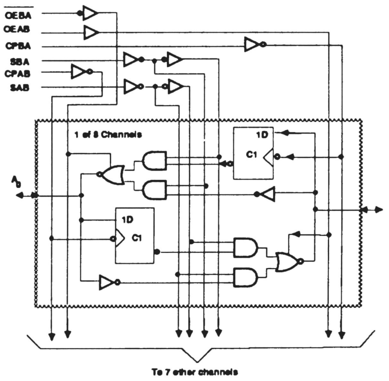
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

LOGIC DIAGRAM

'F651/651A


$\overline{OEBA}$
OEAB
CPBA
SBA
CPAB
SAB
1 of 8 Channels
1D
C1
1D
C1
A_0
B_0
To 7 other channels

'F652/652A


$\overline{OEBA}$
OEAB
CPBA
SBA
CPAB
SAB
1 of 8 Channels
1D
C1
1D
C1
A_0
To 7 other channels

FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
OEAB	**$\overline{OEBA}$**	**CPAB**	**CPBA**	**SAB**	**SBA**	**A_n**	**B_n**	**'F651/651A**	**'F652/652A**
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B data	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified*	Store A, Hold B	Store A, Hold B
H	H	↑	↑	L	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified*	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	L	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real time $\overline{B}$ data to A bus	Real time B data to A bus
L	L	X	H or L	X	H			Stored $\overline{B}$ data to A bus	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real time $\overline{A}$ data to B bus	Real time A data to B bus
H	H	H or L	X	H	X			Stored $\overline{A}$ data to B bus	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Store $\overline{A}$ data to B bus Store $\overline{B}$ data to A bus	Store A data to B bus Store B data to A bus

NOTES:
H= High voltage level
L= Low voltage level
*= The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
↑ =Low-to-High clock transition
X=Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.3		V
					I_{OH}=-15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=64mA	±10%V_{CC}			0.55	V
					I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others		V_{CC} = 0.0V, V_I = 7.0V					100	μA
		A_0-A_7, B_0-B_7		V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	OEAB, $\overline{OEBA}$, CPAB, CPBA SAB, SBA		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-20	μA
$I_{IH}+I_{OZH}$	Off-state output current High-level voltage applied	A_0-A_7, B_0-B_7		V_{CC} = MAX, V_I = 2.7V					70	μA
$I_{IL}+I_{OZL}$	Off-state output current Low-level voltage applied			V_{CC} = MAX, V_I = 0.5V					-70	μA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	74F651 74F652	I_{CCH}	V_{CC} = MAX				110 140[4]	155 185[4]	mA
			I_{CCL}					155 165[4]	200 240[4]	mA
			I_{CCZ}					130	175	mA
		74F651A 74F652A	I_{CCH}					110	145	mA
			I_{CCL}					120	155	mA
			I_{CCZ}					130	170	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. These values are for worst case only. Worst case is defined as all (16) I/O pins selected as outputs. When using worst case conditions thermal mounting is required.

AC ELECTRICAL CHARACTERISTICS for 74F651/74F652

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	**Typ**	**Max**	**Min**	**Max**	
f_{MAX}	Maximum clock frequency	Waveform 1	90	110		80		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.0 5.5	7.0 7.5	10.5 11.0	4.5 5.0	12.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 2,3	3.0 3.0	6.0 6.0	10.0 9.0	2.5 3.0	12.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2,3	4.0 4.0	7.0 6.5	10.0 9.5	4.0 4.0	12.5 10.0	ns
t_{PZH} t_{PZL}	Output Enable time OEAB or $\overline{\text{OEBA}}$ to A_n or B_n	Waveform 7 Waveform 8	4.0 6.0	7.0 10.5	10.0 12.0	3.5 5.5	11.0 13.0	ns
t_{PHZ} t_{PLZ}	Output Disable time OEAB or $\overline{\text{OEBA}}$ to A_n or B_n	Waveform 7 Waveform 8	4.5 4.5	9.5 9.0	13.0 13.0	4.0 4.0	14.5 15.5	ns

AC SETUP REQUIREMENTS for 74F651/74F652

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	**Typ**	**Max**	**Min**	**Max**	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.0 4.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low[1] $\overline{\text{OEBA}}$ to OEAB or OEAB to $\overline{\text{OEBA}}$	Waveform 5, 6	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{\text{OEBA}}$ to OEAB or OEAB to $\overline{\text{OEBA}}$	Waveform 5, 6	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.5 6.5			4.5 6.5		ns

Note: 1.Setup time is to protect against current surge caused by enabling 16 outputs (64mA per output) simultaneously.

AC ELECTRICAL CHARACTERISTICS for 74F651A/74F652A

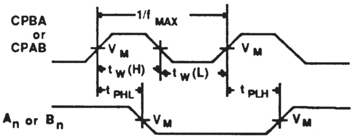
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	90	110		80		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.0 4.5	7.0 6.5	8.5 8.0	4.5 4.0	10.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 2,3	2.0 2.0	5.0 4.5	7.0 7.0	2.0 2.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2,3	4.0 4.0	7.0 6.5	8.0 7.5	4.0 4.0	10.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time OEAB or $\overline{OEBA}$ to A_n or B_n	Waveform 7 Waveform 8	4.0 5.0	7.0 8.5	8.0 9.0	3.5 4.5	9.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time OEAB or $\overline{OEBA}$ to A_n or B_n	Waveform 7 Waveform 8	4.5 4.5	8.0 8.0	8.5 8.5	4.0 4.0	9.5 9.5	ns

AC SETUP REQUIREMENTS for 74F651A/74F652A

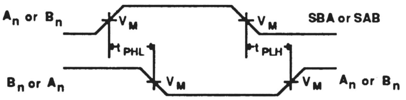
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.0 4.0			5.0 5.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_s(H) t_s(L)	Setup time, High or Low[1] $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	5.0 5.0			5.0 5.0		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	0 0			0 0		ns
t_w(H) t_w(L)	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.5 6.5			4.5 6.5		ns

Note: 1.Setup time is to protect against current surge caused by enabling 16 outputs (64mA per output) simultaneously.

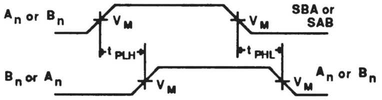
AC WAVEFORMS


CPBA or CPAB
1/f MAX
V_M
$t_W(H)$
$t_W(L)$
t_{PHL}
t_{PLH}
A_n or B_n

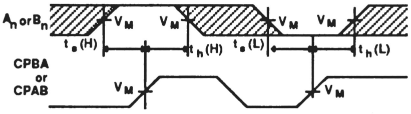
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency


A_n or B_n
SBA or SAB
V_M
t_{PHL}
t_{PLH}
B_n or A_n
A_n or B_n

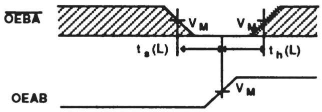
Waveform 2. Propagation Delay, An to Bn or Bn to An and SAB or SBA to An or Bn


A_n or B_n
SBA or SAB
V_M
t_{PLH}
t_{PHL}
B_n or A_n
A_n or B_n

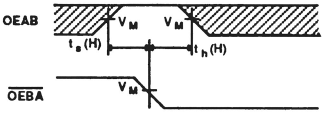
Waveform 3. Propagation Delay, An to Bn or Bn to An and SAB or SBA to An or Bn


A_n or B_n
V_M
$t_s(H)$
$t_h(H)$
$t_s(L)$
$t_h(L)$
CPBA or CPAB

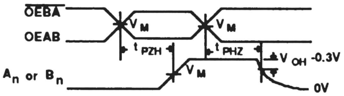
Waveform 4. Data Setup and Hold Times


$\overline{OEBA}$
V_M
$t_s(L)$
$t_h(L)$
OEAB

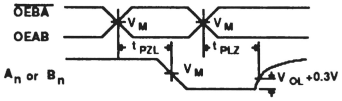
Waveform 5. $\overline{OEBA}$ to OEAB Setup and Hold Times


OEAB
V_M
$t_s(H)$
$t_h(H)$
$\overline{OEBA}$

Waveform 6. OEAB to $\overline{OEBA}$ Setup and Hold Times


$\overline{OEBA}$
OEAB
V_M
t_{PZH}
t_{PHZ}
V_{OH} -0.3V
0V
A_n or B_n

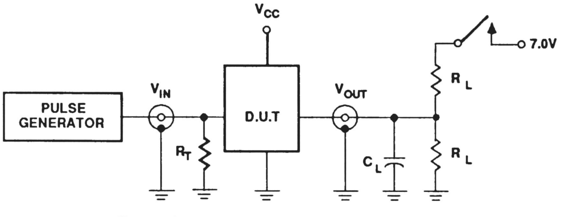
Waveform 7. 3-State Output Enable Time To High Level And Output Disable Time From High Level


$\overline{OEBA}$
OEAB
V_M
t_{PZL}
t_{PLZ}
V_{OL} +0.3V
A_n or B_n

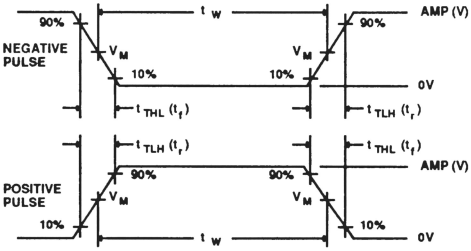
Waveform 8. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
7.0V
R_L
V_{IN}
V_{OUT}
PULSE GENERATOR
D.U.T
R_T
C_L
R_L

Test Circuit For 3-State Outputs


NEGATIVE PULSE
POSITIVE PULSE
t_W
AMP (V)
90%
V_M
10%
0V
t_{THL} (t_f)
t_{TLH} (t_r)

V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F657, 74F657A

Transceivers

74F657/657A Octal Transceivers With 8-Bit Parity Generator/Checker (3-State)

Product Specification for 74F657

Preliminary Specification for 74F657A

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F657	8.0ns	100mA
74F657A	7.0ns	100mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300 mil)	N74F657N, N74F657AN
24-Pin Plastic SOL[1]	N74F657D, N74F657AD

NOTE:

1. Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

FEATURES

- **Combines 74F245 and 74F280A functions in one package**
- **High impedance base input for reduced loading (70μA in High and Low states)**
- **Ideal in applications where High output drive and light bus loading are required (I_{IL} is 70μA vs FAST std of 600μA)**
- **3-state buffer outputs sink 64mA and source 15 mA**
- **Input diodes for termination effects**
- **24-pin plastic Slim Dip (300mil) package**

DESCRIPTION

The 74F657 is an octal transceiver featuring non-inverting buffers with 3-state outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 24mA at the A ports and 64mA at the B ports. The Transmit/Receive (T/$\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active-High) enables data from A ports to B ports; Receive (active-Low) enables data from B ports to A ports.

The 74F657A is the faster version of 74F657.

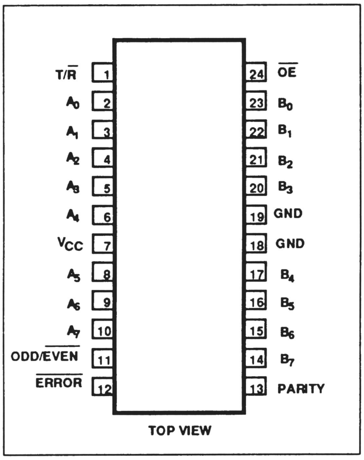
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A ports 3-state inputs	3.5/0.117	70μA/70μA
B_0 - B_7	B ports 3-state inputs	3.5/0.117	70μA/70μA
PARITY	Parity input	3.5/0.117	70μA/70μA
T/$\overline{R}$	Transmit/Receive input	2.0/0.066	40μA/40μA
ODD/$\overline{EVEN}$	Parity select input	1.0/0.033	20μA/20μA
$\overline{OE}$	Output enable input (active Low)	2.0/0.066	40μA/40μA
A_0 - A_7	A port 3-state outputs	150/40	3.0mA/24mA
B_0 - B_7	B port 3-state outputs	750/106.7	15mA/64mA
PARITY	Parity output	750/106.7	15mA/64mA
$\overline{ERROR}$	Error output	750/106.7	15mA/64mA

NOTE:

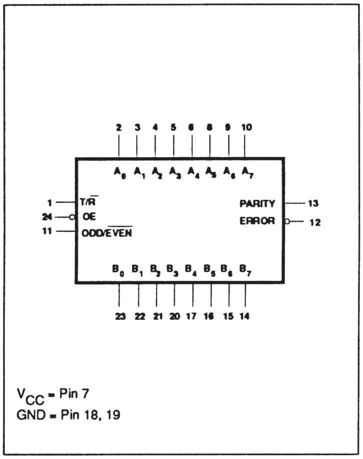
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



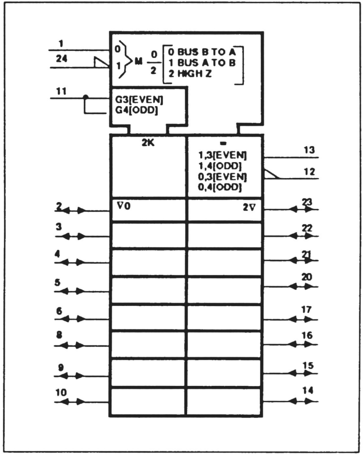
T/R̄ 1
A0 2
A1 3
A2 4
A3 5
A4 6
VCC 7
A5 8
A6 9
A7 10
ODD/EVEN 11
ERROR 12
24 OE
23 B0
22 B1
21 B2
20 B3
19 GND
18 GND
17 B4
16 B5
15 B6
14 B7
13 PARITY
TOP VIEW

LOGIC SYMBOL



2 3 4 5 6 8 9 10
A0 A1 A2 A3 A4 A5 A6 A7
1 T/R̄
24 OE
11 ODD/EVEN
PARITY 13
ERROR 12
B0 B1 B2 B3 B4 B5 B6 B7
23 22 21 20 17 16 15 14
VCC = Pin 7
GND = Pin 18, 19

LOGIC SYMBOL(IEEE/IEC)



1
24
0
1
M
0 BUS B TO A
1 BUS A TO B
2 HIGH Z
11
G3[EVEN]
G4[ODD]
2K
1,3[EVEN]
1,4[ODD]
0,3[EVEN]
0,4[ODD]
13
12
V0
2V
2 3 4 5 6 8 9 10
23 22 21 20 17 16 15 14

The Output Enable ($\overline{\text{OE}}$)input disables both the A and B ports by placing them in a high impedance condition when the $\overline{\text{OE}}$ input is High. The parity select (ODD/$\overline{\text{EVEN}}$) input gives the user the option of odd or even parity systems. The parity (PARITY) pin is an output from the generator/checker when transmitting from the port A to B (T/$\overline{\text{R}}$=High) and an input when receiving from port B to A port (T/$\overline{\text{R}}$=Low). When transmitting (T/$\overline{\text{R}}$=High) the parity select (ODD/$\overline{\text{EVEN}}$) input is set, then the A port data is polled to determine the number of High bits. The parity (PARITY) output then goes to the logic state determined by the parity select (ODD/$\overline{\text{EVEN}}$) setting and by the number of High bits on port A. For example, if the parity select (ODD/$\overline{\text{EVEN}}$) is set Low (even parity), and the number of High bits on port A is odd, then the parity (PARITY) output will be High, transmitting even parity. If the number of High bits on port A is even, then the parity (PARITY) output will be Low, keeping even parity. When in receive mode (T/$\overline{\text{R}}$=Low) the B port is polled to determine the number of High bits. If parity select (ODD/$\overline{\text{EVEN}}$) is Low (even parity) and the number of Highs on port B is:

(1) odd and the parity (PARITY) input is High, then $\overline{\text{ERROR}}$ will be High, signifying no error.

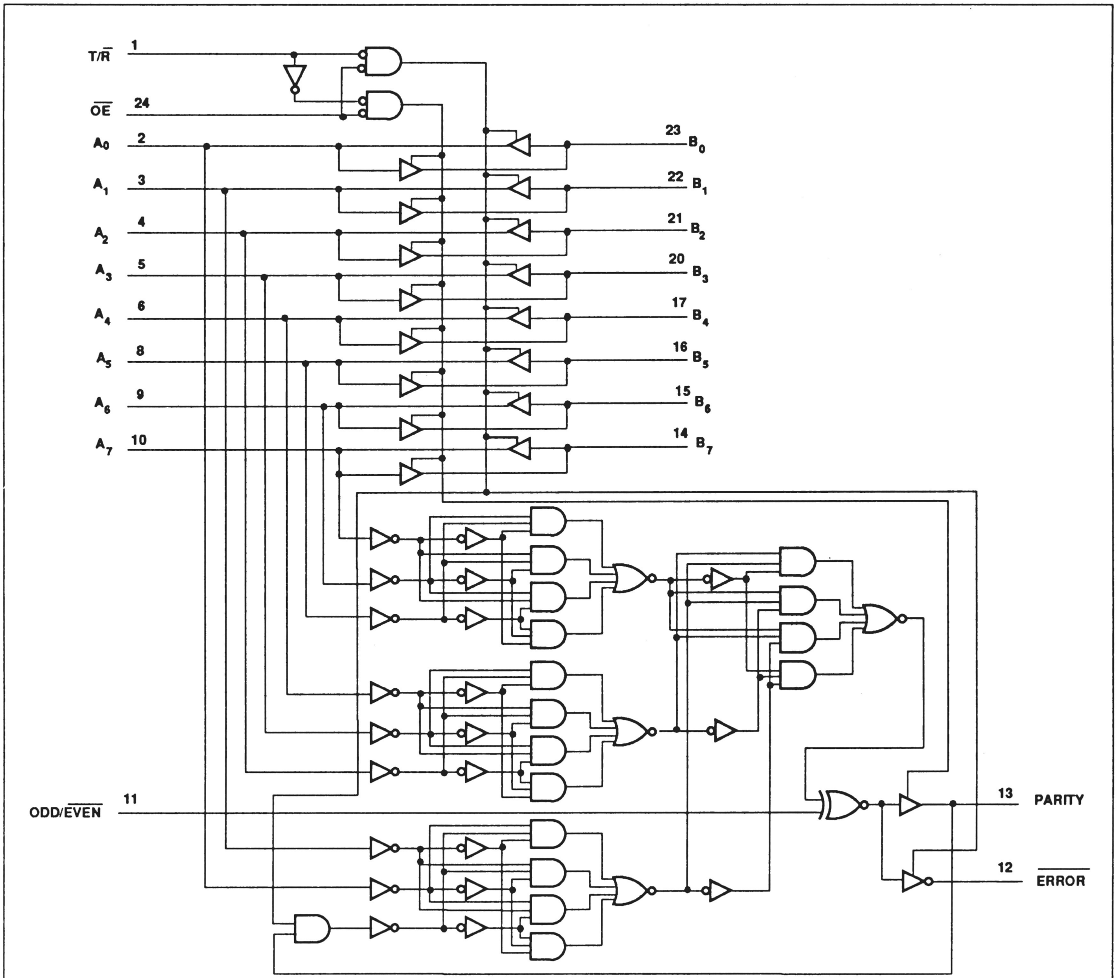
(2) even and the parity (PARITY) input is Low, then $\overline{\text{ERROR}}$ will be asserted Low, indicating an error.

FUNCTION TABLE

NUMBER OF INPUTS THAT ARE HIGH	INPUTS			INPUT/ OUPUT	OUTPUTS	
	$\overline{\text{OE}}$	T/$\overline{\text{R}}$	ODD/$\overline{\text{EVEN}}$	PARITY	$\overline{\text{ERROR}}$	OUTPUTS MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	3-state

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM


T/R̄ 1
O̅E̅ 24
A0 2
A1 3
A2 4
A3 5
A4 6
A5 8
A6 9
A7 10
23 B0
22 B1
21 B2
20 B3
17 B4
16 B5
15 B6
14 B7
ODD/E̅V̅E̅N̅ 11
13 PARITY
12 E̅R̅R̅O̅R̅

V_{CC}=Pin 7
GND=Pin 18, 19

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7, PARITY, $\overline{ERROR}$	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0B_7,PARITY,$\overline{ERROR}$			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7, PARITY, $\overline{ERROR}$			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	All outputs	V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		B_0-B_7, PARITY, $\overline{ERROR}$		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7, PARITY, $\overline{ERROR}$		I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OE}$, T/$\overline{R}$, ODD/$\overline{EVEN}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_0-A_7	V_{CC} = MAX, V_I = 5.5V					2	mA
		B_0-B_7						1	mA
I_{IH}	High-level input current	ODD/$\overline{EVEN}$	V_{CC} = MAX, V_I = 2.7V					20	µA
		$\overline{OE}$, T/$\overline{R}$						40	µA
I_{IL}	Low-level input current	ODD/$\overline{EVEN}$	V_{CC} = MAX, V_I = 0.5V					-20	µA
		$\overline{OE}$, T/$\overline{R}$						-40	µA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied	A_0-A_7, B_0-B_7, PARITY	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-70	µA
I_{OZH}	Off-state output current High-level voltage applied	$\overline{ERROR}$	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]	A_0-A_7	V_{CC} = MAX			-60		-150	mA
		B_0-B_7				-100		-225	µA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				90	125	mA
		I_{CCL}					106	150	mA
		I_{CCZ}					98	145	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for 74F657

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 2	2.5 3.0	5.5 6.0	7.5 7.5	2.5 3.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to PARITY	Waveform 1,2	7.0 7.0	10.0 10.0	14.0 15.0	7.0 7.0	16.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{\text{EVEN}}$ to PARITY, $\overline{\text{ERROR}}$	Waveform 1,2	4.5 4.5	7.5 8.0	11.0 11.5	4.5 4.5	12.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to $\overline{\text{ERROR}}$	Waveform 1,2	8.0 8.0	14.0 14.0	20.5 20.5	7.5 7.5	22.5 22.5	ns
t_{PLH} t_{PHL}	Propagation delay PARITY to $\overline{\text{ERROR}}$	Waveform 2	8.0 8.0	11.5 12.0	15.5 15.5	7.5 6.0	16.5 17.0	ns
t_{PZH} t_{PZL}	Output Enable time[1] to High or Low level	Waveform 3 Waveform 4	3.0 4.0	5.5 7.0	8.0 9.5	3.0 4.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 3 Waveform 4	2.0 2.0	4.5 4.0	7.5 6.0	2.0 2.0	8.0 6.5	ns

NOTE:

1. These delay times reflect the 3-state recovery time only and not the signal through the buffers or the parity check circuitry. To assure VALID information at the $\overline{\text{ERROR}}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{\text{ERROR}}$ output after the $\overline{\text{ERROR}}$ pin has been enabled (Output Enable time). VALID data at the $\overline{\text{ERROR}}$ pin ≥ (B to A) + (A to PARITY) + (Output Enable time).

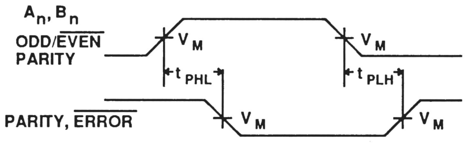
AC ELECTRICAL CHARACTERISTICS for 74F657A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 2	2.0 2.0	4.5 4.5	7.0 7.0	2.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n to PARITY	Waveform 1,2	6.5 6.5	9.5 9.5	13.0 13.0	6.5 6.5	14.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{\text{EVEN}}$ to PARITY, $\overline{\text{ERROR}}$	Waveform 1,2	4.5 4.5	7.0 7.0	10.5 10.5	4.5 4.5	11.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to $\overline{\text{ERROR}}$	Waveform 1,2	7.0 7.0	12.0 12.0	18.0 18.0	6.5 6.5	19.0 19.0	ns
t_{PLH} t_{PHL}	Propagation delay PARITY to $\overline{\text{ERROR}}$	Waveform 2	8.0 8.0	10.5 10.5	14.0 14.0	7.0 7.0	15.0 15.0	ns
t_{PZH} t_{PZL}	Output Enable time[1] to High or Low level	Waveform 3 Waveform 4	3.0 4.0	5.5 6.5	8.0 9.0	3.0 4.0	9.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 3 Waveform 4	2.0 2.0	4.5 4.0	7.5 6.0	2.0 2.0	8.0 6.5	ns

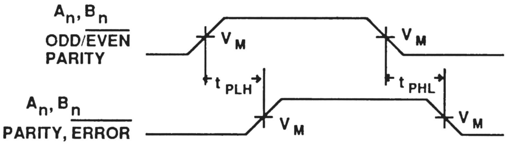
NOTE:

1. These delay times reflect the 3-state recovery time only and not the signal through the buffers or the parity check circuitry. To assure VALID information at the $\overline{\text{ERROR}}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{\text{ERROR}}$ output after the $\overline{\text{ERROR}}$ pin has been enabled (Output Enable time). VALID data at the $\overline{\text{ERROR}}$ pin ≥ (B to A) + (A to PARITY) + (Output Enable time).

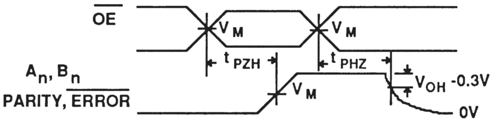
AC WAVEFORMS


A_n, B_n
ODD/$\overline{\text{EVEN}}$
PARITY
V_M
V_M
t_{PHL}
t_{PLH}
PARITY, $\overline{\text{ERROR}}$
V_M
V_M

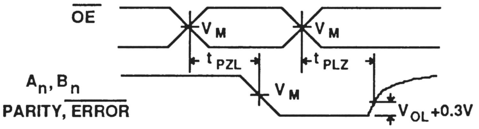
Waveform 1. Propagation Delay for Inverting Outputs


A_n, B_n
ODD/$\overline{\text{EVEN}}$
PARITY
V_M
V_M
t_{PLH}
t_{PHL}
A_n, B_n
PARITY, $\overline{\text{ERROR}}$
V_M
V_M

Waveform 2. Propagation Delay for Non-Inverting Outputs


$\overline{\text{OE}}$
V_M
V_M
t_{PZH}
t_{PHZ}
A_n, B_n
PARITY, $\overline{\text{ERROR}}$
V_M
V_{OH} -0.3V
0V

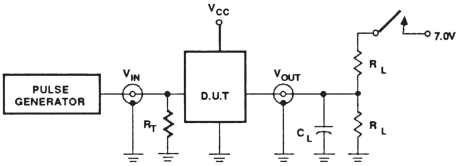
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level


$\overline{\text{OE}}$
V_M
V_M
t_{PZL}
t_{PLZ}
A_n, B_n
PARITY, $\overline{\text{ERROR}}$
V_M
V_{OL}+0.3V

Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
7.0V
PULSE GENERATOR
V_{IN}
D.U.T
V_{OUT}
R_L
R_T
C_L
R_L

Test Circuit For 3-State Outputs

SWITCH POSITION

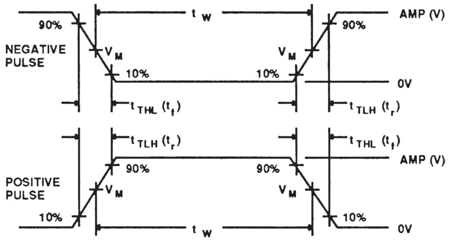
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


NEGATIVE PULSE
90%
t_w
90%
AMP (V)
V_M
V_M
10%
10%
0V
t_{THL} (t_f)
t_{TLH} (t_r)
t_{TLH} (t_r)
t_{THL} (t_f)
AMP (V)
POSITIVE PULSE
90%
90%
V_M
V_M
10%
t_w
10%
0V

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F670
Register File

4X4 Register File (3-State)
Product Specification

FEATURES

- **Simultaneous and independent Read and Write operations**
- **Expandable to almost any word size and bit length**
- **3-state outputs**

DESCRIPTION

The 74F670 is a 16 bit 3-state Register File organized as 4 words of 4 bits each. Separate Read and Write Address and Enable inputs are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four data inputs. The Write Address inputs (W_A and W_B) determine the location of the stored word. The Write Address inputs should only be changed when the $\overline{WE}$ input is High for conventional operation. When the Write Enable ($\overline{WE}$) input is Low, the data is entered into the addressed location. The addressed location remains transparent to the data while the $\overline{WE}$ is Low.Data supplied at the inputs will be read out in true (non-inverting) form from the 3-state outputs. Data and address inputs are inhibited when $\overline{WE}$ is High. Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs (R_A, R_B). The addressed word appears at the four outputs when the Read Enable ($\overline{RE}$) is Low. Data outputs are in the High impedance "off" state when the $\overline{RE}$ is High. This permits outputs to be tied together to increase the word capacity to very large numbers.

Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-state outputs together. Since the limiting factor for expansion is the output High current, further stacking is possible by tying pullup resistors to the outputs to increase the I_{OH} current available. Design of the Read Enable signals for the stacked devices must ensure that there is no overlap in the Low levels which cause more than one output tobe active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the Enable and address inputs of each device in parallel.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N74F670	6.5 ns	50mA

ORDERING INFORMATION

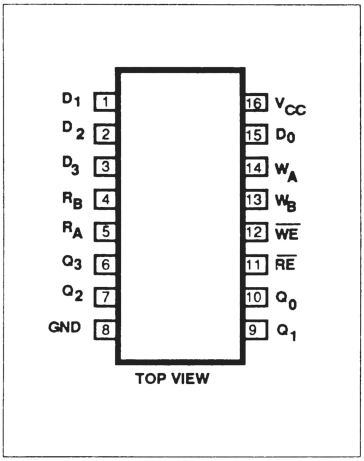
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F670N
16-Pin Plastic SOL	N74F670D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

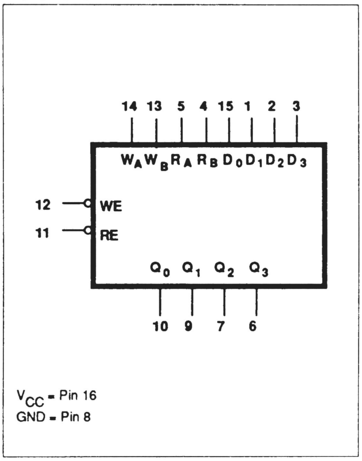
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
W_A ,W_B	Write address inputs	1.0/1.0	20µA/0.6mA
R_A ,R_B	Read address inputs	1.0/1.0	20µA/0.6mA
$\overline{WE}$	Write Enable input	1.0/1.0	20µA/0.6mA
$\overline{RE}$	Read Enable input	1.0/1.0	20µA/0.6mA
Q_0 - Q_3	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

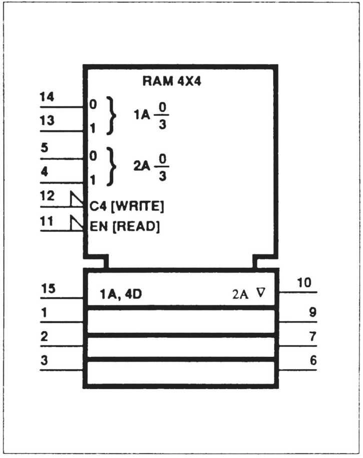
PIN CONFIGURATION



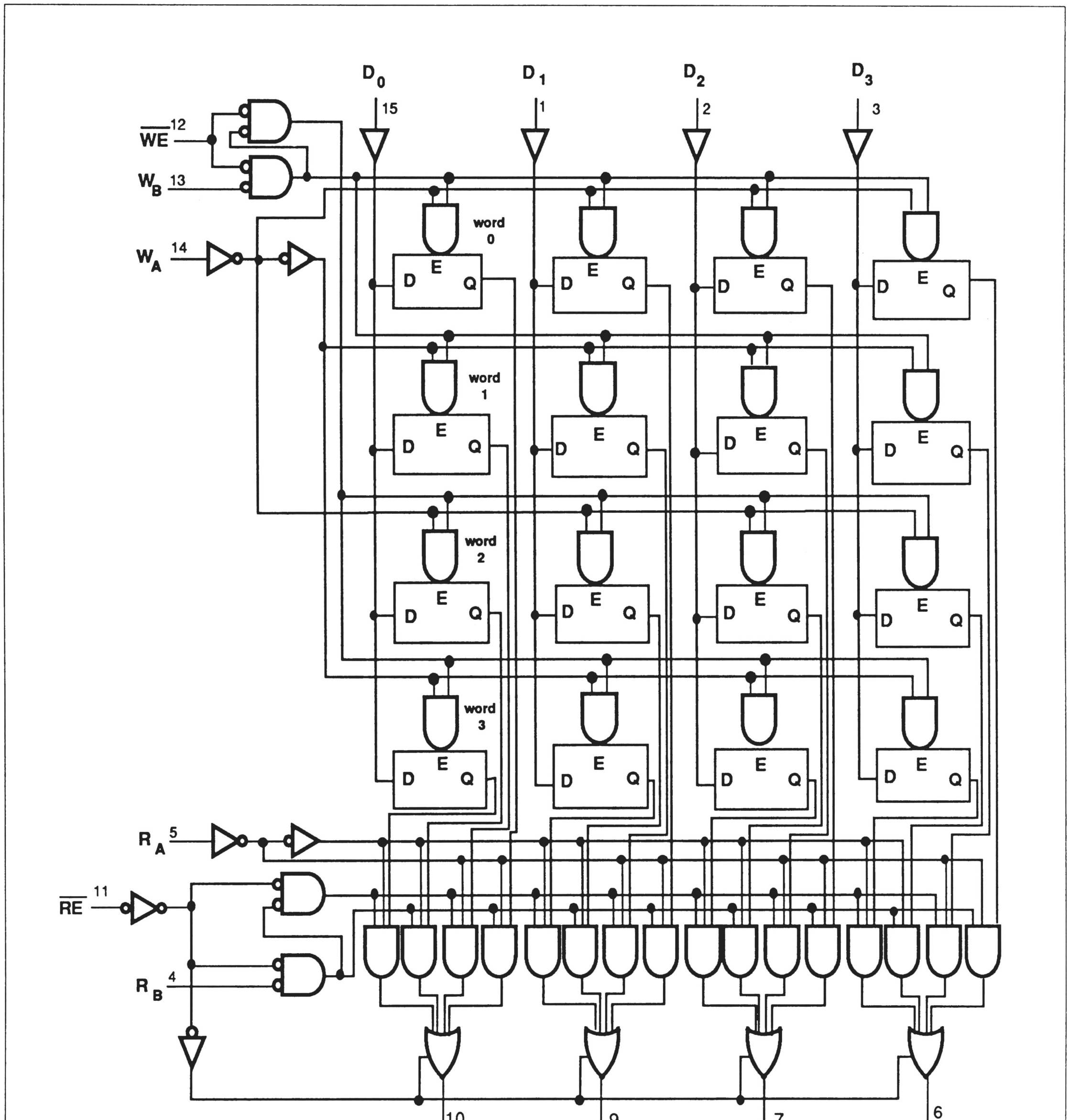
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM


D0
D1
D2
D3
15
1
2
3
WE 12
WB 13
WA 14
word 0
word 1
word 2
word 3
D
E
Q
RA 5
RE 11
RB 4
10
9
7
6
Q0
Q1
Q2
Q3

VCC=pin 16
GND=pin 8

WORD SELECT FUNCTION TABLE

WRITE MODE		READ MODE		OPERATING MODE
W_a	W_b	R_a	R_b	**Word selected**
L	L	L	H	Word 0
L	H	L	H	Word 1
H	L	H	L	Word 2
H	H	H	H	Word 3

H = High voltage level
L = Low voltage level

WRITE MODE FUNCTION TABLE

INPUTS		INTERNAL LATCHES*	OPERATING MODE
$\overline{WE}$	D_n		
L	L	L	Write data
L	H	H	
H	X	NC	Data latched

H = High voltage level
L = Low voltage level
NC=No change
X = Don't care

*=The write address (W_A and W_B) to the "Internal latches" must be stable while $\overline{WE}$ is Low for conventional operation.

READ MODE FUNCTION TABLE

INPUT	INTERNAL LATCHES*	OUTPUT	OPERATING MODE
$\overline{RE}$		Q_n	
L	L	L	Read
L	H	H	
H	X	Z	Disabled

H = High voltage level
L = Low voltage level
X=Don't care
Z=High impedance"off" state

*=The selection of the "internal latches" by Read Address (R_A and R_B) are not constrained by $\overline{WE}$ or $\overline{RE}$ operation.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off state output current, High-level voltage applied		V_{CC} =MAX, V_O=2.7V				50	µA
I_{OZL}	Off state output current, Low-level voltage applied		V_{CC} =MAX, V_O=0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			50	70	mA
		I_{CCL}				50	70	mA
		I_{CCZ}				55	80	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

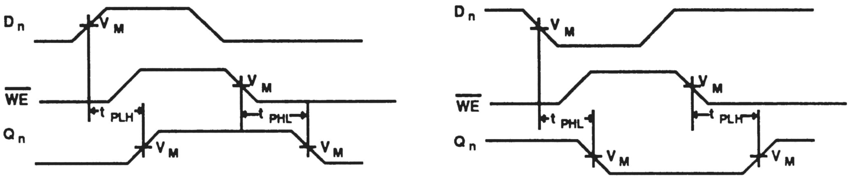
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay R_A, R_B to Q_n	Waveform 2	3.5 4.0	5.5 5.5	9.0 8.5	3.0 3.5	10.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{WE}$ to Q_n	Waveform 1	5.0 6.5	7.0 8.5	10.0 11.5	4.5 6.0	11.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	3.5 6.0	6.0 8.0	8.5 11.0	3.0 5.5	9.5 12.5	ns
t_{PZH} t_{PZL}	$\overline{RE}$ Enable time Q_n High or Low level	Waveform 3 Waveform 4	3.0 4.5	7.0 6.5	12.0 9.0	2.5 4.0	13.0 10.0	ns
t_{PHZ} t_{PLZ}	$\overline{RE}$ Disable time Q_n High or Low level	Waveform 3 Waveform 4	2.0 3.0	3.0 5.0	6.5 8.5	1.5 3.0	7.5 8.5	ns

AC SETUP REQUIREMENTS

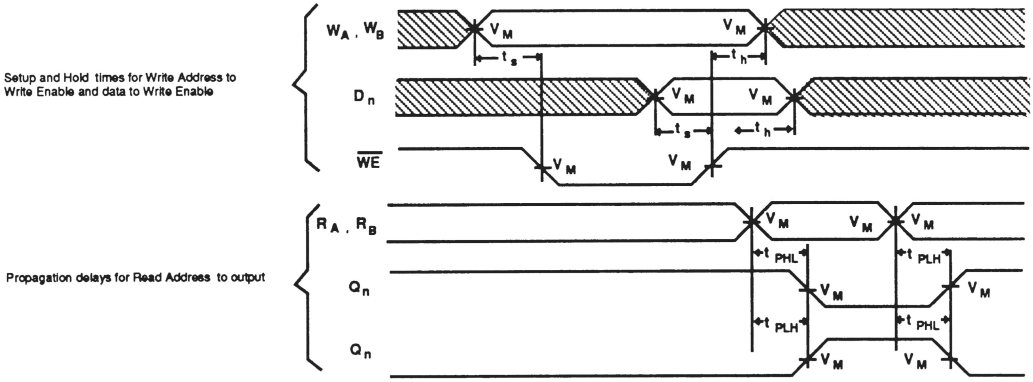
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to positive going $\overline{WE}$	Waveform 2	1.5 6.0			1.5 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to positive going $\overline{WE}$	Waveform 2	0 1.0			0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low W_A, W_B to negative going $\overline{WE}$[1]	Waveform 2	0 0			0 0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low W_A, W_B to negative going $\overline{WE}$[1]	Waveform 2	0 0			0 0		ns
$t_w(L)$	$\overline{RE}$ Pulse width, Low	W aveform 3	6.5			8.5		ns

NOTE 1: Write Address (W_A,W_B) setup time will protect the data written into the previous address. If protection of data in the previous address is not required, setup time for Write Address to $\overline{WE}$ can be ignored.. Any address selection sustained for the final 7ns of the $\overline{WE}$ pulse and during hold time for Write Address to $\overline{WE}$ will result in data being written into that location.

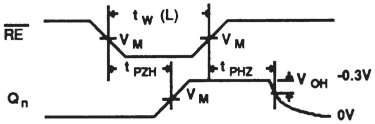
AC WAVEFORMS


Dn
VM
WE
VM
tPLH
tPHL
Qn
VM
VM
Dn
VM
WE
VM
tPHL
tPLH
Qn
VM
VM

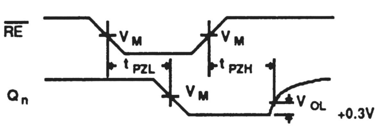
Waveform1. Propagation delay, Write Enable And Data To Outputs


Setup and Hold times for Write Address to Write Enable and data to Write Enable
WA, WB
VM
VM
ts
th
Dn
VM
VM
ts
th
WE
VM
VM
Propagation delays for Read Address to output
RA, RB
VM
VM
VM
tPHL
tPLH
Qn
VM
VM
tPLH
tPHL
Qn
VM
VM

Waveform 2. Setup and Hold Times, Write Address To Write Enable and Data To Write Enable And Propagation Delay Read Address To Output


RE
tW (L)
VM
VM
tPZH
tPHZ
VOH
-0.3V
Qn
VM
0V

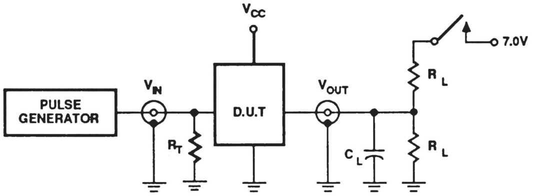
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level


RE
VM
VM
tPZL
tPZH
Qn
VM
VOL
+0.3V

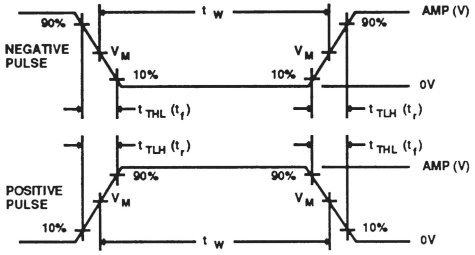
Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
R_T
D.U.T
V_{OUT}
C_L
R_L
R_L
7.0V

Test Circuit For 3-State Outputs


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
V_M
t_W
t_{THL} (t_f)
t_{TLH} (t_r)
AMP (V)
0V

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F674

Shift Register

16-Bit Shift Register, Parallel-In/Serial-Out (3-State)
Product Specification

FEATURES

- **16-bit serial I/O shift register**
- **16-bit parallel-in/serial-out converter**
- **Recirculating serial shifting**
- **Common serial data I/O pins (3-state)**

DESCRIPTION

The 74F674 is a 16 bit shift register with serial and parallel load capability and serial output. A single pin serves alternately as an input for serial entry or as 3-state serial output. In the serial out mode the data recirculates in the register. Chip select, Read/Write and Mode inputs provide control flexibility. The 'F674 operates in one of four modes, as indicated in the Function Table.

Hold : a High signal on the Chip Select ($\overline{CS}$) input prevents clocking and forces the Serial Input/Output (SI/O) 3-state buffer into the high impedance state.

Serial load : data present on the SI/O pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the D_0 position and shifts toward Q_{15} on successive clocks.

Serial output : the SI/O 3-state buffer is active and the register contents are shifted out from Q_{15} and simultaneously shifted back into Q_0.

Parallel load : data present on D_0-D_{15} IS entered into the register on the falling edge of $\overline{CP}$. The SI/O 3-state buffer is active and represents the Q_{15} output.

To prevent false clocking, $\overline{CP}$ must be Low during a Low-to-High transition of $\overline{CS}$.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F674	95MHz	55mA

ORDERING INFORMATION

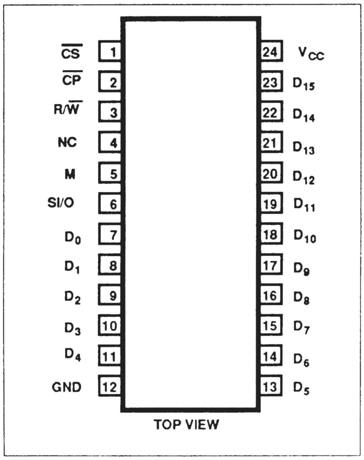
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F674N
24-Pin Plastic SOL	N74F674D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_{15}	Parallel data inputs	1.0/1.0	20µA/0.6mA
$\overline{CS}$	Chip Select input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CP}$	Clock Pulse input (active falling edge)	1.0/1.0	20µA/0.6mA
M	Mode select input	1.0/1.0	20 A/0.6mA
R/$\overline{W}$	Read/Write input	1.0/1.0	20µA/0.6mA
SI/O	Serial data input or	3.5/1.0	70 A/0.6mA
	Serial 3-state output	150/40	3.0mA/24mA

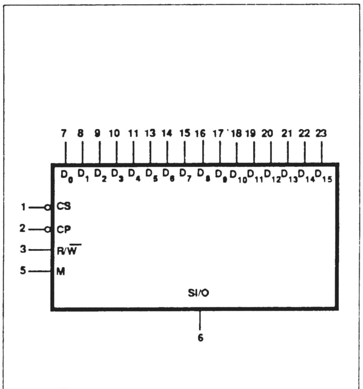
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



$\overline{CS}$ 1
$\overline{CP}$ 2
R/$\overline{W}$ 3
NC 4
M 5
SI/O 6
D_0 7
D_1 8
D_2 9
D_3 10
D_4 11
GND 12
24 V_{CC}
23 D_{15}
22 D_{14}
21 D_{13}
20 D_{12}
19 D_{11}
18 D_{10}
17 D_9
16 D_8
15 D_7
14 D_6
13 D_5
TOP VIEW

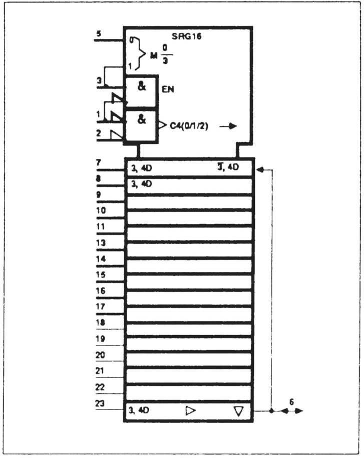
LOGIC SYMBOL



7 8 9 10 11 13 14 15 16 17 18 19 20 21 22 23
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8 D_9 D_{10} D_{11} D_{12} D_{13} D_{14} D_{15}
1 CS
2 CP
3 R/$\overline{W}$
5 M
SI/O
6

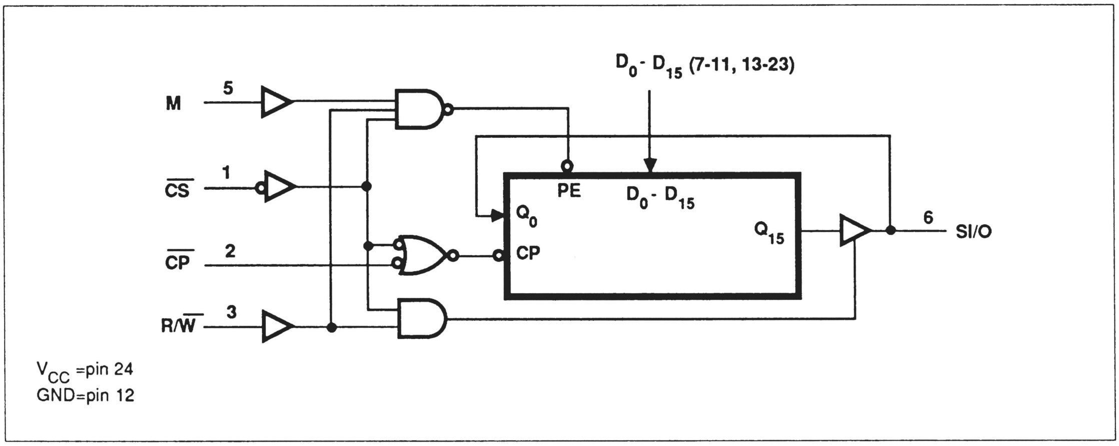
V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)



SRG16
5
0
1
M $\frac{0}{3}$
3
&
EN
1
2
&
C4(0/1/2)
7
3, 4D
$\overline{3}$, 4D
8
3, 4D
9
10
11
13
14
15
16
17
18
19
20
21
22
23
3, 4D
6

LOGIC DIAGRAM



V_{CC} =pin 24
GND=pin 12

FUNCTION TABLE

CONTROL INPUTS				SI/O STATUS	OPERATING MODE
$\overline{CS}$	R/$\overline{W}$	M	$\overline{CP}$		
H	X	X	X	High Z	Hold
L	L	X	↓	Data in	Serial load
L	H	L	↓	Data out	Serial output with recirculation
L	H	H	↓	Active	Parallel load ; no shifting

H = High voltage level
L = Low voltage level
X = Don't care
↓ = High-to-Low transition of designated input

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input clamp current at maximum input voltage	SI/O only	V_{CC} = MAX, V_I = 5.5V				100	µA
		others	V_{CC} = MAX, V_I = 7.0V					
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
$I_{OZH}+I_{IH}$	Off state output current, High-level voltage applied	SI/O only	V_{CC} =MAX, V_O=2.7V				70	µA
$I_{OZL}+I_{IL}$	Off state output current, Low-level voltage applied		V_{CC} =MAX, V_O=0.5V				-600	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			55	80	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

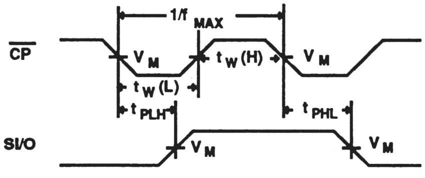
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	95		70		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to SI/O	Waveform 1	7.0 6.0	9.5 8.5	12.5 11.5	6.5 5.5	14.0 12.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{CS}$ to SI/O	Waveform 3 Waveform 4	5.5 7.0	8.5 9.5	11.0 12.5	5.0 6.5	12.5 14.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{CS}$ to SI/O	Waveform 3 Waveform 4	3.0 4.5	6.0 7.5	8.5 10.0	3.0 4.5	10.0 11.5	ns
t_{PZH} t_{PZL}	Output Enable time R/$\overline{W}$ to SI/O	Waveform 3 Waveform 4	6.0 7.5	8.5 10.0	11.5 13.0	5.5 7.0	13.0 14.0	ns
t_{PHZ} t_{PLZ}	Output Disable time R/$\overline{W}$ to SI/O	Waveform 3 Waveform 4	5.0 5.5	7.5 8.0	10.5 11.0	4.5 5.0	12.0 13.5	ns

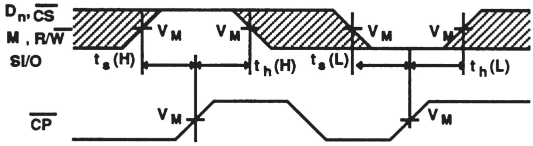
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low SI/O to $\overline{CP}$	Waveform 2	2.0 2.0			2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low SI/O to $\overline{CP}$	Waveform 2	1.5 1.5			2.0 2.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{CP}$	Waveform 2	1.5 1.0			2.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{CP}$	Waveform 2	3.0 4.0			3.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low M to $\overline{CP}$	Waveform 2	2.0 5.5			2.5 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low M to $\overline{CP}$	Waveform 2	0.0 0.0			1.0 1.0		ns
$t_s(L)$	Setup time, Low $\overline{CS}$ to $\overline{CP}$	Waveform 2	8.0			9.0		ns
$t_h(H)$	Hold time, High $\overline{CS}$ to $\overline{CP}$	Waveform 2	0.0			0.0		ns
$t_w(H)$ $t_w(L)$	$\overline{CP}$ Pulse width, High or Low	Waveform 1	3.5 4.5			4.0 5.0		ns

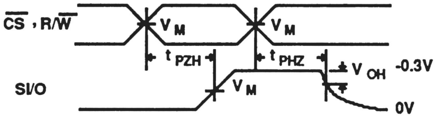
AC WAVEFORMS


CP
1/f MAX
V M
t W (L)
t W (H)
t PLH
t PHL
SI/O
V M

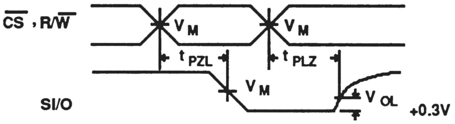
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency


D n, CS
M , R/W
SI/O
V M
t s (H)
t h (H)
t s (L)
t h (L)
CP

Waveform 2. Data Setup And Hold Times


CS , R/W
V M
t PZH
t PHZ
V OH -0.3V
SI/O
0V

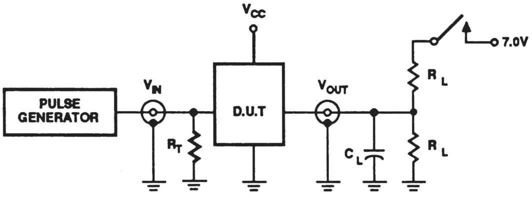
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level


CS , R/W
V M
t PZL
t PLZ
SI/O
V OL
+0.3V

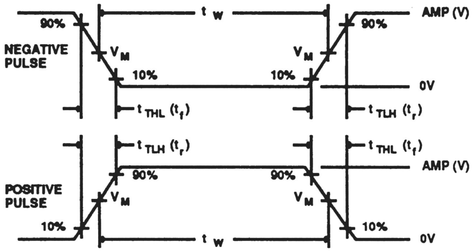
Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V CC
7.0V
PULSE GENERATOR
V IN
R T
D.U.T
V OUT
C L
R L
R L

Test Circuit For 3-State Outputs


NEGATIVE PULSE
90%
V M
10%
t W
AMP (V)
0V
t THL (t f)
t TLH (t r)
POSITIVE PULSE
90%
V M
10%
t W
AMP (V)
0V

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F711/711-1,
74F712/712-1
Multiplexers

FEATURES for 74F711/711-1

- **Consists of five 2-to-1 Multiplexers**
- **Equivalent to two 'F257As or 'F258As**
- **High impedance NPN base inputs for reduced loading (20µA in High and Low states)**
- **Designed for address multiplexing of dynamic RAM and other applications**
- **Output inverting/non-inverting option**
- **A 30 ohm series termination resistor on each output-'F711-1**
- **Outputs sink 64mA**

FEATURES for 74F712/712-1

- **Consists of five 3-to-1 Multiplexers**
- **Equivalent to four 'F157As or 'F158As**
- **High impedance NPN base inputs for reduced loading (20µA in High and Low states)**
- **Designed for address multiplexing of dynamic RAM and other applications**
- **A 30 ohm series termination resistor on each output-'F712-1**

DESCRIPTION

The 74F711/711-1 consists of five 2-to-1 multiplexers designed for address multiplexing for dynamic RAMs and other multiplexing applications. The 'F711 has a common select (S) input, an Output Enable ($\overline{OE}$) input and an Output Inverting ($\overline{INV}$) input to control the 3-state outputs.

74F711 Quint 2-to-1 Data Selector Multiplexer (3-State)
74F711-1 Quint 2-to-1 Data SelectorMultiplexer With 30 ohm series termination resistors(3State)
74F712 Quint 3-to-1 Data SelectorMultiplexer
74F712-1 Quint 3-to-1 Data SelectorMultiplexer With 30 ohm series termination resistors

Preliminary Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F711/711-1	5.5ns	24mA
74F712/712-1	6.0ns	24mA

ORDERING INFORMATION

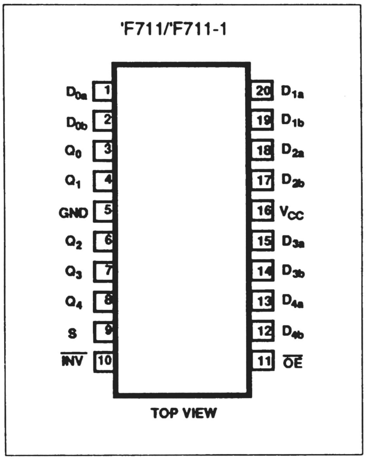
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F711N, N74F711-1N
24-Pin Plastic Slim DIP (300 mil)	N74F712N, N74F712-1N
20-Pin Plastic SOL	N74F711D, N74F711-1D
24-Pin Plastic SOL	N74F712D, N74F712-1D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

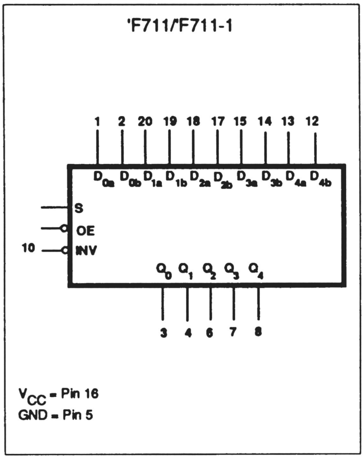
TYPE	PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F711/ 'F711-1	D_{na} - D_{nb}	Data inputs	1.0/0.033	20µA/20µA
	S	Select input	1.0/0.033	20µA/20µA
	$\overline{OE}$	Output Enable input (active Low)	1.0/0.033	20µA/20µA
	$\overline{INV}$	Output Inverting input (active Low)	1.0/0.033	20µA/20µA
	Q_0 - Q_4	Data outputs	750/106.7	15mA/64mA
'F712/ 'F712-1	D_{na}, D_{nb}, D_{nc}	Data inputs	1.0/0.033	20µA/20µA
	S_0, S_1	Select inputs	1.0/0.033	20µA/20µA
	Q_0 - Q_4	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

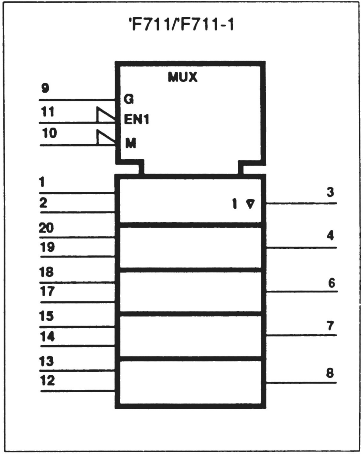
PIN CONFIGURATION


'F711/'F711-1
D0a 1
D0b 2
Q0 3
Q1 4
GND 5
Q2 6
Q3 7
Q4 8
S 9
INV 10
20 D1a
19 D1b
18 D2a
17 D2b
16 VCC
15 D3a
14 D3b
13 D4a
12 D4b
11 OE
TOP VIEW

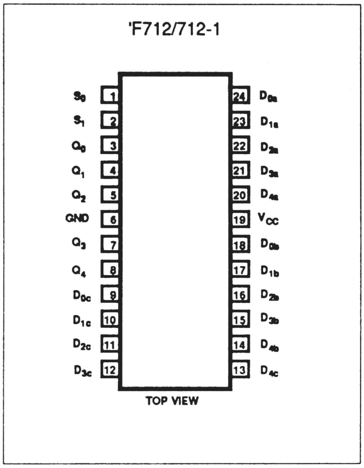
LOGIC SYMBOL


'F711/'F711-1
1 2 20 19 18 17 15 14 13 12
D0a D0b D1a D1b D2a D2b D3a D3b D4a D4b
S
OE
10 INV
Q0 Q1 Q2 Q3 Q4
3 4 6 7 8
VCC = Pin 16
GND = Pin 5

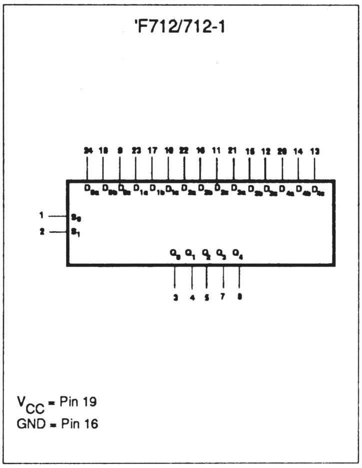
LOGIC SYMBOL(IEEE/IEC)


'F711/'F711-1
MUX
9 G
11 EN1
10 M
1
2
1 ▽
3
20
19
4
18
17
6
15
14
7
13
12
8

PIN CONFIGURATION

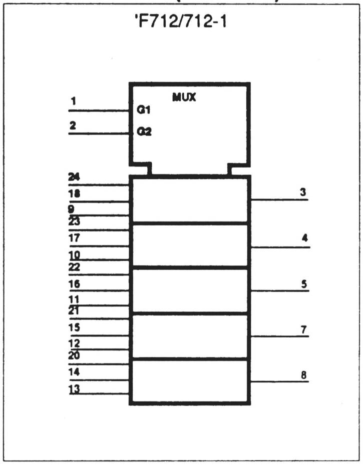

'F712/712-1
S0 1
S1 2
Q0 3
Q1 4
Q2 5
GND 6
Q3 7
Q4 8
D0c 9
D1c 10
D2c 11
D3c 12
24 D0a
23 D1a
22 D2a
21 D3a
20 D4a
19 VCC
18 D0b
17 D1b
16 D2b
15 D3b
14 D4b
13 D4c
TOP VIEW

LOGIC SYMBOL


'F712/712-1
S0
S1
Q0 Q1 Q2 Q3 Q4

V_{CC} = Pin 19
GND = Pin 16

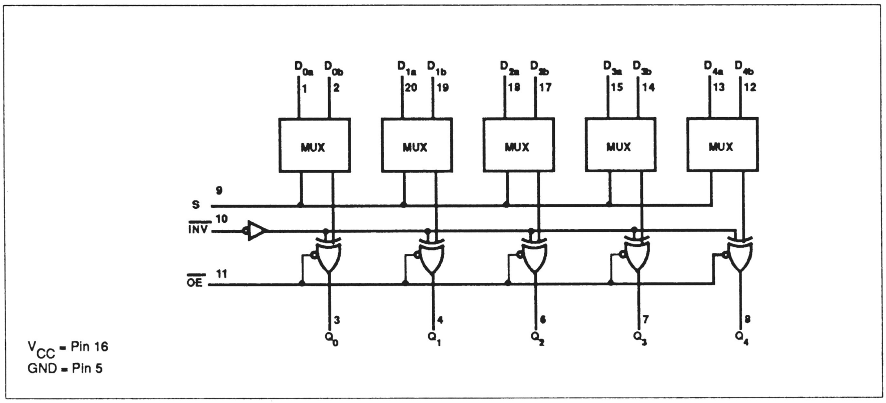
LOGIC SYMBOL(IEEE/IEC)


'F712/712-1
MUX
G1
G2

The 'F711-1 is as same as 'F711 except that it has a 30 ohm series termination resistor on each output to reduce line noise. The inverting ($\overline{INV}$) input, when Low, changes data path to inverting in To improve speed and noise immunity, multiple side pins are used by V_{CC} and GND pins. The 3-state outputs source 15mA and sink 64mA.

The 74F712/712-1 consists of four 3-to-1 multiplexers designed for address multiplexing for dynamic RAMs and other multiplexing applications. The 'F712 has two select (S_0,S_1) inputs to determine which set of five inputs will be propagated to the five outputs. The 'F712-1 is as same as 'F712 except that it has a 30 ohm series termination resistor on each output to reduce line noise. The outputs source 15mA and sink 64mA.

LOGIC DIAGRAM for 'F711/711-1


D0a D0b
D1a D1b
D2a D2b
D3a D3b
D4a D4b
MUX
S
INV
OE
Q0
Q1
Q2
Q3
Q4

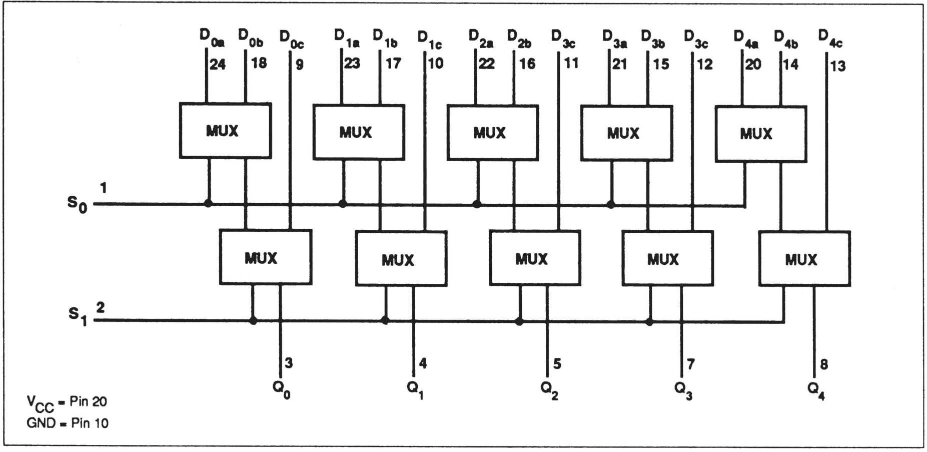
V_{CC} = Pin 16
GND = Pin 5

FUNCTION TABLE for 'F711/711-1

INPUTS					OUTPUT
S	INV	$\overline{OE}$	D_{na}	D_{nb}	Q_n
L	L	L	data a	data b	$\overline{\text{data a}}$
H	L	L	data a	data b	$\overline{\text{data b}}$
L	H	L	data a	data b	data a
H	H	L	data a	data b	data b
X	X	H	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM, 'F712/712-1



D0a 24
D0b 18
D0c 9
D1a 23
D1b 17
D1c 10
D2a 22
D2b 16
D3c 11
D3a 21
D3b 15
D3c 12
D4a 20
D4b 14
D4c 13
MUX
S0 1
S1 2
3 Q0
4 Q1
5 Q2
7 Q3
8 Q4
VCC = Pin 20
GND = Pin 10

FUNCTION TABLE for 'F712/712-1

INPUTS					OUTPUT
S_0	S_1	D_{na}	D_{nb}	D_{nc}	Q_n
L	L	data a	data b	data c	data a
X	H	data a	data b	data c	data b
H	L	data a	data b	data c	data c

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-3mA	±10%VCC	2.4			V
						±5%VCC	2.7	3.4		V
					I_{OH}=-15mA	±10%VCC	2.0			V
						±5%VCC	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=48mA	±10%VCC		0.38	0.55	V
					I_{OL}=64mA	±5%VCC		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OZH}	Off-state current High level voltage applied	'F711/711-1 only		V_{CC} = MAX, V_O= 2.7V					70	µA
I_{OZL}	Off-state current Low-level voltage applied			V_{CC} = MAX, V_O= 0.5V					-70	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F711/ 711-1	I_{CCH}	V_{CC} = MAX				12		mA
			I_{CCL}					24		mA
			I_{CCZ}					30		mA
		'F712/ 712-1	I_{CCH}					18		mA
			I_{CCL}					24		mA
			I_{CCZ}					30		mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

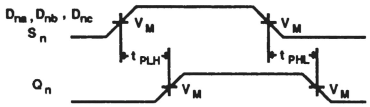
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F711/74F711-1					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to Q_n	Waveform 1, 2			6.0 6.0		7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay S, $\overline{INV}$ to Q_n	Waveform 1,3			9.5 9.5		10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_n	Waveform 4 Waveform 5			7.0 7.0		8.0 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Q_n	Waveform 4 Waveform 5			6.0 6.0		6.5 6.5	ns

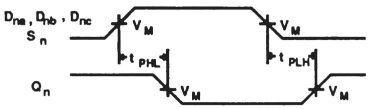
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F712/74F712-1					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc} to Q_n	Waveform 1, 2			6.0 6.0		7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to Q_n	Waveform 1			11.0 11.0		10.0 10.0	ns

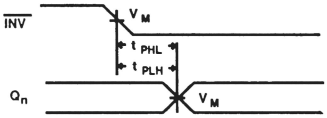
AC WAVEFORMS


D_{na}, D_{nb}, D_{nc}
S_n
V_M
V_M
t_{PLH}
t_{PHL}
Q_n
V_M
V_M

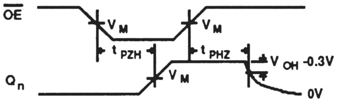
Waveform 1. Propagation Delay For Non-Inverting Output


D_{na}, D_{nb}, D_{nc}
S_n
V_M
V_M
t_{PHL}
t_{PLH}
Q_n
V_M
V_M

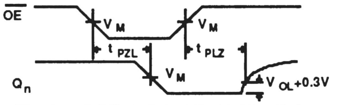
Waveform 2. Propagation Delay For Inverting Output


$\overline{INV}$
V_M
t_{PHL}
t_{PLH}
Q_n
V_M

Waveform 3. Propagation Delay For $\overline{INV}$ To Output


$\overline{OE}$
V_M
V_M
t_{PZH}
t_{PHZ}
V_{OH} -0.3V
Q_n
V_M
0V

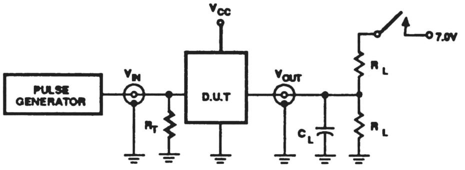
Waveform4. 3-State Output Enable Time To High Level And Output Disable Time From High Level


$\overline{OE}$
V_M
V_M
t_{PZL}
t_{PLZ}
Q_n
V_M
V_{OL}+0.3V

Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
7.0V
PULSE GENERATOR
V_{IN}
D.U.T
V_{OUT}
R_L
R_T
C_L
R_L

Test Circuit For 3-State Outputs

SWITCH POSITION

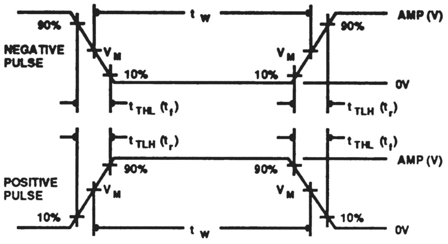
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


t_W
AMP (V)
90%
NEGATIVE PULSE
V_M
10%
0V
t_{THL} (t_f)
t_{TLH} (t_r)
POSITIVE PULSE

V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F723/723-1, 74F725/725-1

Multiplexers

74F723 Quad 3-to-1 Data Selector Multiplexer (3-State)
74F723-1 Quad 3-to-1 Data Selector Multiplexer With 30 ohm series termination resistors (3-State)
74F725 Quad 4-to-1 Data SelectorMultiplexer
74F725-1 Quad 3-to-1 Data Selector Multiplexer With 30 ohm series termination resistors

PreliminarySpecification

FEATURES for 74F723/723-1

- **Consists of four 3-to-1 Multiplexers**
- **Equivalent to three 'F157As or 'F158As**
- **Inverting or non-inverting data path capability by an inverting ($\overline{INV}$) input**
- **Designed for address multiplexing of dynamic RAM and other applications**
- **Multiple side pins for V_{CC} and GND to reduce lead inductance (improves speed and noise immunity)**
- **3-State outputs sink 64mA**
- **30 ohm output series termination resistor option-74F723-1**

FEATURES for 74F725/725-1

- **Consists of four 4-to-1 Multiplexers**
- **Equivalent to two 'F253s without 3-state**
- **Outputs sink 64mA**
- **3-State outputs sink 64mA**
- **30 ohm output series termination resistor option-74F723-1**

DESCRIPTION

The 74F723/723-1 consists of four 3-to-1 multiplexers designed for address multiplexing for dynamic RAMs and other multiplexing applications. The 'F723/723-1 can take place of four 'F157As or 'F158As. Select (S_0,S_1)inputs control which line is to be selected, as defined in the Function Table for 'F723/723-1. The inverting (INV) input,

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F723/723-1	5.5ns	28mA
74F725/725-1	6.0ns	29mA

ORDERING INFORMATION

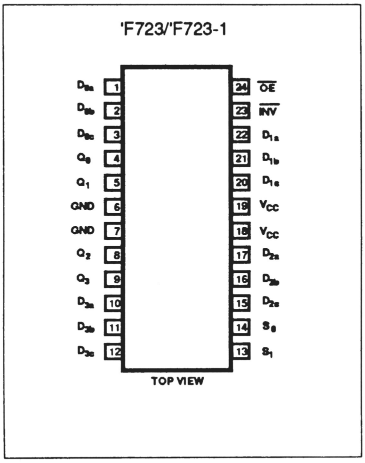
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300 mil)	N74F723N, N74F723-1N, N74F725N, N74F725-1N
24-Pin Plastic SOL	N74F723D, N74F723-1D, N74F725D, N74F725-1D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

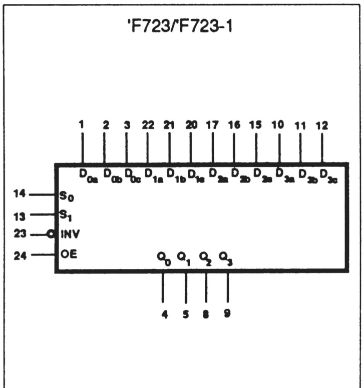
TYPE	PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F723/ 'F723-1	D_{na}, D_{nb}, D_{nc}	Data inputs	1.0/0.033	20µA/20µA
	S_0, S_1	Select inputs	1.0/0.033	20µA/20µA
	$\overline{INV}$	Output Inverting input	1.0/0.033	20µA/20µA
	$\overline{OE}$	Output Enable input	1.0/0.033	20µA/20µA
	Q_0 - Q_4	Data outputs	750/106.7	15mA/64mA
'F725/ 'F725-1	D_{na}, D_{nb}, D_{nc}, D_{nc}	Data inputs	1.0/0.033	20µA/20µA
	S_0, S_1	Select inputs	1.0/0.033	20µA/20µA
	Q_0 - Q_4	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

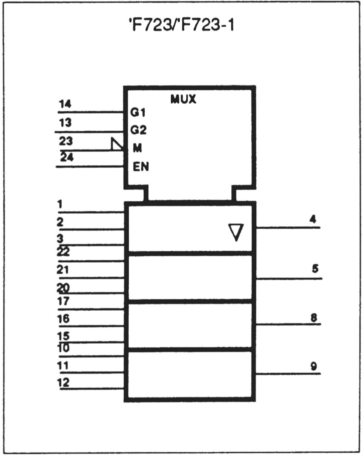

'F723/'F723-1
D0a 1
D0b 2
D0c 3
Q0 4
Q1 5
GND 6
GND 7
Q2 8
Q3 9
D3a 10
D3b 11
D3c 12
24 OE
23 INV
22 D1a
21 D1b
20 D1c
19 Vcc
18 Vcc
17 D2a
16 D2b
15 D2c
14 S0
13 S1
TOP VIEW

LOGIC SYMBOL


'F723/'F723-1
1 2 3 22 21 20 17 16 15 10 11 12
D0a D0b D0c D1a D1b D1c D2a D2b D2c D3a D3b D3c
14 S0
13 S1
23 INV
24 OE
Q0 Q1 Q2 Q3
4 5 8 9

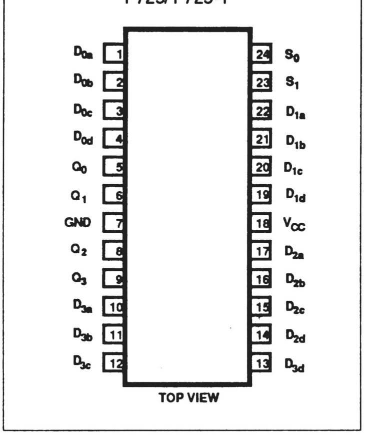
V_{CC} = Pin 18, 19
GND = Pin 6,7

LOGIC SYMBOL(IEEE/IEC)


'F723/'F723-1
MUX
14 G1
13 G2
23 M
24 EN
1
2
3
22
21
20
17
16
15
10
11
12
4
5
8
9

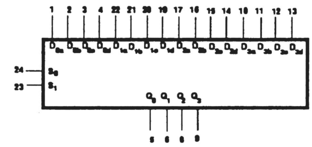
PIN CONFIGURATION

'F725/'F725-1


D0a 1
D0b 2
D0c 3
D0d 4
Q0 5
Q1 6
GND 7
Q2 8
Q3 9
D3a 10
D3b 11
D3c 12
24 S0
23 S1
22 D1a
21 D1b
20 D1c
19 D1d
18 VCC
17 D2a
16 D2b
15 D2c
14 D2d
13 D3d
TOP VIEW

LOGIC SYMBOL

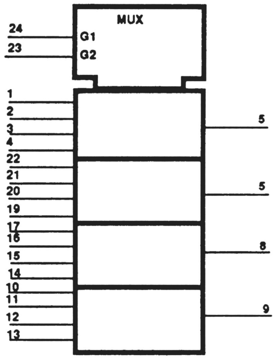
'F725/'F725-1


1 2 3 4 22 21 20 19 17 16 15 14 10 11 12 13
D0a D0b D0c D0d D1a D1b D1c D1d D2a D2b D2c D2d D3a D3b D3c D3d
24 S0
23 S1
Q0 Q1 Q2 Q3
5 6 8 9

V_{CC} = Pin 18
GND = Pin 7

LOGIC SYMBOL(IEEE/IEC)

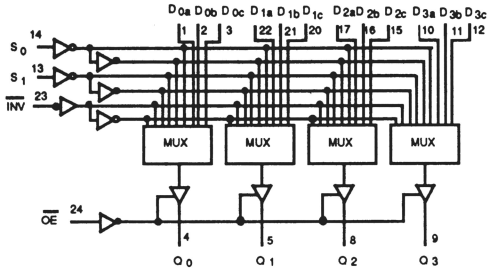
'F725/'F725-1


MUX
24
23
G1
G2
1
2
3
4
22
21
20
19
17
16
15
14
10
11
12
13
5
5
8
9

when Low, changes data path to inverting, To improve speed and noise immunity, multiple side pins are used by V_{CC} and GND pins. The 3-state outputs sink 64mA. The 74F723-1 is same as 74F723 except that it has a 30 ohm series termination resistor on each output to reduce line noise..

The 74F725/725-1 consists of four 4-to-1 multiplexers designed for general multiplexing purpose. The 'select (S_0,S_1) inputs control which line is to be selected, as defined in the Function Table for 'F725/725-1. 'F725/725-1 can take palce of two 'F257As without the 3-state function.The outputs source 15mA and sink 64mA.The 74F725-1 is as same as 74F725 except that it has a 30 ohm series termination resistor on each output to reduce line noise.

LOGIC DIAGRAM for 'F723/'F723-1


D0a D0b D0c D1a D1b D1c D2a D2b D2c D3a D3b D3c
1 2 3 22 21 20 17 16 15 10 11 12
S0 14
S1 13
INV 23
MUX
MUX
MUX
MUX
OE 24
4
5
8
9
Q0
Q1
Q2
Q3

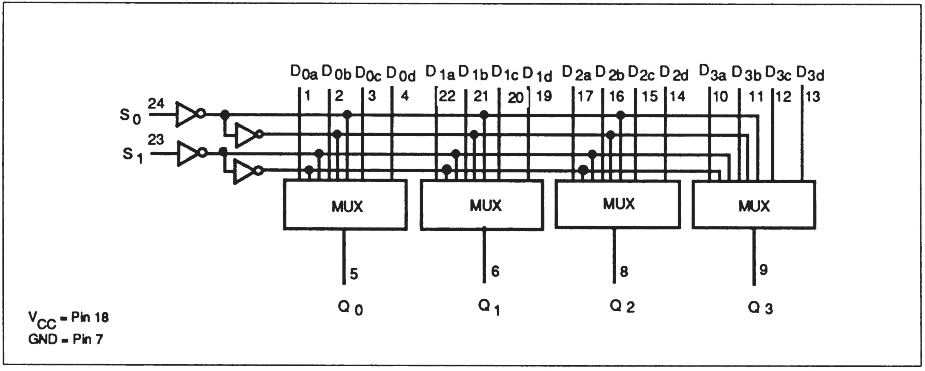
V_{CC} = Pin 18, 19
GND = Pin 6, 7

FUNCTION TABLE for 'F723/'F723-1

INPUTS							OUTPUT
S_0	S_1	$\overline{INV}$	$\overline{OE}$	D_{na}	D_{nb}	D_{nc}	Q_n
L	L	L	H	data a	data b	data c	$\overline{\text{data a}}$
L	L	H	H	data a	data b	data c	data a
H	L	L	H	data a	data b	data c	$\overline{\text{data b}}$
H	L	H	H	data a	data b	data c	data b
X	H	L	H	data a	data b	data c	$\overline{\text{data c}}$
X	H	H	H	data a	data b	data c	data c
X	X	X	X	X	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM, 'F725/'F725-1


D0a D0b D0c D0d D1a D1b D1c D1d D2a D2b D2c D2d D3a D3b D3c D3d
1 2 3 4 22 21 20 19 17 16 15 14 10 11 12 13
S0 24
S1 23
MUX
MUX
MUX
MUX
5 6 8 9
Q0 Q1 Q2 Q3
VCC = Pin 18
GND = Pin 7

FUNCTION TABLE for 'F725/'F725-1

INPUTS						OUTPUT
S_0	S_1	D_{na}	D_{nb}	D_{nc}	D_{nd}	Q_n
L	L	data a	data b	data c	data d	data a
H	L	data a	data b	data c	data d	data b
L	H	data a	data b	data c	data d	data c
H	H	data a	data b	data c	data d	data d

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-3mA	±10%VCC	2.4			V
						±5%VCC	2.7	3.4		V
					I_{OH}=-15mA	±10%VCC	2.0			V
						±5%VCC	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=48mA	±10%VCC		0.38	0.55	V
					I_{OL}=64mA	±5%VCC		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} =MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-20	μA
I_{OZH}	Off-state current High level voltage applied	'F723/723-1 only		V_{CC} = MAX, V_O= 2.7V					50	μA
I_{OZL}	Off-state current Low-level voltage applied			V_{CC} = MAX, V_O= 0.5V					-50	μA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F723/ 723-1	I_{CCH}	V_{CC} = MAX				28		mA
			I_{CCL}					26		mA
			I_{CCZ}					30		mA
		'F725/ 725-1	I_{CCH}					29		mA
			I_{CCL}					28		mA
			I_{CCZ}					30		mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

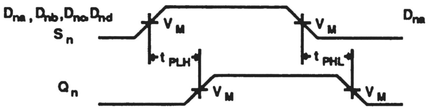
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F723/74F723-1					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc} to Q_n	Waveform 1, 2			6.0 6.0		7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 $\overline{INV}$ to Q_n	Waveform 1, 3			9.5 9.5		10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_n	Waveform 4 Waveform 5			7.0 7.0		8.0 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Q_n	Waveform 4 Waveform 5			6.0 6.0		6.5 6.5	ns

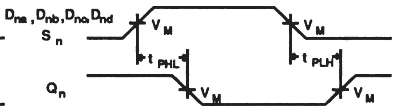
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F725/74F725-1					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc}, D_{nd} to Q_n	Waveform 1, 2			6.0 6.0		7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to Q_n	Waveform 1			11.0 11.0		10.0 10.0	ns

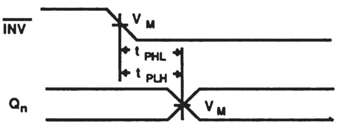
AC WAVEFORMS


Dna, Dnb, Dnc, Dnd
Sn
VM
VM
tPLH
tPHL
Qn
VM
VM

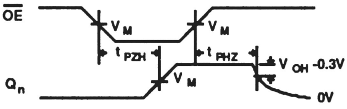
Waveform 1. Propagation Delay For Non-Inverting Output


Dna, Dnb, Dnc, Dnd
Sn
VM
VM
tPHL
tPLH
Qn
VM
VM

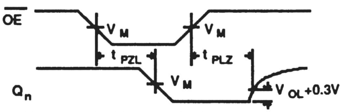
Waveform 2. Propagation Delay For Inverting Output


INV
VM
tPHL
tPLH
Qn
VM

Waveform 3. Propagation Delay For $\overline{INV}$ To Output


OE
VM
VM
tPZH
tPHZ
VOH -0.3V
Qn
VM
0V

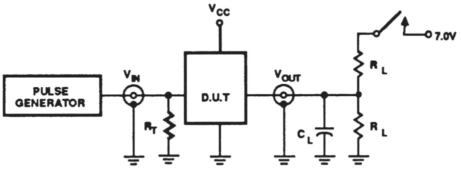
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level


OE
VM
VM
tPZL
tPLZ
Qn
VM
VOL+0.3V

Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS


V_CC
7.0V
PULSE GENERATOR
V_IN
R_T
D.U.T
V_OUT
C_L
R_L
R_L

Test Circuit For 3-State Outputs

SWITCH POSITION

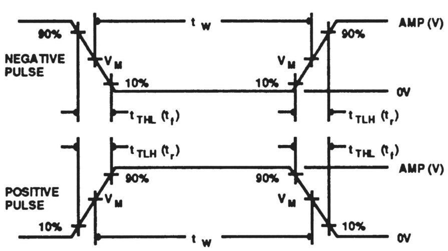
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


t_W
90%
AMP (V)
NEGATIVE PULSE
V_M
V_M
10%
10%
0V
t_THL (t_f)
t_TLH (t_r)
t_TLH (t_r)
t_THL (t_f)
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
0V
t_W

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

74F728
FLIP-FLOP

Synchronizing Cascaded Dual D-Type Flip-Flop

Preliminary Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F728	200 MHz	10mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F728N
14-Pin Plastic SO	N74F728D

FEATURES

- **Metastable Immune Characteristics**
- **See 74F74A for Synchronizing Dual D-Type Flip-Flop**
- **See 74F109A for Synchronizing Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop**
- **See 74F729 for Synchronizing Cascaded Dual D-Type Flip-Flop with Edge-Triggered Set and Reset**

DESCRIPTION

The 74F728 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also true and complementary outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-Low inputs and operate independently of the Clock (CP) input. They set and reset both flip-flops of a cascaded pair simultaneously. Data must be stable just one setup time prior to the Low-to-High transition of the clock for guaranteed propagation delays.

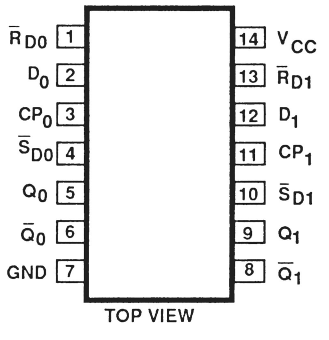
Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D input may be changed without affecting the levels of the output. Data entering the 'F728 requires two clock cycles to arrive at the outputs. The 'F728 is designed so that the outputs can never display a metastable state due to setup and hold times violations. If setup and hold times are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F728 are: $\tau < .100$ns, T_0=1µs, and h=3.3ns. Estimated Mean TIme Between Failures on the output flops with data and clock at 100 MHz (failures being any extension of the propagation delays is ~1.55X 10^{26} seconds or ~5X10^{18} years).

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

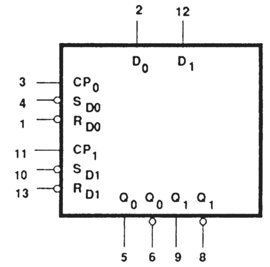
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0, D_1	Data inputs	1.0/0.166	20µA/100µA
CP_0, CP_1	Clock inputs (active rising edge)	1.0/0.083	20µA/50µA
$\overline{S}_{D0}$, $\overline{S}_{DI}$	Set inputs (active Low)	1.0/0.083	20µA/50µA
$\overline{R}_{D0}$, $\overline{R}_{DI}$	Reset inputs (active Low)	1.0/0.083	20µA/50µA
Q_0, Q_I, $\overline{Q}_0$, $\overline{Q}_I$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

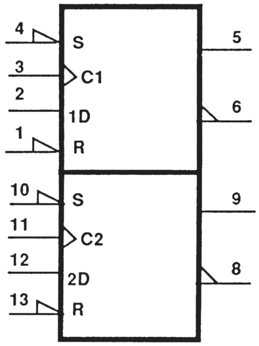


LOGIC SYMBOL

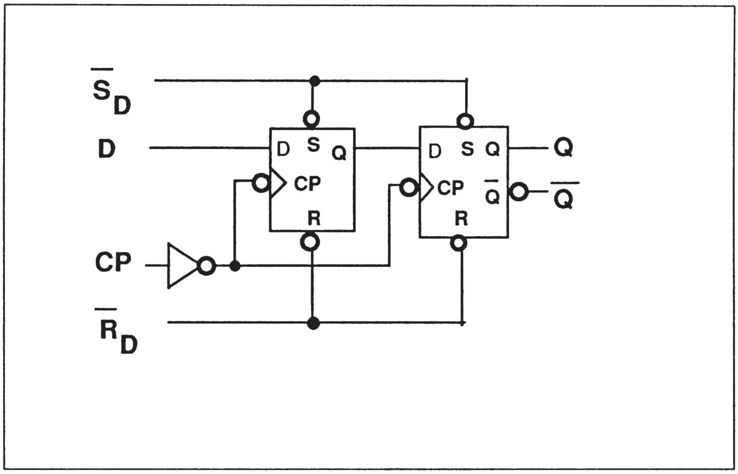


V_{CC} =pin 14
GND =pin 7

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q+n	Q	
L	H	X	X	H	H	Asynchronous Set
H	L	X	X	L	L	Asynchronous Reset
L	L	X	X	H	H	Undetermined*
H	H	↑	h	H	Q_{n-1}	Load "1"
H	H	↑	l	L	Q_{n-1}	Load "0"
H	H	L	X	NC	NC	Hold

H = High voltage level
h-= High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
NC =No change from the previous setup
* = The output in this configuration is not guaranteed to meet the minimum V_{OH} levels when Set and Reset are near V_{IL} maximum. Also, this setup is unstable and will change when either Set or Reset return to the High level.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} =MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} =MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	D_n	V_{CC} = MAX, V_I = 0.5V					-100	μA
		CP_n, $\overline{S}_{Dn}$, $\overline{R}_{Dn}$						-50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				10	16	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs High in turn.

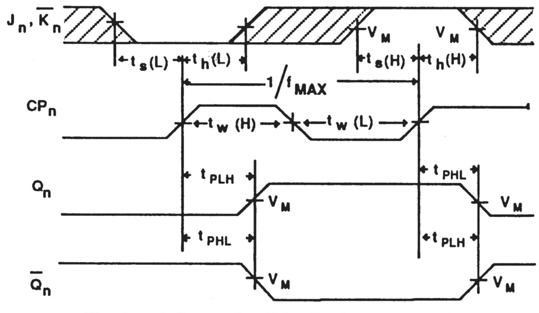
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1		200		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveform 1	2.0 2.0	2.9 3.3	4.5 5.0	2.0 2.0	5.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$, $\overline{R}_{Dn}$ to Q_n or $\overline{Q}_n$	Waveform 2	2.0 2.0	2.8 3.3	4.5 5.0	2.0 2.0	5.5 6.0	ns

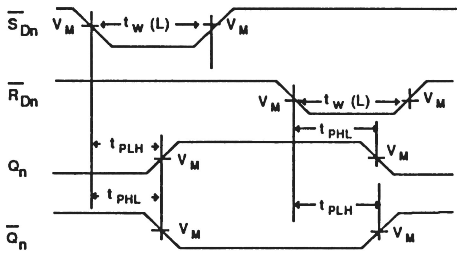
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 1	1.0 1.0			1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 1	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	$\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ Pulse width, Low	Waveform 2	4.0			4.0		ns
t_{rec}	Recovery time $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to CP	Waveform 3	2.0			2.0		ns

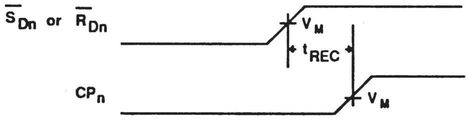
AC WAVEFORMS


$J_n, \overline{K}_n$
$t_s(L)$
$t_h(L)$
$t_s(H)$
$t_h(H)$
V_M
$1/f_{MAX}$
CP_n
$t_w(H)$
$t_w(L)$
Q_n
t_{PLH}
t_{PHL}
$\overline{Q}_n$

Waveform 1. Propagation Delay For data to output, data setup time and hold times, and clock width


$\overline{S}_{Dn}$
V_M
$t_w(L)$
$\overline{R}_{Dn}$
t_{PHL}
t_{PLH}
Q_n
$\overline{Q}_n$

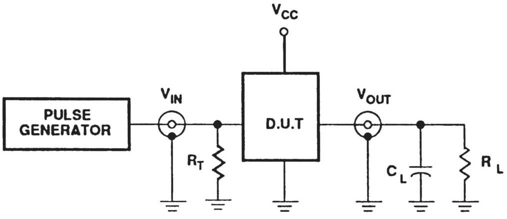
Waveform 2.
Propagation Delay for set and reset to output, set and reset pulse width


$\overline{S}_{Dn}$ or $\overline{R}_{Dn}$
V_M
t_{REC}
CP_n

Waveform 3.
Recovery time for set or reset to clock

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
R_T
D.U.T
V_{OUT}
C_L
R_L

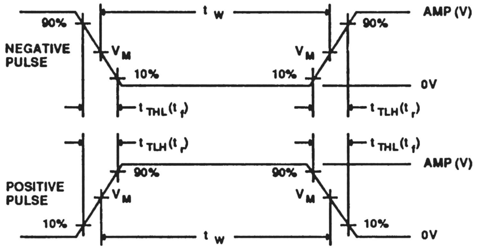
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
V_M
t_w
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
AMP (V)
0V

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F729
FLIP-FLOP

Synchronizing Dual D-Type Flip-Flop With Edge triggered Set and Reset

FEATURES

- **Metastable Immune Characteristics**
- **See 74F74A for Synchronizing Dual D-Type Flip-Flop**
- **See 74F109A for Synchronizing Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop**
- **See 74F728 for Synchronizing Cascaded Dual D-Type Flip-Flop**

DESCRIPTION

The 74F729 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also true and complementary outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous positive-edge triggered inputs and operate independently of the Clock (CP) input. Data must be stable just one setup time prior to the Low-to-High transition of the clock for guaranteed propagation delays.

Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D input may be changed without affecting the levels of the output.

The'F729 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup and hold times are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F729 are: $\tau<100$ns, $T_0=0.1\mu$s, and h=3.3ns.

Preliminary Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F729	200 MHz	10mA

ORDERING INFORMATION

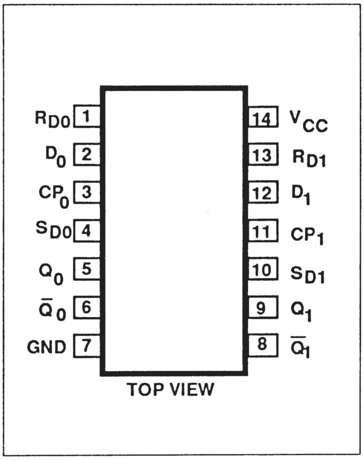
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F729N
14-Pin Plastic SO	N74F729D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

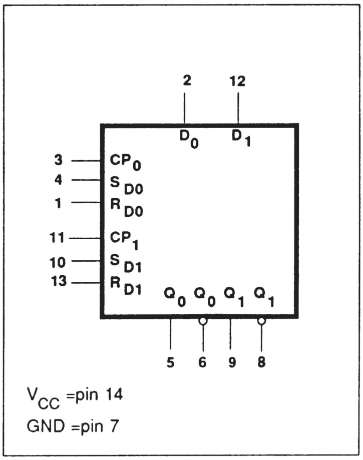
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0, D_1	Data inputs	1.0/0.166	20μA/100μA
CP_0, CP_1	Clock inputs (active rising edge)	1.0/0.083	20μA/50μA
S_{D0}, S_{D1}	Set inputs (active rising edge)	1.0/0.083	20μA/50μA
R_{D0}, R_{D1}	Reset inputs (active rising edge)	1.0/0.083	20μA/50μA
Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

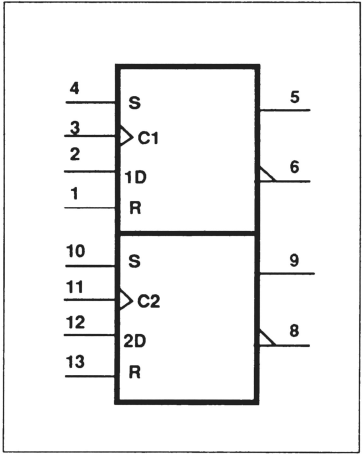


LOGIC SYMBOL

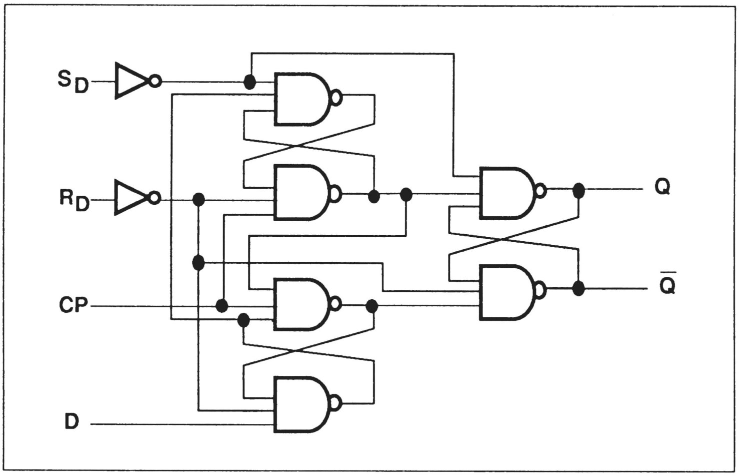


V_{CC} =pin 14
GND =pin 7

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
S_D	R_D	CP	D	Q	$\overline{Q}$	
↑	$\not\uparrow$	X	X	H	L	Asynchronous Set
$\not\uparrow$	↑	X	X	L	H	Asynchronous Reset
$\not\uparrow$	$\not\uparrow$	↑	h	H	L	Load "1"
$\not\uparrow$	$\not\uparrow$	↑	l	L	H	Load "0"
$\not\uparrow$	$\not\uparrow$	$\not\uparrow$	X	NC	NC	Hold

H = High voltage level
h-= High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
X = Don't care
↑ = Low-to-High transition
NC =No change from the previous setup
$\not\uparrow$ = Not Low-to-High transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} =MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} =MAX V_{IH} = MIN	±10%V_{CC}		0.30	0.50	V
				±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	D_n	V_{CC} = MAX, V_I = 0.5V				-100	µA
		CP_n, S_{Dn}, R_{Dn}					-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			10	16	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs High in turn.

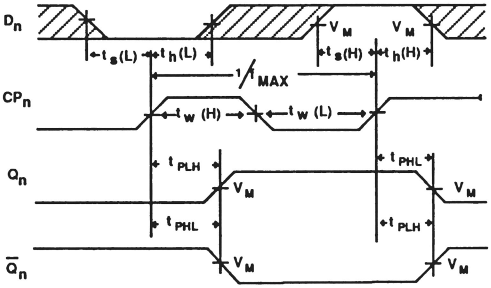
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1		200				MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveform 1	2.0 2.0	2.9 3.3	4.5 5.0	2.0 2.0	5.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveform 2	2.0 2.0	2.8 3.3	4.5 5.0	2.0 2.0	5.5 6.0	ns

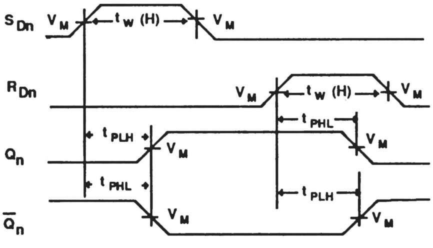
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 1	1.0 1.0			1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 1	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(H)$	S_{Dn} or R_{Dn} Pulse width, High	Waveform 2	4.0			4.0		ns
t_{REC}	Recovery time S_{Dn} or R_{Dn} to CP	Waveform 3	2.0			2.0		ns
t_{REC}	Recovery time S_{Dn} to R_{Dn} or R_{Dn} to S_{Dn}	Waveform 3	2.0			2.0		ns

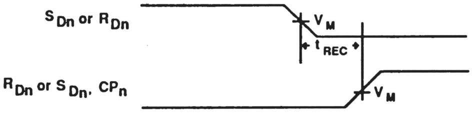
AC WAVEFORMS


D_n
CP_n
Q_n
$\overline{Q}_n$
t_s(L)
t_h(L)
t_s(H)
t_h(H)
1/f_MAX
V_M
t_w (H)
t_w (L)
t_PLH
t_PHL

Waveform 1. Propagation Delay For data to output, data setup time and hold times, and clock width


S_Dn
R_Dn
Q_n
$\overline{Q}_n$
V_M
t_w (H)
t_PLH
t_PHL

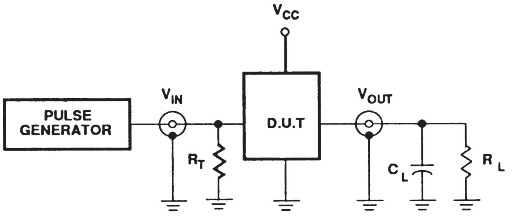
Waveform 2.
Propagation Delay for set and reset to output, set and reset pulse width


S_Dn or R_Dn
R_Dn or S_Dn, CP_n
V_M
t_REC

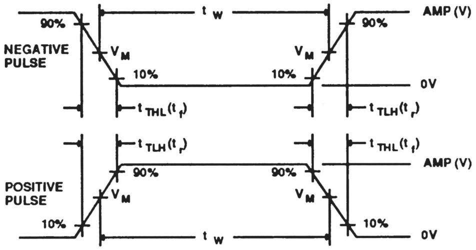
Waveform 3.
Recovery time for set or reset to clock and set to reset or reset to set

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_CC
PULSE GENERATOR
V_IN
R_T
D.U.T
V_OUT
C_L
R_L

Test Circuit For Totem-Pole Outputs


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
V_M
t_w
AMP (V)
0V
t_THL(t_f)
t_TLH(t_r)

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F732, 74F733

Multiplexers

74F732 Quad Data Multiplexer, Inverting (3-State)
74F733 Quad Data Multiplexer, Non-Inverting (3-State)
Product Specification

FEATURES

- **Quad 2-to-1 Multiplexer (two busses to one bus)**
- **Data can flow in either direction between busses (A → B, A → C, B → C, B → A, C → A, C → B)**
- **A built-in "break-before-make" feature eliminates current glitches and simplifies PC board design**
- **Output Enable for each bus to allow flexible contention control**
- **3-State outputs sink 64mA**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F732	6.0ns	65mA
74F733	6.0ns	75mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F732N, N74F733N
20-Pin Plastic SOL	N74F732D, N74F733D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_3$	Data inputs for Bus A	3.5/1.0	70μA/0.6mA
$B_0 - B_3$	Data inputs for Bus B	3.5/1.0	70μA/0.6mA
$C_0 - C_3$	Data inputs for Bus C	3.5/1.0	70μA/0.6mA
DIR	Direction control input	1.0/1.0	20 A/0.6mA
$S_0 - S_1$	Select inputs	1.0/1.0	20μA/0.6mA
$\overline{OEA}$, $\overline{OEB}$ $\overline{OEC}$	Output Enable inputs (Active Low)	1.0/1.0	20μA/0.6mA
$A_0 - A_3$	Data output for Bus A	750/106.7	15mA/64mA
$B_0 - B_3$	Data output for Bus B	750/106.7	15mA/64mA
$C_0 - C_3$	Data output for Bus C	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

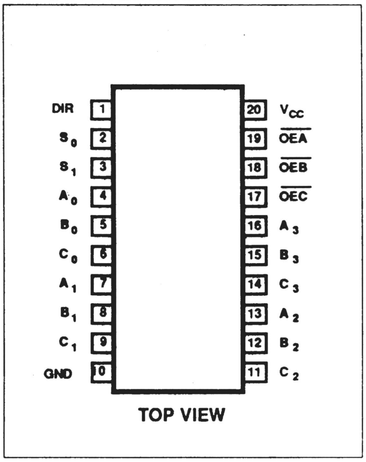
DESCRIPTION

The 74F732/74F733 are Quad Data Multiplexers designed to provide a simple means to control the flow of bidirectional data between three data busses.

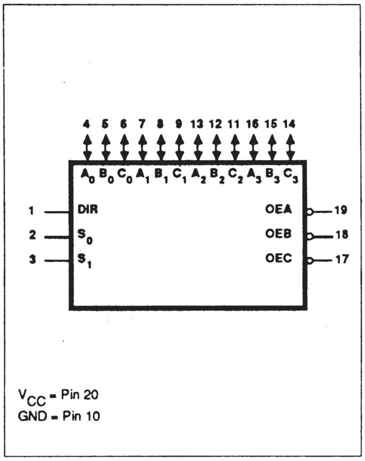
The 74F732/74F733 consist of four multiplexers. Each multiplexer has three I/O (A_n, B_n, C_n) pins and uses one Output Enable pin ($\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$). There are two Select (S_0, S_1) pins and a Direction (DIR) pin to control data flow paths for all four multiplexers.

With the Select control, data can flow in the following directions between busses: A to B, A to C, B to A, B to C, C to B, A to B and C. A built-in "break-before-make" feature eliminates current glitches common to systems using 3-State transceivers to accomplish the same function.

PIN CONFIGURATION

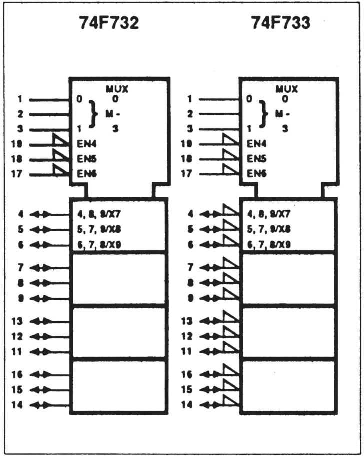

DIR 1
S_0 2
S_1 3
A_0 4
B_0 5
C_0 6
A_1 7
B_1 8
C_1 9
GND 10
11 C_2
12 B_2
13 A_2
14 C_3
15 B_3
16 A_3
17 $\overline{OEC}$
18 $\overline{OEB}$
19 $\overline{OEA}$
20 V_{CC}
TOP VIEW

LOGIC SYMBOL

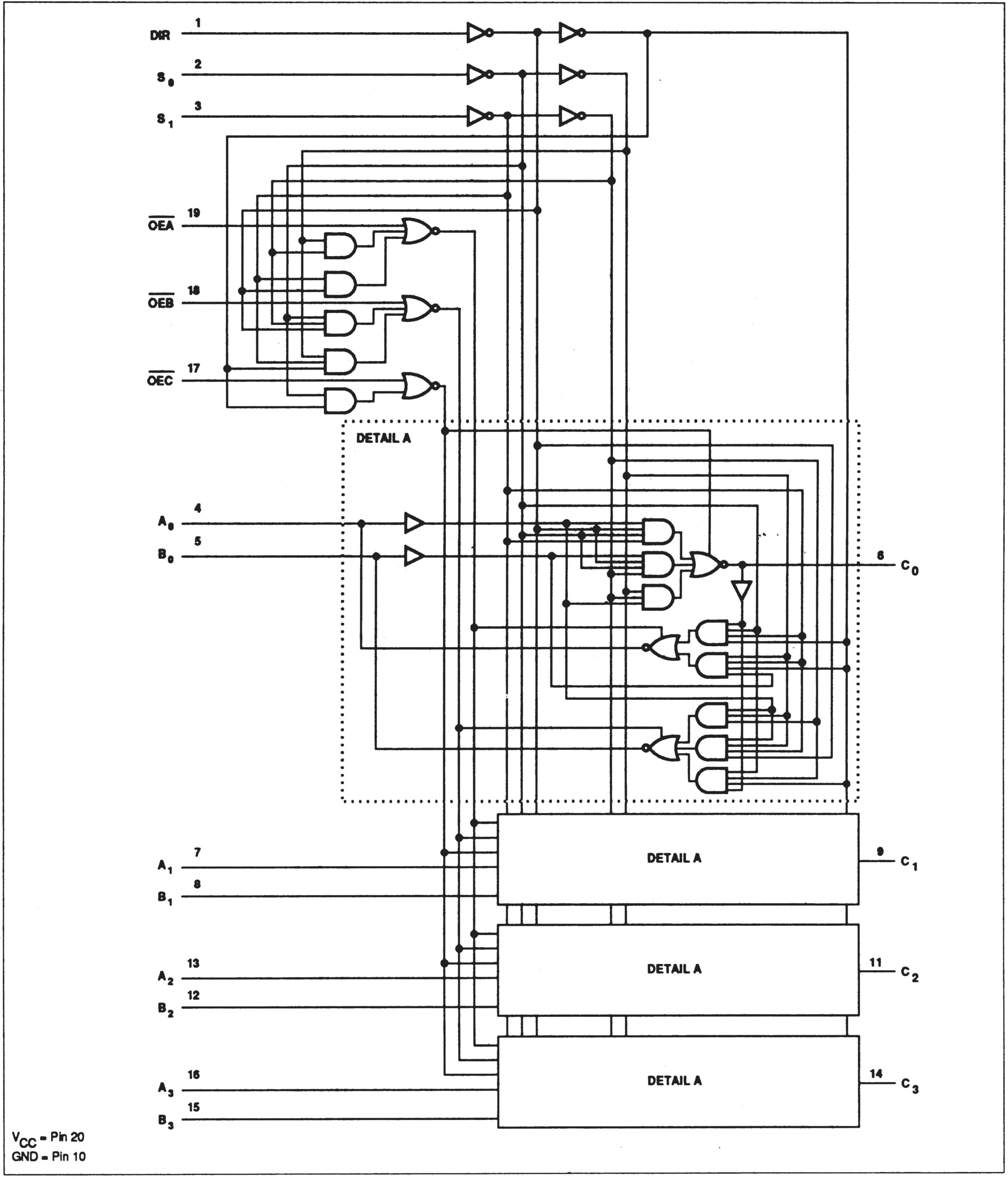

4 5 6 7 8 9 13 12 11 16 15 14
A_0 B_0 C_0 A_1 B_1 C_1 A_2 B_2 C_2 A_3 B_3 C_3
1 DIR
2 S_0
3 S_1
OEA 19
OEB 18
OEC 17

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)

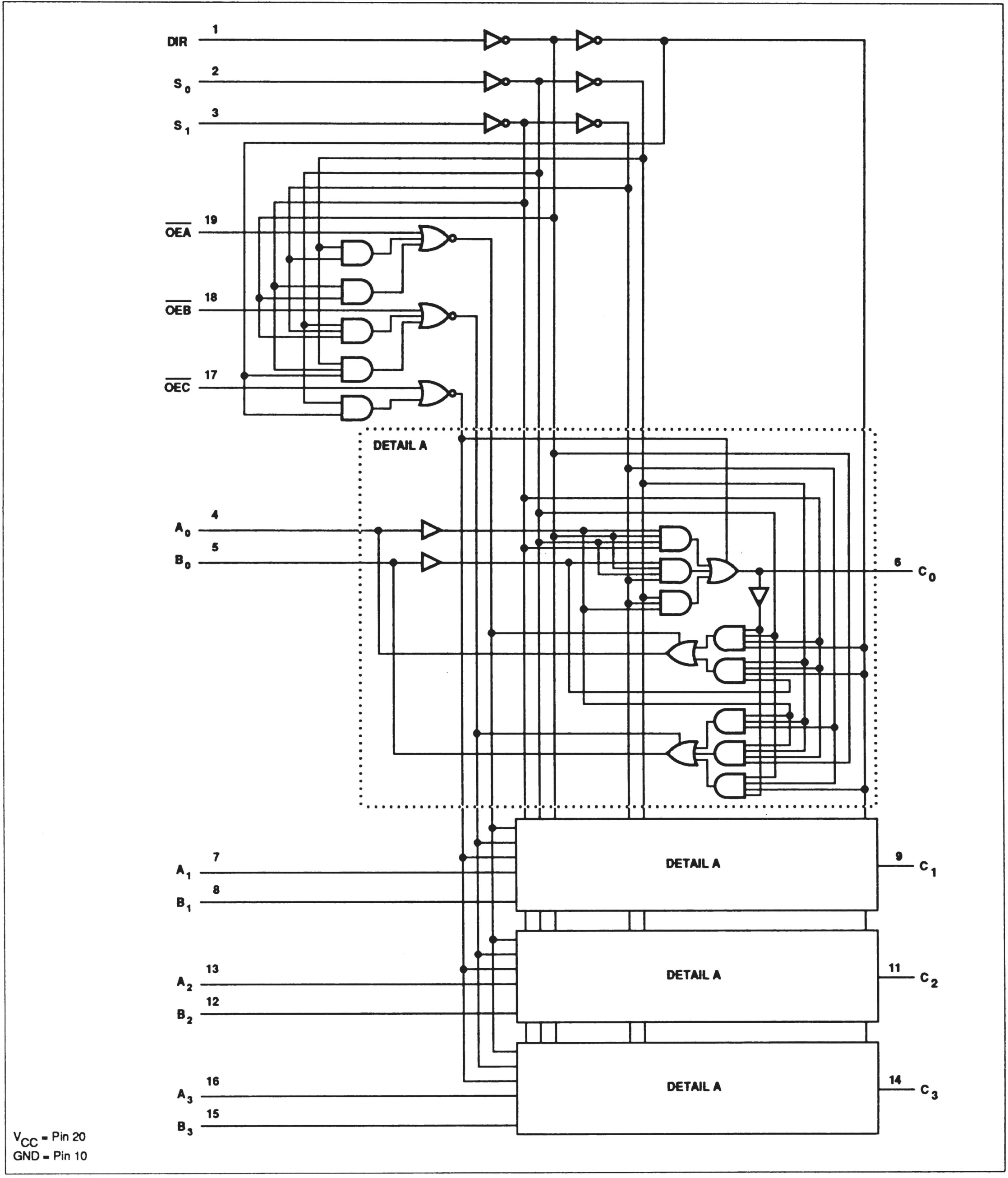

74F732
74F733
MUX
0
0
M-
1
3
EN4
EN5
EN6
4, 8, 9/X7
5, 7, 9/X8
6, 7, 8/X9
1
2
3
19
18
17
4
5
6
7
8
9
13
12
11
16
15
14

LOGIC DIAGRAM, 74F732


DIR
1
S0
2
S1
3
OEA
19
OEB
18
OEC
17
DETAIL A
A0
4
B0
5
6
C0
A1
7
B1
8
DETAIL A
9
C1
A2
13
B2
12
DETAIL A
11
C2
A3
16
B3
15
DETAIL A
14
C3

V_{CC} = Pin 20
GND = Pin 10

LOGIC DIAGRAM, 74F733


DIR
1
S0
2
S1
3
OEA
19
OEB
18
OEC
17
DETAIL A
A0
4
B0
5
6
C0
A1
7
B1
8
DETAIL A
9
C1
A2
13
B2
12
DETAIL A
11
C2
A3
16
B3
15
DETAIL A
14
C3
VCC = Pin 20
GND = Pin 10

FUNCTION TABLE

INPUTS						OPERATING MODE
DIR	S_0	S_1	$\overline{OEA}$	$\overline{OEB}$	$\overline{OEC}$	
X	X	X	H	X	X	Bus A disabled except for input
X	X	X	X	H	X	Bus B disabled except for input
X	X	X	X	X	H	Bus C disabled except for input
L	L	L	X	H*	L	Data flow from Bus A to Bus C
H	L	L	L	H*	X	Data flow from Bus C to Bus A
L	L	H	H*	X	L	Data flow from Bus B to Bus C
H	L	H	H*	L	X	Data flow from Bus C to Bus B
L	H	L	X	L	H*	Data flow from Bus A to Bus B
H	H	L	L	X	H*	Data flow from Bus B to Bus A
X	H	H	X	L	L	Data flow from Bus A to Bus B and Bus C
X	H	H	X	H	L	Data flow from Bus A to Bus C
X	H	H	X	L	H	Data flow from Bus A to Bus B

H = High voltage level
L = Low voltage level
X = Don't care
* = If this is not High then the corresponding outputs will be High (74F732) or Low (74F733)

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OH} = -3mA	±10% V_{CC}	2.4			V
						±5% V_{CC}	2.7	3.4		V
					I_{OH} = -15mA	±10% V_{CC}	2.0			V
						±5% V_{CC}	2.0	3.1		V
V_{OL}	Low-level output voltage			V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OL} = 48mA	±10% V_{CC}		0.38	0.55	V
					I_{OL} = 64mA	±5% V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current	$\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ DIR, S_0, S_1		V_{CC} = MAX, V_I = 2.7 V					20	μA
I_{IL}	Low-level input current	$\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ DIR, S_0, S_1		V_{CC} = MAX, V_I = 0.5 V					-0.6	mA
$I_{OZH} + I_{IH}$	Off-state output current, High-level voltage applied	A_0 - A_3 B_0 - B_3 C_0 - C_3		V_{CC} = MAX, V_O = 2.7V					70	μA
$I_{OZL} + I_{IL}$	Off-state output current, Low-level voltage applied	A_0 - A_3 B_0 - B_3 C_0 - C_3		V_{CC} = MAX, V_O = 0.5V					-0.6	mA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	74F732	I_{CCH}	V_{CC} = MAX				55	80	mA
			I_{CCL}					75	105	mA
			I_{CCZ}					65	100	mA
		74F733	I_{CCH}	V_{CC} = MAX				70	100	mA
			I_{CCL}					80	115	mA
			I_{CCZ}					80	110	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

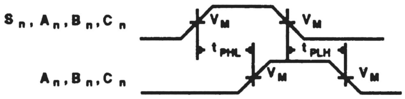
SYMBOL	PARAMETER	TEST CONDITION	74F732					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay A_n, B_n, C_n to A_n, B_n, C_n	Waveform 1, 2	2.0	4.5	8.0	2.0	8.5	ns
t_{PHL}			1.0	3.0	6.0	1.0	6.5	
t_{PLH}	Propagation delay S_0, S_1 to A_n, B_n, C_n (NINV)	Waveform 1	4.5	7.0	10.0	4.0	11.5	ns
t_{PHL}			4.5	7.0	10.0	4.0	12.0	
t_{PLH}	Propagation delay S_0, S_1 to A_n, B_n, C_n (INV)	Waveform 2	5.0	7.0	10.0	4.5	10.5	ns
t_{PHL}			2.5	4.5	7.5	2.5	8.0	
t_{PZH}	Output Enable time from $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3	2.0	4.5	7.5	1.5	8.5	ns
t_{PZL}		Waveform 4	4.0	6.5	9.5	3.5	10.0	
t_{PHZ}	Output Disable time from $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3	2.0	4.0	7.0	1.5	7.5	ns
t_{PLZ}		Waveform 4	2.0	4.0	7.0	2.0	7.5	
t_{PZH}	Output Enable time from DIR, S_0, S_1 to A_n, B_n, C_n	Waveform 3	4.0	7.5	11.0	3.0	13.5	ns
t_{PZL}		Waveform 4	5.5	8.5	11.5	5.0	13.5	
t_{PHZ}	Output Disable time from DIR, S_0, S_1 to A_n, B_n, C_n	Waveform 3	1.0	6.0	9.0	1.0	10.0	ns
t_{PLZ}		Waveform 4	1.0	4.5	7.5	1.0	8.0	

AC ELECTRICAL CHARACTERISTICS

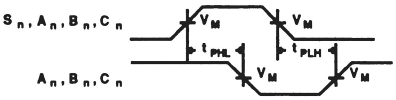
SYMBOL	PARAMETER	TEST CONDITION	74F733					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay A_n, B_n, C_n to A_n, B_n, C_n	Waveform 1, 2	1.5	4.0	7.0	1.0	7.5	ns
t_{PHL}			1.5	4.0	7.0	1.0	7.5	
t_{PLH}	Propagation delay S_0, S_1 to A_n, B_n, C_n (NINV)	Waveform 1	3.0	5.0	7.5	2.5	8.5	ns
t_{PHL}			4.0	6.0	9.0	3.5	9.5	
t_{PLH}	Propagation delay S_0, S_1 to A_n, B_n, C_n (INV)	Waveform 2	5.0	7.5	10.5	4.5	13.5	ns
t_{PHL}			3.0	5.0	8.0	3.0	8.5	
t_{PZH}	Output Enable time from $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3	2.5	5.0	7.5	2.0	8.5	ns
t_{PZL}		Waveform 4	3.5	5.5	8.5	3.0	9.0	
t_{PHZ}	Output Disable time from $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3	2.0	4.0	7.0	1.5	7.5	ns
t_{PLZ}		Waveform 4	2.0	4.5	7.0	2.0	7.5	
t_{PZH}	Output Enable time from DIR, S_0, S_1 to A_n, B_n, C_n	Waveform 3	4.5	7.5	11.0	4.0	13.0	ns
t_{PZL}		Waveform 4	5.5	8.5	12.0	5.0	13.5	
t_{PHZ}	Output Disable time from DIR, S_0, S_1 to A_n, B_n, C_n	Waveform 3	1.5	4.5	7.5	1.0	8.0	ns
t_{PLZ}*		Waveform 4	7.0	11.5	14.5	7.0	16.0	

* Because of the 3-state output characteristics, the pick-off point is V_{OL} +0.8V.

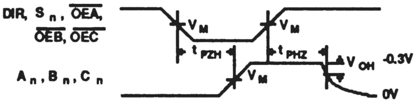
AC WAVEFORMS


S n , A n , B n , C n
A n , B n , C n
V M
t PHL
t PLH

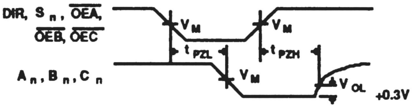
Waveform 1. Propagation Delay, Select And Data Busses


S n , A n , B n , C n
A n , B n , C n
V M
t PHL
t PLH

Waveform 2. Propagation Delay, Select And Data Busses


DIR, S n , OEA, OEB, OEC
A n , B n , C n
V M
t PZH
t PHZ
V OH -0.3V
0V

Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level

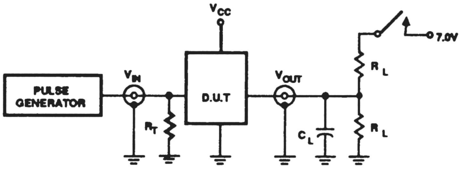

DIR, S n , OEA, OEB, OEC
A n , B n , C n
V M
t PZL
t PZH
V OL
+0.3V

Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

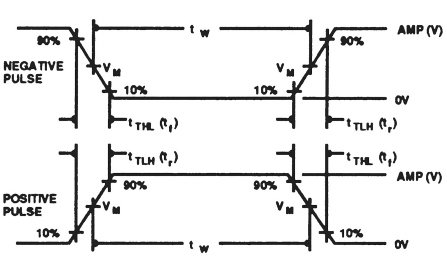
NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V CC
7.0V
R L
PULSE GENERATOR
V IN
R T
D.U.T
V OUT
C L
R L

Test Circuit For 3-State Outputs


t w
AMP (V)
90%
NEGATIVE PULSE
V M
10%
0V
t THL (t f)
t TLH (t r)
POSITIVE PULSE
90%
10%

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F739
Shift Register

8-Bit Shift Register With Multiplexed Inputs
Preliminary Specification

FEATURES

- **8-bit shift register with multiplexed inputs**
- **Facilitates parallel to serial conversion from two sources**
- **Slim DIP 300 MIL package**

DESCRIPTION

The 74F739 is an 8-bit Shift Register With Multiplexed Inputs. The shift register is an 8-bit parallel/serial in /serial out shift register. The multiplexed inputs consist of eight 2-input multiplexers with outputs internally connected to the 8-bit shift regsiter. The shift register will shift right on each Low-to-High transition of the CLock (CP) input when Clock Enable ($\overline{CE}$) input is Low and Parallel Enable ($\overline{PE}$) input is High. When $\overline{PE}$ input is Low, then the shift is inhibited and a byte on one of the two sets of inputs can be loaded into the shift register on each Low-to-High transition of the CP input regardless of the state of the $\overline{CE}$. If the Select (S) input is Low, then the D_{0a}-D_{7a} set of input will be selected for loading, and if the S input is High, the D_{0b}-D_{7b} set will be selected. When the $\overline{PE}$ input and $\overline{CE}$ input are both are High, the shift register will hold the data.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F739	130 MHz	45mA

ORDERING INFORMATION

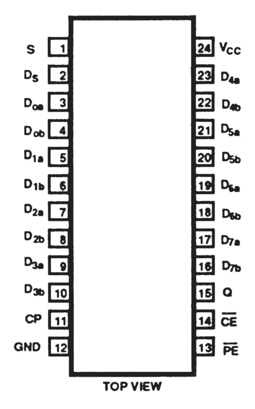
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim Dip (300 mil)	N74F739N
24-Pin Plastic SOL	N74F739D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

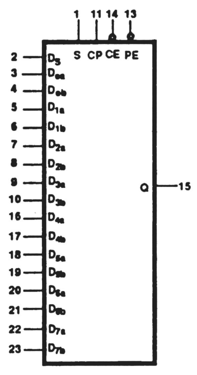
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_n	Data inputs	1.0/1.0	20μA/0.6mA
CP	Clock input	1.0/1.0	20 A/0.6mA
$\overline{CE}$	Clock Enable input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/1.0	20μA/0.6mA
S	Select input	1.0/1.0	20 A/0.6mA
Q	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

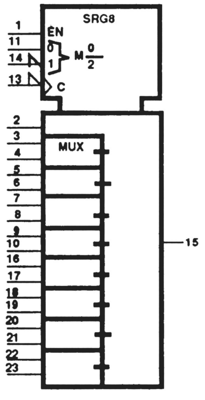

S 1
D_S 2
D_{0a} 3
D_{0b} 4
D_{1a} 5
D_{1b} 6
D_{2a} 7
D_{2b} 8
D_{3a} 9
D_{3b} 10
CP 11
GND 12
24 V_{CC}
23 D_{4a}
22 D_{4b}
21 D_{5a}
20 D_{5b}
19 D_{6a}
18 D_{6b}
17 D_{7a}
16 D_{7b}
15 Q
14 $\overline{CE}$
13 $\overline{PE}$
TOP VIEW

LOGIC SYMBOL

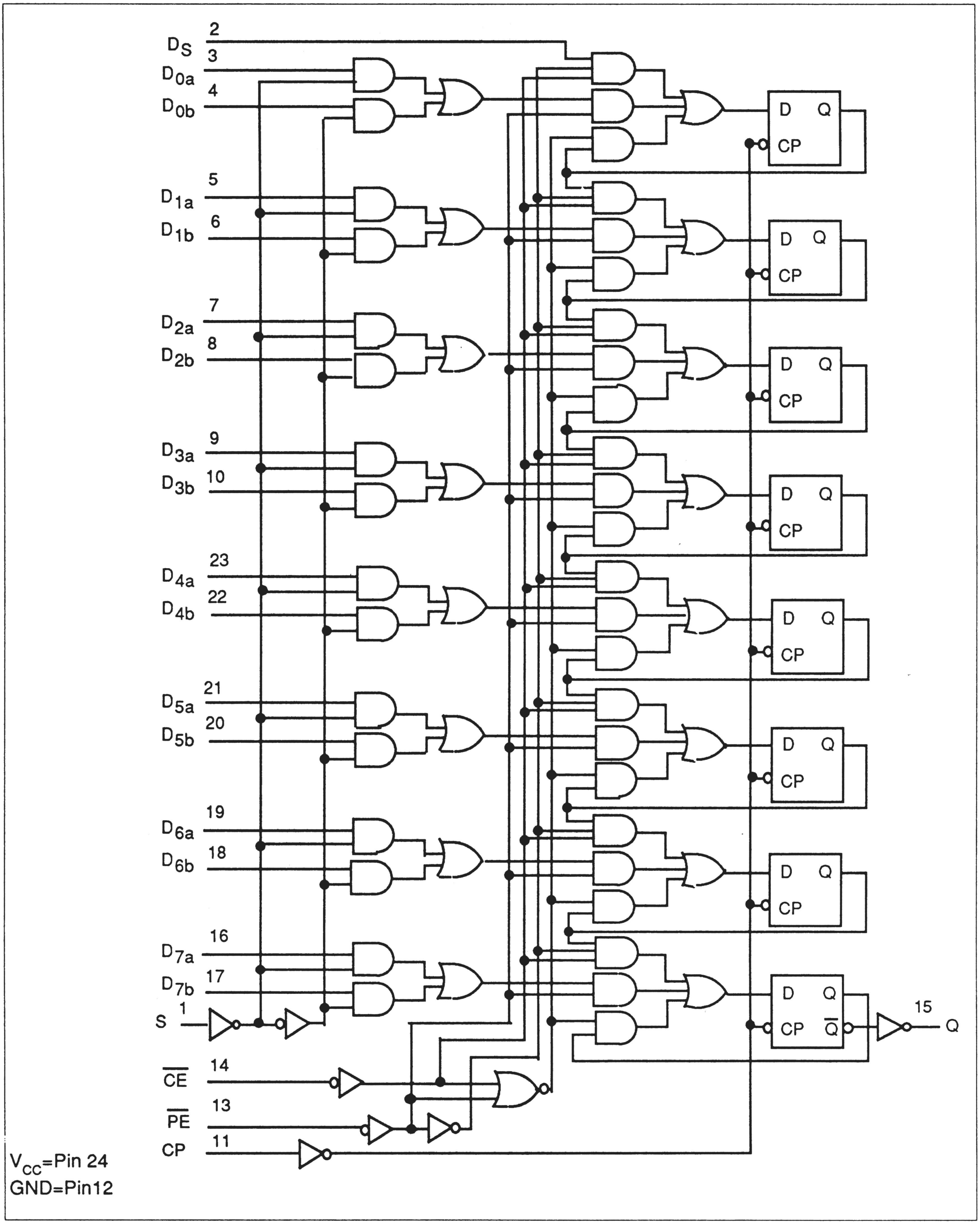

1 11 14 13
S CP CE PE
2 D_S
3 D_{0a}
4 D_{0b}
5 D_{1a}
6 D_{1b}
7 D_{2a}
8 D_{2b}
9 D_{3a}
10 D_{3b}
16 D_{4a}
17 D_{4b}
18 D_{5a}
19 D_{5b}
20 D_{6a}
21 D_{6b}
22 D_{7a}
23 D_{7b}
Q 15

V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)


SRG8
1 EN
11 0 1
14 M $\frac{0}{2}$
13 C
2
3
4
5
6
7
8
9
10
16
17
18
19
20
21
22
23
MUX
15

LOGIC DIAGRAM


DS 2
D0a 3
D0b 4
D1a 5
D1b 6
D2a 7
D2b 8
D3a 9
D3b 10
D4a 23
D4b 22
D5a 21
D5b 20
D6a 19
D6b 18
D7a 16
D7b 17
S 1
CE 14
PE 13
CP 11
D Q
CP
Q̄
15 Q
VCC=Pin 24
GND=Pin12

FUNCTION TABLE

INPUTS							OUTPUTS	OPERATING MODES
S	D_n	$\overline{CE}$	$\overline{PE}$	CP	D_{7a}	D_{7b}	Q	
L	X	X	L	↑	L	X	L	Parallel load D_{na}
L	X	X	H	↑	X	X	H	
H	X	X	L	↑	X	L	L	Parallel load D_{nb}
H	X	X	L	↑	X	H	H	
X	X	H	H	↑	X	X	Q_n	Hold (do nothing)
X	D_s	L	H	↑	X	X	Q_{n-1}	Shift data

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} =MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} =MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input clamp current at maximum input voltage	V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-600 µA	
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX				45	65	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

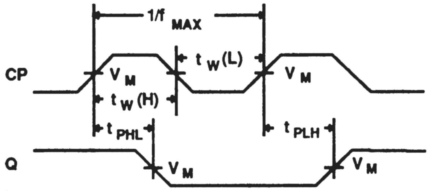
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	130		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q	Waveform 1		6.0 6.0			10.0 10.0	ns

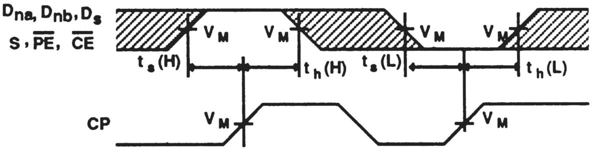
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_S, D_{na}, D_{nb} to CP	Waveform 2	7.0 7.0			7.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_S, D_{na}, D_{nb} to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S, $\overline{CE}$, $\overline{PE}$ to CP	Waveform 2	8.0 8.0			8.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S, $\overline{CE}$, $\overline{PE}$ to CP	Waveform 2	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	5.0 5.0			5.0 5.0		ns

AC WAVEFORMS


1/f MAX
CP
Q
V M
t W(L)
t W(H)
t PHL
t PLH

Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency

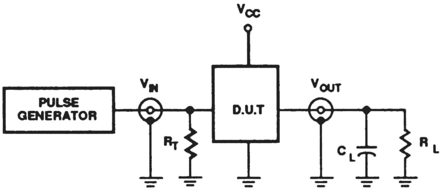

Dna, Dnb, Ds
S, PE, CE
CP
V M
t s(H)
t h(H)
t s(L)
t h(L)

Waveform 2. Data Setup And Hold Times

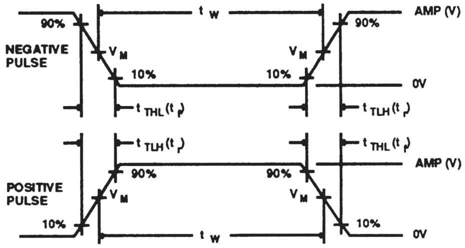
NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


Vcc
PULSE GENERATOR
V IN
R T
D.U.T
V OUT
C L
R L

Test Circuit For Totem-Pole Outputs


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
V M
t w
t THL (t f)
t TLH (t r)
AMP (V)
0V

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F755
Register

Octal MailBox Register With Ready Flag (3-State)

Product Specification

FEATURES

- **Flag set on Write signal (if desired)**
- **Automatic flag set upon Read signal**
- **Pen collector flag status output**
- **Flag status can be read via data bus**
- **300 mil 24 pin Slim DIP plastic package option**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F755	180MHz	60mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F755N
24-Pin Plastic SOL	N74F755D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

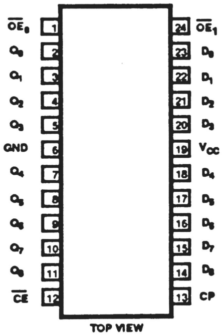
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_8	Data inputs	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/3.0	20 A/1.8mA
$\overline{CE}$	Chip Enable input (Active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable inputs (Active Low)	1.0/1.0	20µA/0.6mA
Q_8	Open Collector output	OC/ 40	OC/24mA
Q_0 - Q_7	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC=Open Collector

DESCRIPTION

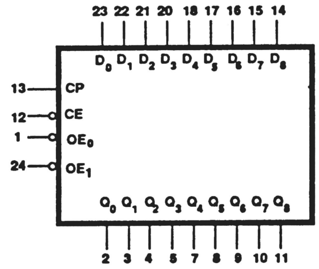
The 74F755 is an octal three state register with simple handshaking logic. Data is latched into and read from the part in the same manner as the 'F374 or other octal registers with the exception that the 'F755 has a Clock Enable pin. Handshaking can be performed in either a polled or interrupt environment by using the D_8 input and the Q_7 or Q_8 output. D_8 is latched along with the other data bits on the rising edge of the clock, but is handled differently on the output. The status of this bit can be sampled on the Q_8 open collector output and used as an interrupt or other control function. The status of D_8 can also be sampled on the Q_7 output with the appropriate combination of $\overline{OE}_0$ and $\overline{OE}_1$ for polled operation. The D_8 register is automatically reset when Q_0-Q_7 are sampled, resetting the handshaking for the next cycle. The 'F755 is equipped with a true Clock Enable ($\overline{CE}$) pin. There are no functional restrictions on the use of the $\overline{CE}$ pin. $\overline{CE}$ may be cycled with the clock input either Low or High with no false clocks generated. The 'F755 can serve as a single chip communications channel with simple handshaking, or two can be used for a bidirectional channel.

PIN CONFIGURATION



$\overline{OE}_0$ 1
Q_0 2
Q_1 3
Q_2 4
Q_3 5
GND 6
Q_4 7
Q_5 8
Q_6 9
Q_7 10
Q_8 11
$\overline{CE}$ 12
13 CP
14 D_8
15 D_7
16 D_6
17 D_5
18 D_4
19 V_{CC}
20 D_3
21 D_2
22 D_1
23 D_0
24 $\overline{OE}_1$
TOP VIEW

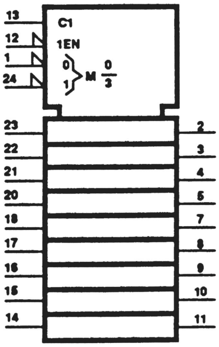
LOGIC SYMBOL



23 22 21 20 18 17 16 15 14
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8
13 CP
12 CE
1 OE_0
24 OE_1
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7 Q_8
2 3 4 5 7 8 9 10 11

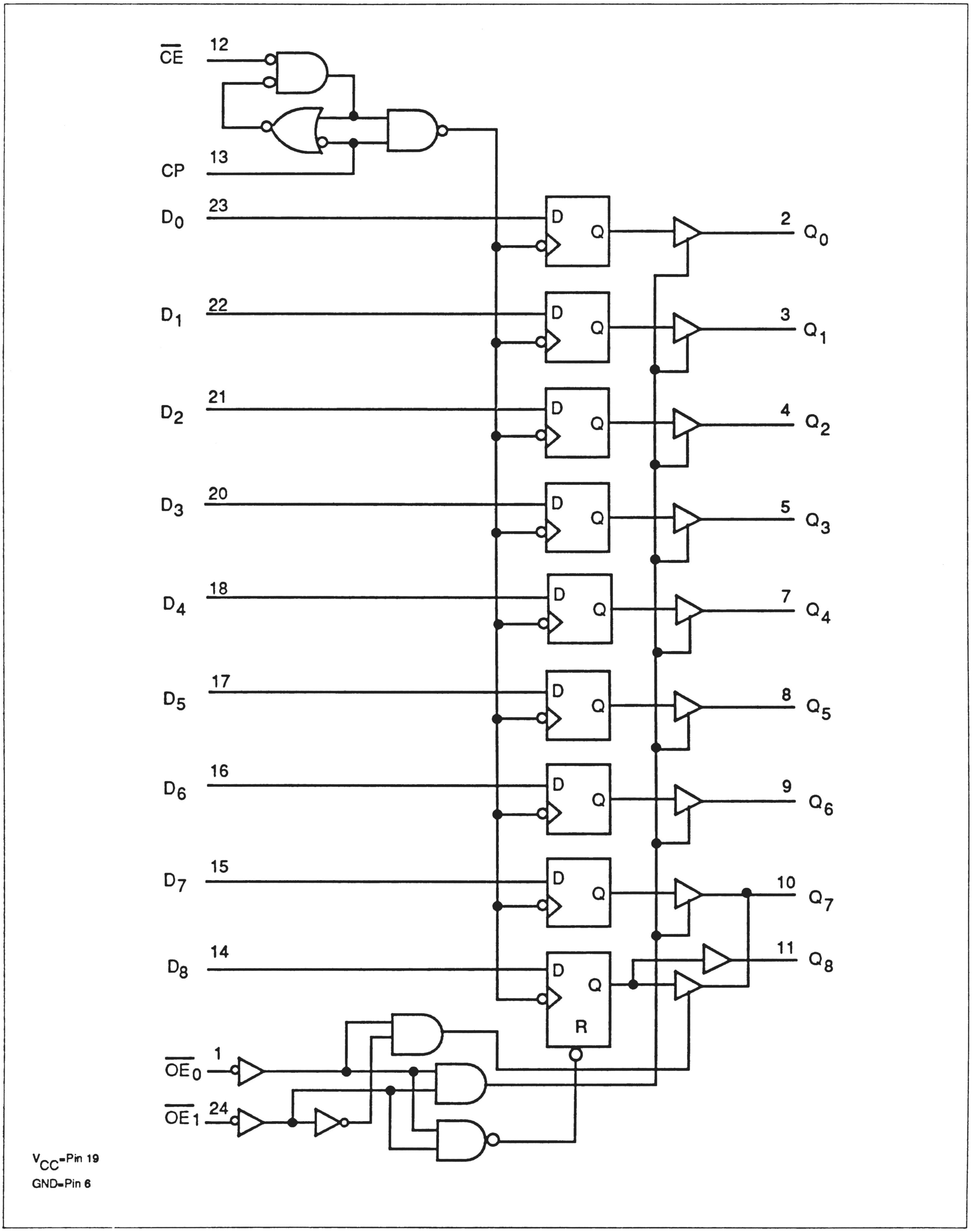
V_{CC} = Pin 19
GND = Pin 6

LOGIC SYMBOL(IEEE/IEC)



13
12
1
24
C1
1EN
0
1
M
0/3
23
22
21
20
18
17
16
15
14
2
3
4
5
7
8
9
10
11

LOGIC DIAGRAM


CE 12
CP 13
D0 23
D1 22
D2 21
D3 20
D4 18
D5 17
D6 16
D7 15
D8 14
D
Q
R
2 Q0
3 Q1
4 Q2
5 Q3
7 Q4
8 Q5
9 Q6
10 Q7
11 Q8
OE0 1
OE1 24
VCC=Pin 19
GND=Pin 6

FUNCTION TABLE

INPUTS						INTERNAL REGISTERS		OUTPUTS			OPERATING MODE
$\overline{OE}_0$	$\overline{OE}_1$	$\overline{CE}$	CP	D_0-D_7	D_8	Q_0-Q_7	Q_8	Q_0-Q_6	Q_7	Q_8	
H	X	L	‡	X	X	Q_0-Q_7	Q_8	Z	Z	Q_8	Hold and Read Q_8
H	X	H	X	X	X	Q_0-Q_7	Q_8	Z	Z	Q_8	
L	H	L	‡	X	X	Q_0-Q_7	Q_8	Z	Q_8	Q_8	
L	H	H	X	X	X	Q_0-Q_7	Q_8	Z	Q_8	Q_8	
L	L	L	‡	X	X	Q_0-Q_7	L	Q_0-Q_6	Q_7	L	Hold and Read (Q_0-Q_7) and reset Q_8
L	L	H	X	X	X	Q_0-Q_7	L	Q_0-Q_6	Q_7	L	
H	X	L	↑	D_0-D_7	D_8	D_0-D_7	D_8	Z	Z	D_8	Load (D_0-D_8)
L	H	L	↑	D_0-D_7	D_8	D_0-D_7	D_8	Z	D_8	D_8	
L	L	L	↑	D_0-D_7	X	D_0-D_7	L	D_0-D_6	D_7	L	Load (D_0-D_7) and reset Q_8

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
‡ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
V_{OH}	High level output voltage	Q_8 only			4.5	V
I_{OH}	High-level output current	Q_0-Q_7			-3	mA
I_{OL}	Low-level output current				24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current	Q_8 only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OH}	High-level output voltage	Q_0-Q_7	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=MAX	±10%VCC	2.4			V
					±5%VCC	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=MAX	±10%VCC		0.35	0.50	V
					±5%VCC		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 5.5V, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	Others	V_{CC} = MAX, V_I = 0.5V					-600	µA
		CP						-1.8	mA
I_{OZH}	Off-state output current High-level voltage applied	Q_0-Q_7	V_{CC} = MAX, V_O= 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				50	70	mA
		I_{CCL}					65	90	mA
		I_{CCZ}					60	90	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

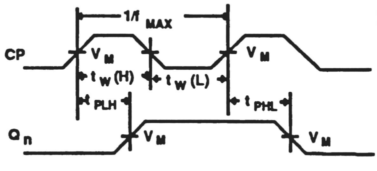
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	165	180		160		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_0-Q_7	Waveform 1	3.0 4.5	5.0 6.5	8.0 9.5	2.5 4.0	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_8	Waveform 1	7.5 5.0	9.5 6.5	12.0 9.5	7.5 4.5	12.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_1$ to Q_7	Waveform 2	6.0 6.5	7.5 8.5	10.5 11.0	5.0 6.5	11.5 11.5	ns
t_{PHL}	Propagation delay OE_n to Q_8 (reset)	Waveform 2	9.0	11.5	15.0	8.0	17.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_0$ to Q_0-Q_7	Waveform 4 Waveform 5	7.0 7.5	9.0 10.0	12.0 13.0	6.0 6.5	13.0 13.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_0$ to Q_0-Q_7	Waveform 4 Waveform 5	3.5 4.0	5.5 6.0	8.0 9.0	2.5 3.5	9.0 9.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_1$ to Q_0-Q_7	Waveform 4 Waveform 5	5.5 6.0	7.5 8.0	10.5 11.0	4.5 5.5	11.5 12.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_1$ to Q_0-Q_7	Waveform 4 Waveform 5	3.0 3.5	5.0 5.5	7.5 8.5	2.5 3.0	8.5 9.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_0$ to Q_7	Waveform 4 Waveform 5	9.5 10.5	11.0 12.5	14.0 15.0	8.5 9.5	16.0 17.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_0$ to Q_7	Waveform 4 Waveform 5	3.5 3.5	5.0 5.5	8.0 8.0	2.5 3.5	8.5 8.5	ns

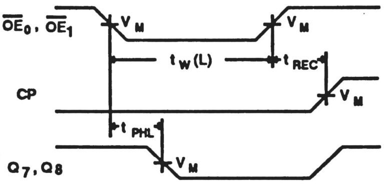
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 3	3.5 3.0			4.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CE}$ to CP	Waveform 3	0.0 0.0			0.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP	Waveform 3	2.0 3.0			2.5 3.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	3.0 3.5			3.0 4.0		ns
$t_w(L)$	$\overline{OE}_0$ Pulse width,Low	Waveform 2	6.5			8.5		ns
$t_w(L)$	$\overline{OE}_1$ Pulse width, Low	Waveform 2	5.5			6.5		ns
t_{REC}	Recovery time, $\overline{OE}_n$ to CP	Waveform 2	5.0			5.5		ns

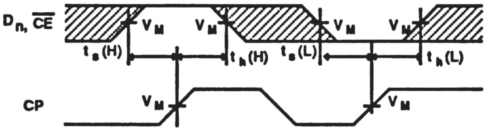
AC WAVEFORMS


CP
1/f MAX
V M
t w (H)
t w (L)
t PLH
t PHL
Q n

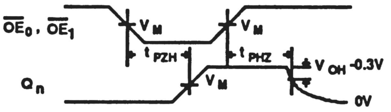
Waveform 1.
Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency


OE0, OE1
V M
t w (L)
t REC
CP
t PHL
Q7, Q8

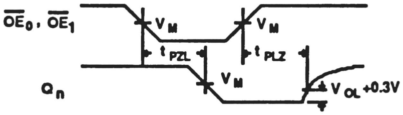
Waveform 2. Output Enables Pulse Width, Output Enables to Q8 Output Delay and Output Enables to Clock ad Chip Enable Recovery Time


Dn, CE
V M
t s (H)
t h (H)
t s (L)
t h (L)
CP

Waveform 3. Data Setup And Hold Times


OE0, OE1
V M
t PZH
t PHZ
V OH -0.3V
Q n
0V

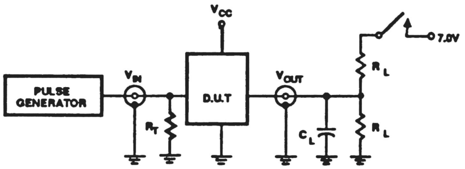
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level


OE0, OE1
V M
t PZL
t PLZ
Q n
V OL +0.3V

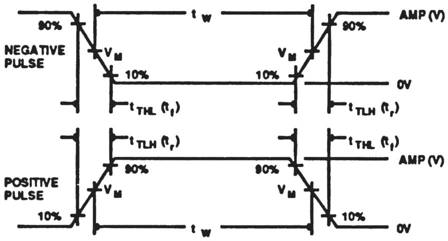
Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


Vcc
PULSE GENERATOR
V IN
R T
D.U.T
V OUT
C L
R L
7.0V

Test Circuit For 3-State Outputs


90%
NEGATIVE PULSE
V M
10%
t w
AMP (V)
0V
t THL (t f)
t TLH (t r)
POSITIVE PULSE

$V_M = 1.5V$
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F756, 74F757, 74F760

Buffers

74F756 Octal Inverter Buffer (Open Collector)
74F757 Octal Buffer (Open Collector)
74F760 Octal Buffer (Open Collector)

Product Specification

FEATURES

- **Octal bus interface**
- **Open collector versions of 74F240, 74F241 and 74F244**

DESCRIPTION

The 74F756, 74F757 and 74F760 are octal buffers that are ideal for driving bus lines of buffer memory address registers. The 74F756 is the open collector version of 74F240, 74F757 is the open collector version of 74F241 and 74F760 is the open collector version of 74F244. These devices feature two Output Enables, $\overline{OE}_a$ and $\overline{OE}_b$ (or OE_b for the 'F757), each controlling four of the outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F756	9.0ns	40mA
74F757	9.0ns	45mA
74F760	9.0ns	45mA

ORDERING INFORMATION

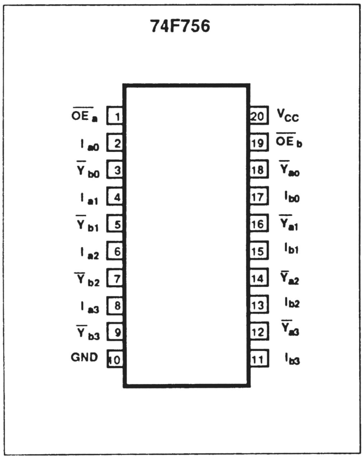
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F756N, N74F757N, N74F760N
20-Pin Plastic SOL	N74F756D, N74F757D, N74F760D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

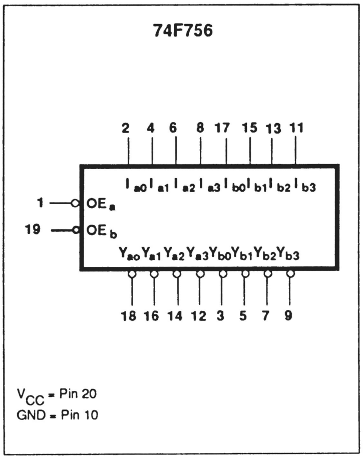
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{an}, I_{bn}	Data inputs	1.0/1.67	20µA/1.0mA
$\overline{OE}_a$ $\overline{OE}_b$	Output enable input (active Low)	1.0/1.67	20µA/1.0mA
OE_b	Output enable input (active High 'F757)	1.0/1.67	20µA/1.0mA
Y_{an}, Y_{bn}	Data outputs ('F757, 'F760)	OC/106.7	OC/64mA
$\overline{Y}_{an}$, $\overline{Y}_{bn}$	Data outputs ('F756)	OC/106.7	OC/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC= Open Collector

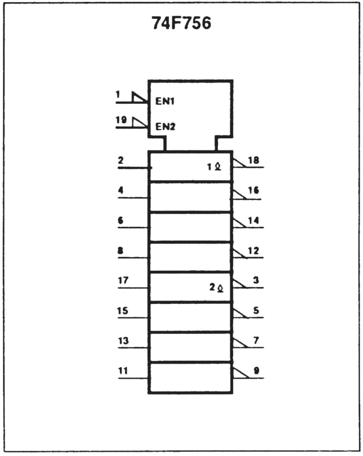
PIN CONFIGURATION


74F756
$\overline{OE}_a$ 1
I_{a0} 2
$\overline{Y}_{b0}$ 3
I_{a1} 4
$\overline{Y}_{b1}$ 5
I_{a2} 6
$\overline{Y}_{b2}$ 7
I_{a3} 8
$\overline{Y}_{b3}$ 9
GND 10
20 V_{CC}
19 $\overline{OE}_b$
18 $\overline{Y}_{a0}$
17 I_{b0}
16 $\overline{Y}_{a1}$
15 I_{b1}
14 $\overline{Y}_{a2}$
13 I_{b2}
12 $\overline{Y}_{a3}$
11 I_{b3}

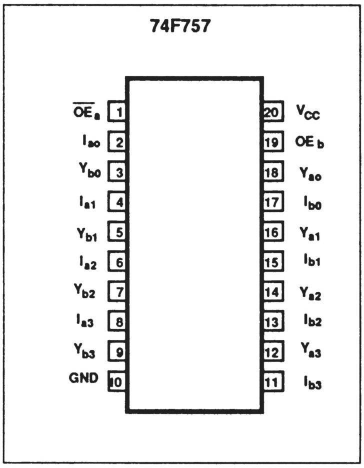
LOGIC SYMBOL


74F756
2 4 6 8 17 15 13 11
I_{a0} I_{a1} I_{a2} I_{a3} I_{b0} I_{b1} I_{b2} I_{b3}
1 OE_a
19 OE_b
Y_{a0} Y_{a1} Y_{a2} Y_{a3} Y_{b0} Y_{b1} Y_{b2} Y_{b3}
18 16 14 12 3 5 7 9
V_{CC} = Pin 20
GND = Pin 10

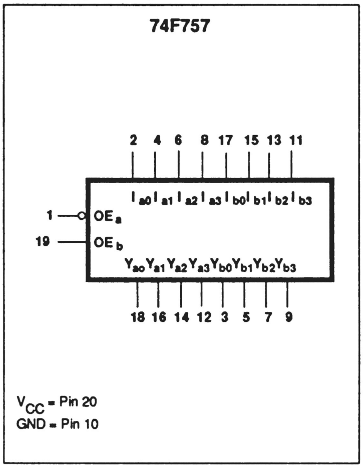
LOGIC SYMBOL(IEEE/IEC)


74F756
1 EN1
19 EN2
2 1 18
4 16
6 14
8 12
17 2 3
15 5
13 7
11 9

PIN CONFIGURATION

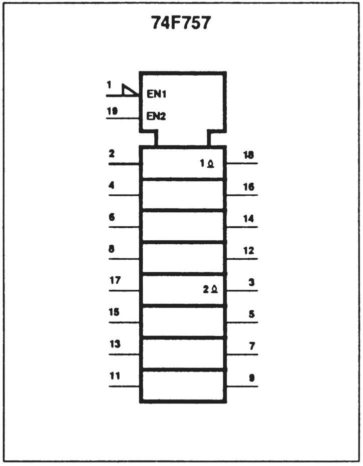

74F757
$\overline{OE}_a$ 1
I_{a0} 2
Y_{b0} 3
I_{a1} 4
Y_{b1} 5
I_{a2} 6
Y_{b2} 7
I_{a3} 8
Y_{b3} 9
GND 10
20 V_{CC}
19 OE_b
18 Y_{a0}
17 I_{b0}
16 Y_{a1}
15 I_{b1}
14 Y_{a2}
13 I_{b2}
12 Y_{a3}
11 I_{b3}

LOGIC SYMBOL

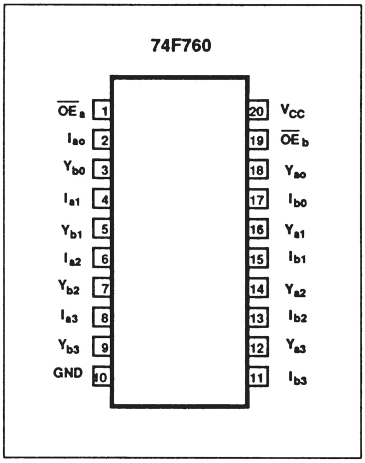

74F757
2 4 6 8 17 15 13 11
I_{a0} I_{a1} I_{a2} I_{a3} I_{b0} I_{b1} I_{b2} I_{b3}
1 OE_a
19 OE_b
Y_{a0} Y_{a1} Y_{a2} Y_{a3} Y_{b0} Y_{b1} Y_{b2} Y_{b3}
18 16 14 12 3 5 7 9

V_{CC} = Pin 20
GND = Pin 10

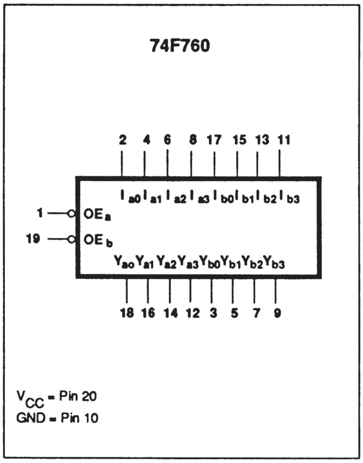
LOGIC SYMBOL(IEEE/IEC)


74F757
1
EN1
19
EN2
2
1▽
18
4
16
6
14
8
12
17
2▽
3
15
5
13
7
11
9

PIN CONFIGURATION

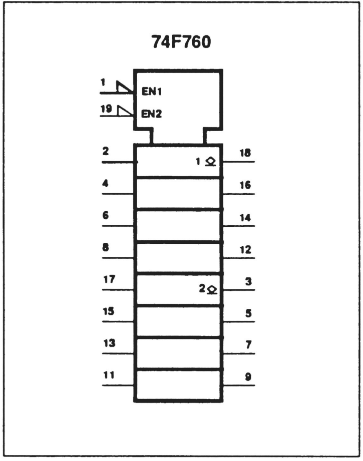

74F760
$\overline{OE}_a$ 1
I_{a0} 2
Y_{b0} 3
I_{a1} 4
Y_{b1} 5
I_{a2} 6
Y_{b2} 7
I_{a3} 8
Y_{b3} 9
GND 10
20 V_{CC}
19 $\overline{OE}_b$
18 Y_{a0}
17 I_{b0}
16 Y_{a1}
15 I_{b1}
14 Y_{a2}
13 I_{b2}
12 Y_{a3}
11 I_{b3}

LOGIC SYMBOL

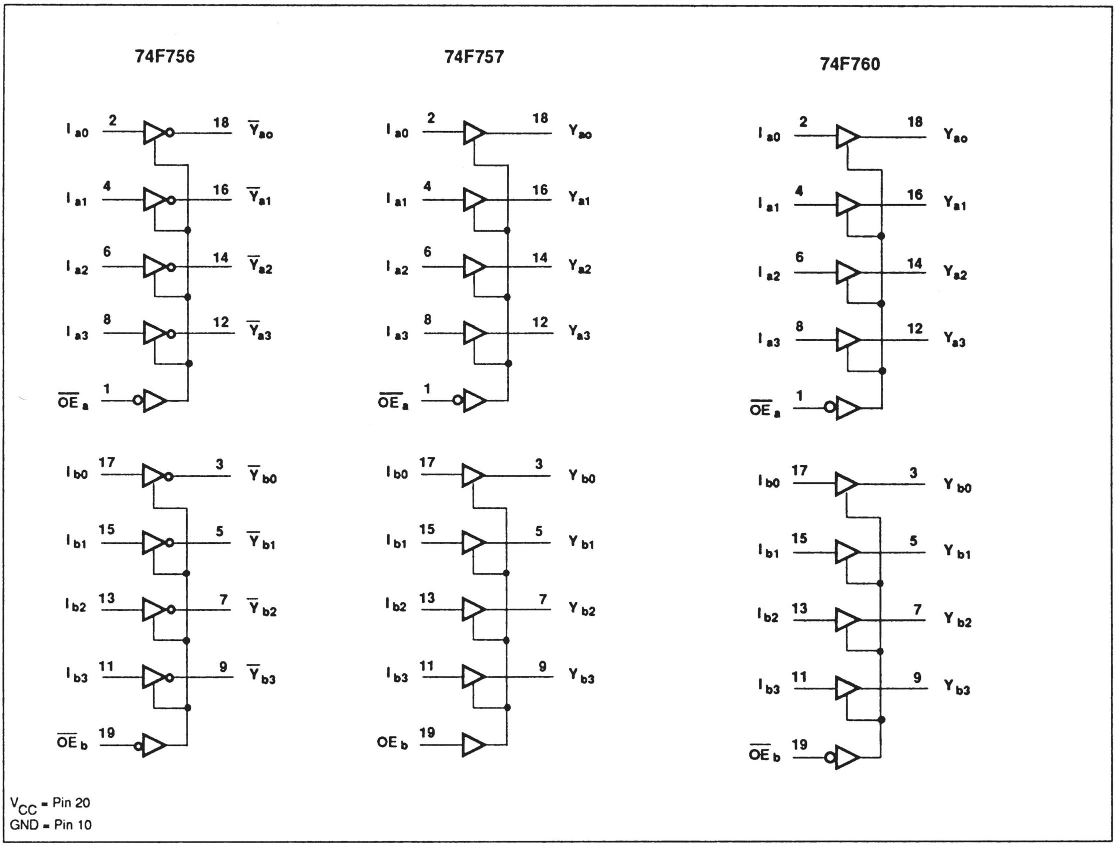

74F760
2 4 6 8 17 15 13 11
I_{a0} I_{a1} I_{a2} I_{a3} I_{b0} I_{b1} I_{b2} I_{b3}
1 OE_a
19 OE_b
Y_{a0} Y_{a1} Y_{a2} Y_{a3} Y_{b0} Y_{b1} Y_{b2} Y_{b3}
18 16 14 12 3 5 7 9

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)


74F760
1
EN1
19
EN2
2
1▽
18
4
16
6
14
8
12
17
2▽
3
15
5
13
7
11
9

LOGIC DIAGRAM


74F756
74F757
74F760
I_{a0} 2 18 $\overline{Y}_{a0}$
I_{a1} 4 16 $\overline{Y}_{a1}$
I_{a2} 6 14 $\overline{Y}_{a2}$
I_{a3} 8 12 $\overline{Y}_{a3}$
$\overline{OE}_a$ 1
I_{b0} 17 3 $\overline{Y}_{b0}$
I_{b1} 15 5 $\overline{Y}_{b1}$
I_{b2} 13 7 $\overline{Y}_{b2}$
I_{b3} 11 9 $\overline{Y}_{b3}$
$\overline{OE}_b$ 19
I_{a0} 2 18 Y_{a0}
I_{a1} 4 16 Y_{a1}
I_{a2} 6 14 Y_{a2}
I_{a3} 8 12 Y_{a3}
$\overline{OE}_a$ 1
I_{b0} 17 3 Y_{b0}
I_{b1} 15 5 Y_{b1}
I_{b2} 13 7 Y_{b2}
I_{b3} 11 9 Y_{b3}
OE_b 19
I_{a0} 2 18 Y_{a0}
I_{a1} 4 16 Y_{a1}
I_{a2} 6 14 Y_{a2}
I_{a3} 8 12 Y_{a3}
$\overline{OE}_a$ 1
I_{b0} 17 3 Y_{b0}
I_{b1} 15 5 Y_{b1}
I_{b2} 13 7 Y_{b2}
I_{b3} 11 9 Y_{b3}
$\overline{OE}_b$ 19

V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE, 74F756

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_a$	$\overline{Y}_b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	H(off)	H(off)

FUNCTION TABLE, 74F760

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	H(off)	H(off)

FUNCTION TABLE, 74F757

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	OE_b	I_b	Y_a	Y_b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	H(off)	H(off)

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER				UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_K	Input clamp current			-18	mA
V_{OH}	High level output voltage			4.5	V
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX			250	µA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL}=48mA ±10%V_{CC}		0.38	0.55	V
		I_{OL}=64mA ±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}		-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V			100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V			20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V			-1.0	mA
I_{CC}	Supply current (total) 74F756 I_{CCH}	V_{CC}=MAX		20	30	mA
	I_{CCL}			50	70	mA
	74F757 I_{CCH}			30	40	mA
	I_{CCL}			55	80	mA
	74F760 I_{CCH}			25	37	mA
	I_{CCL}			55	80	mA

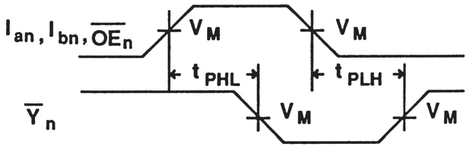
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

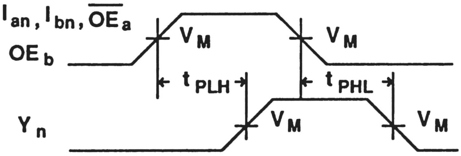
AC ELECTRICAL CHARACTERISITICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to $\overline{Y}_n$	74F756	Waveform 1, 2	8.5 1.0	11.0 3.0	14.0 6.0	8.5 1.0	15.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_n$ to $\overline{Y}_n$		Waveform 1, 2	9.0 5.0	11.5 7.0	14.5 10.0	9.0 4.5	15.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to Y_n	74F757	Waveform 1, 2	7.5 3.0	10.5 5.5	13.5 8.5	7.5 3.0	14.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_a$ or OE_b to Y_n		Waveform 1, 2	9.5 4.5	12.5 7.0	16.5 10.0	9.0 4.0	17.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to Y_n	74F760	Waveform 1, 2	7.5 3.5	10.0 5.5	13.5 8.5	7.5 3.0	14.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_n$ to Y_n		Waveform 1, 2	9.5 5.0	11.5 7.0	14.5 10.0	9.0 4.5	15.0 10.5	ns

AC WAVEFORMS



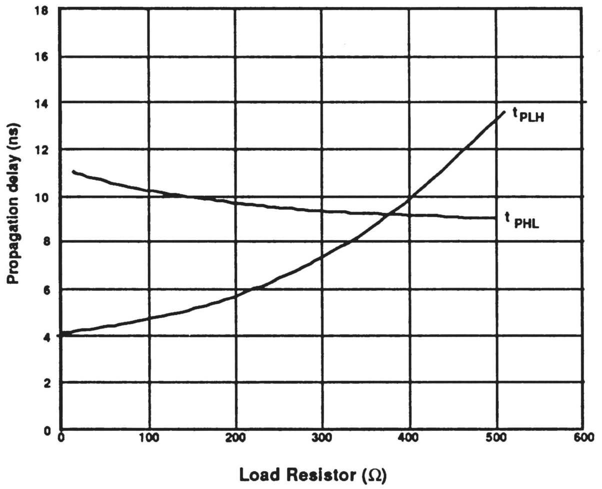
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs

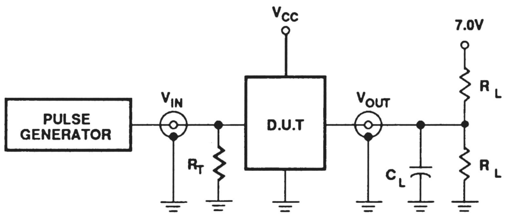
NOTE: For all waveforms, $V_M = 1.5V$.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

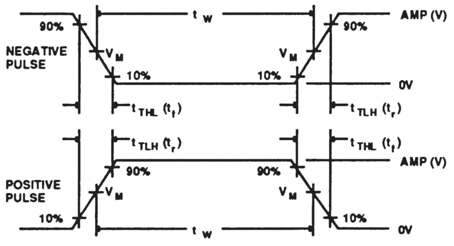


NOTE:
When using open-collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the pull-up resistor value from 500 Ω to 100Ω will improve the t_{PLH} up to 50% with only slight increase in the t_{PHL}. However, if the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL} 's of the receivers do not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
7.0V
R_L
PULSE GENERATOR
V_{IN}
D.U.T
V_{OUT}
R_T
C_L
R_L

Test Circuit For Open Collector Outputs


90%
NEGATIVE PULSE
V_M
10%
t_{THL} (t_f)
t_W
V_M
10%
90%
AMP (V)
0V
t_{TLH} (t_r)
t_{TLH} (t_r)
90%
POSITIVE PULSE
V_M
10%
t_W
t_{THL} (t_f)
90%
V_M
10%
AMP (V)
0V

V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F776

Pi-Bus Transceiver

Octal Bidirectional Latched Transceiver (Open Collector)
Product Specification

FEATURES

- **Octal Latched Transceiver**
- **Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms**
- **High drive (100mA) open collector drivers on B-port**
- **Reduced voltage swing (1 volt) produces less noise and reduces power consumption**
- **High speed operation enhances performance of backplane buses and facilitates incident wave switching**
- **Compatible with Pi-bus and IEEE 896 Futurebus Standards**
- **Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity**
- **Controlled output ramp and multiple GND pins minimize ground bounce**
- **Glitch-free power up / power down operation**
- **Multiple package options**

TYPE	TYPICAL PROPAGATION DELAY	MAX SUPPLY CURRENT (TOTAL)
74F776	7.5ns	85mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V\pm10\%$; $T_A = 0°C$ to $+70°C$
28-Pin Plastic DIP (600mil)[1]	N74F776N
28-Pin PLCC[1]	N74F776A

NOTE:
1. Thermal mounting techniques are recommended. See SMD Process ASpllications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	PNP latched inputs	3.5/0.117	70µA/70µA
$B_0 - B_7$	Data inputs with threshold circuitry	5.0/0.167	100µA/100µA
OEA	A Output Enable input (active High)	1.0/0.033	20µA/20µA
$\overline{OEB}_0$, $\overline{OEB}_1$	B Output Enable inputs (active Low)	1.0/0.033	20µA/20µA
$\overline{LE}$	Latch Enable input (active Low)	1.0/0.033	20µA/20µA
$A_0 - A_7$	3-State outputs	150/40	3mA/24mA
$B_0 - B_7$	Open Collector outputs	OC*/166.7	OC*/100mA

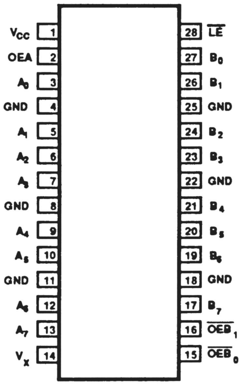
NOTES:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
* OC = Open Collector

DESCRIPTION

The 74F776 is an octal bidirectional latched transceiver and is intended to provide the electrical interface to a high performance wired-or bus. The B port inverting drivers are low-capacitance open collector with controlled ramp and are designed to sink 100 mA from 2 volts. The B port inverting receivers have a 100 mV threshold region and a 4ns glitch filter.

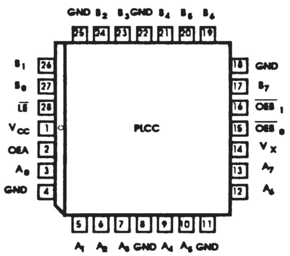
The 74F776 B port interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive

PIN CONFIGURATION



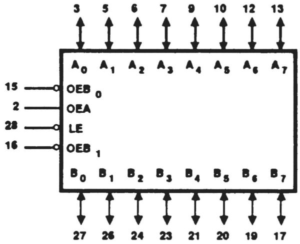
V_{CC} 1
OEA 2
A_0 3
GND 4
A_1 5
A_2 6
A_3 7
GND 8
A_4 9
A_5 10
GND 11
A_6 12
A_7 13
V_X 14
28 $\overline{LE}$
27 B_0
26 B_1
25 GND
24 B_2
23 B_3
22 GND
21 B_4
20 B_5
19 B_6
18 GND
17 B_7
16 $\overline{OEB}_1$
15 $\overline{OEB}_0$

PIN CONFIGURATION PLCC



GND B_2 B_3 GND B_4 B_5 B_6
25 24 23 22 21 20 19
B_1 26
B_0 27
$\overline{LE}$ 28
V_{CC} 1
OEA 2
A_0 3
GND 4
18 GND
17 B_7
16 $\overline{OEB}_1$
15 $\overline{OEB}_0$
14 V_X
13 A_7
12 A_6
PLCC
5 6 7 8 9 10 11
A_1 A_2 A_3 GND A_4 A_5 GND

LOGIC SYMBOL



3 5 6 7 9 10 12 13
A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7
15 OEB_0
2 OEA
28 LE
16 OEB_1
B_0 B_1 B_2 B_3 B_4 B_5 B_6 B_7
27 26 24 23 21 20 19 17

V_{CC} = Pin 1 V_X = Pin 14
GND = Pin 4, 8, 11, 18, 22, 25

September 2, 1988

DESCRIPTION (Continued)

loading (<5 pF). Incident wave switching is employed, therefore BTL propagation delays are short. Although the voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane.

The 74F776 A port has TTL 3-State drivers and TTL receivers with a latch function. A separate High-level control voltage input (V_x) is provided to limit the A side output level to a given voltage level (such as 3.3V). For 5.0V systems, V_x is simply tied to V_{CC}.

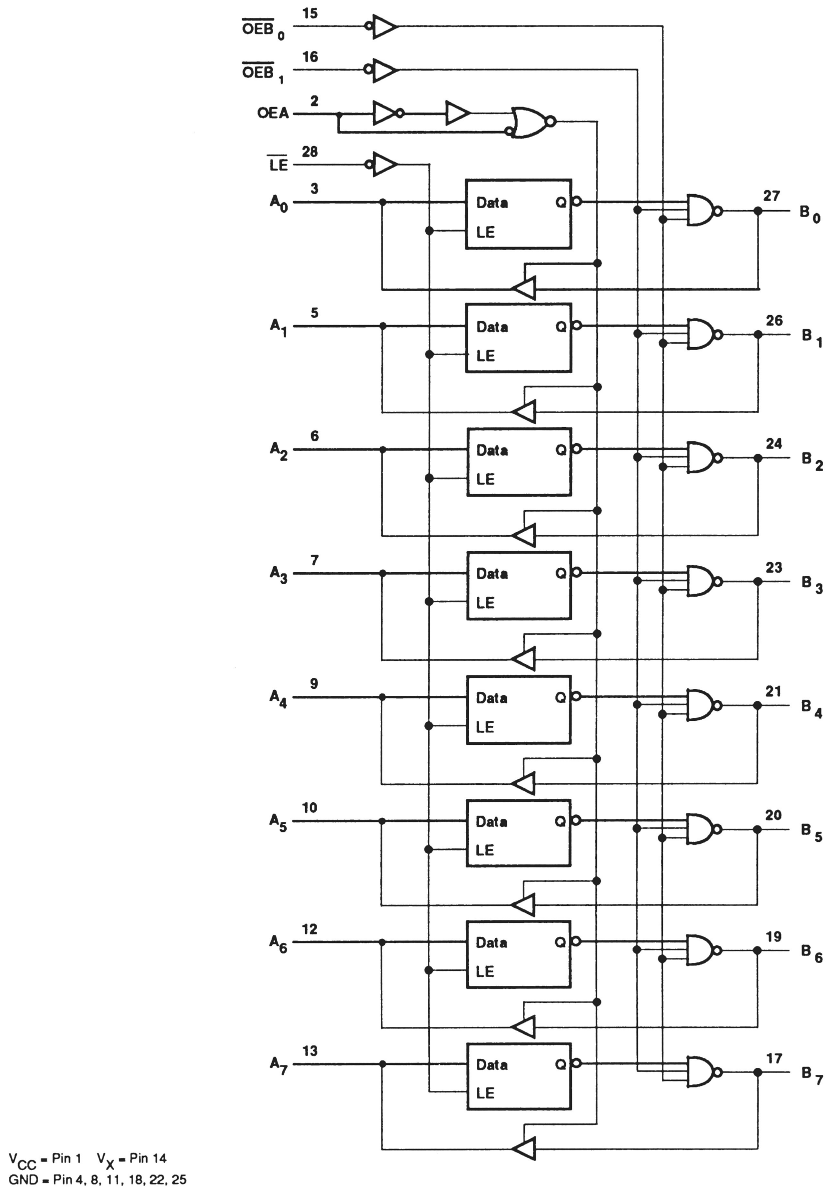
The 'F776 has a designed feature to control the B output transitions during power sequencing. There are two possible sequences, They are as follows:

1. When $\overline{LE}$=Low and $\overline{OEB}_n$= Low then the B outputs are disabled until the $\overline{LE}$ circuitry takes control. Then the B outputs will follow the A inputs, making a maximum of one transition during power-up (or down).
2. If $\overline{LE}$=High or $\overline{OEB}_n$= High then the B outputs will be disabled durng power-up (or down).

PIN DESCRIPTION

SYMBOL	PINS	TYPE	NAME AND FUNCTION
A_0	3	I/O	PNP latched input / 3-State output (with V_X control option)
A_1	5	I/O	
A_2	6	I/O	
A_3	7	I/O	
A_4	9	I/O	
A_5	10	I/O	
A_6	12	I/O	
A_7	13	I/O	
B_0	27	I/O	Data input with special threshold circuitry to reject noise / Open Collector output, High current drive
B_1	26	I/O	
B_2	24	I/O	
B_3	23	I/O	
B_4	21	I/O	
B_5	20	I/O	
B_6	19	I/O	
B_7	17	I/O	
$\overline{OEB}_0$	15	I	Enables the B outputs when both pins are Low
$\overline{OEB}_1$	16	I	
OEA	2	I	Enables the A outputs when High
$\overline{LE}$	28	I	Latched when High (a special delay feature is built in for proper enabling times)
V_X	14	I	Clamping voltage keeping V_{OH} from rising above V_X ($V_X = V_{CC}$ for normal use)

LOGIC DIAGRAM


$\overline{OEB}_0$ 15
$\overline{OEB}_1$ 16
OEA 2
$\overline{LE}$ 28
A_0 3
A_1 5
A_2 6
A_3 7
A_4 9
A_5 10
A_6 12
A_7 13
Data
LE
Q
27 B_0
26 B_1
24 B_2
23 B_3
21 B_4
20 B_5
19 B_6
17 B_7
V_{CC} = Pin 1 V_X = Pin 14
GND = Pin 4, 8, 11, 18, 22, 25

FUNCTION TABLE

INPUTS						LATCH	OUTPUTS		MODE
A_n	B_n*	$\overline{LE}$	OEA	$\overline{OEB_0}$	$\overline{OEB_1}$	STATE	A_n	B_n	
H	X	L	L	L	L	H	Z	Z	A 3-state, Data from A to B
L	X	L	L	L	L	L	Z	L	
X	X	H	L	L	L	Q_n	Z	Q_n	A 3-state, Latched data to B
–	–	L	H	L	L	(1)	(1)	(1)	Feedback: A to B, B to A
–	H	H	H	L	L	$H^{(2)}$	H	$Z^{(2)}$	Preconditioned Latch enabling data transfer from B to A
–	L	H	H	L	L	$H^{(2)}$	L	$Z^{(2)}$	
–	–	H	H	L	L	Q_n	Q_n	Q_n	Latch state to A and B
H	X	L	L	H	X	H	Z	Z	B and A 3-state
L	X	L	L	H	X	L	Z	Z	
X	X	H	L	H	X	Q_n	Z	Z	
–	H	L	H	H	X	H	H	Z	B 3-state, Data from B to A
–	L	L	H	H	X	L	L	Z	
–	H	H	H	H	X	Q_n	H	Z	
–	L	H	H	H	X	Q_n	L	Z	
H	X	L	L	X	H	H	Z	Z	B and A 3-state
L	X	L	L	X	H	L	Z	Z	
X	X	H	L	X	H	Q_n	Z	Z	
–	H	L	H	X	H	H	H	Z	B 3-state, Data from B to A
–	L	L	H	X	H	L	L	Z	
–	H	H	H	X	H	Q_n	H	Z	
–	L	H	H	X	H	Q_n	L	Z	

H = High voltage level
L = Low voltage level
X = Don't care
– = Input not externally driven
Z = High Impedance (off) state
Q_n = High or Low voltage level one setup time prior to the Low-to-High $\overline{LE}$ transition
(1) = Condition will cause a feedback loop path; A to B and B to A
(2) = The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB_0}$ and $\overline{OEB_1}$ are Low and $\overline{LE}$ is High.
B* = Precaution should be taken to insure the B inputs do not float. If they do they are equal to Low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_X	Threshold control		-0.5 to +7.0	V
V_{IN}	Input voltage	$\overline{OEB}_n$, OEA, $\overline{LE}$	-0.5 to +7.0	V
		A_0 - A_7, B_0 - B_7	-0.5 to 5.5	
I_{IN}	Input current		-40 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	A_0 -A_7	48	mA
		B_0 - B_7	200	
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage	Except B_0 - B_7	2.0			V
		B_0 - B_7	1.8			
V_{IL}	Low-level input voltage	Except B_0 - B_7			0.8	V
		B_0 - B_7			1.45	
I_{IK}	Input clamp current	Except A_0 - A_7			-18	mA
		A_0 - A_7			-40	
I_{OH}	High-level output current	A_0 - A_7			-3	mA
I_{OL}	Low-level output current	A_0 -A_7			24	mA
		B_0 - B_7			100	
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
I_{OH}	High level output current	B_0 - B_7	V_{CC} = MAX, V_{IL} =MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
I_{OFF}	Power-off output current	B_0 - B_7	V_{CC} = 0.0V, V_{IL} =MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
V_{OH}	High-level output voltage	A_0 - A_7[4]	V_{CC} = MIN, V_{IL}= MAX,	I_{OH} = -3mA, V_X = V_{CC}	2.5		V_{CC}	V
			V_{IH} = MIN	I_{OH} = -0.4mA, V_X = 3.13V & 3.47V	2.5		V_X	V
V_{OL}	Low-level output voltage	A_0 - A_7[4]	V_{CC} = MIN, V_{IL}= MAX, V_{IH} = MIN	I_{OL} = 20mA, V_X = V_{CC}			0.5	V
		B_0 - B_7	V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = 100mA			1.15	V
			V_{IH} = MIN	I_{OL} = 4mA	0.40			V
V_{IK}	Input clamp voltage	A_0 - A_7	V_{CC} = MIN, I_I = I_{IK}				-0.5	V
		Except A_0 - A_7	V_{CC} = MIN, I_I = I_{IK}				-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEB}_n$, OEA, $\overline{LE}$	V_{CC} = 0.0V, V_I = 7.0V				100	µA
		A_0 - A_7, B_0 - B_7	V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High-level input current	$\overline{OEB}_n$, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 2.7V, B_n - A_n = 0V				20	µA
		B_0 - B_7	V_{CC} = MAX, V_I = 2.1V				100	µA
I_{IL}	Low-level input current	$\overline{OEB}_n$, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 0.5V				-20	µA
		B_0 - B_7	V_{CC} = MAX, V_I = 0.3V				-100	µA
I_{OZH} + I_{IH}	Off-state output current, High-level voltage applied	A_0 - A_7	V_{CC} = MAX, V_O =2.7V				70	µA
I_{OZL} + I_{IL}	Off-state output current, Low-level voltage applied	A_0 - A_7	V_{CC} = MAX, V_O =0.5V				-70	µA
I_X	High-level control current		V_{CC} = MAX, V_X = V_{CC}, $\overline{LE}$ = OEA = $\overline{OEB}_n$ = 2.7V, A_0 - A_7 = 2.7V, B_0 - B_7 = 2.0V		-100		100	µA
			V_{CC} = MAX, V_X = 3.13V & 3.47 V, $\overline{LE}$ = OEA = 2.7V, $\overline{OEB}_n$ =A_0 - A_7 = 2.7V, B_0 - B_7 = 2.0V		-10		10	mA
I_{OS}	Short-circuit output current[3]	A_0 - A_7 only	V_{CC} = MAX, B_n = 1.6V, OEA = 2.0V, $\overline{OEB}_n$ = 2.7V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			70	100	mA
		I_{CCL}	V_{CC} = MAX, V_{IL} = 0.5V			100	145	mA
		I_{CCZ}	V_{CC} = MAX, V_{IL} = 0.5V			80	100	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. Unless otherwise specified, V_X = V_{CC} for all test conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH}=1.6V and V_{IL}=1.3V.

AC ELECTRICAL CHARACTERISTICS

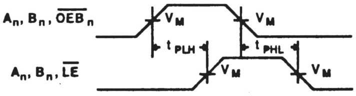
SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay B to A	Waveform 1, 2	5.5 6.0	7.5 7.5	12.0 10.5	5.0 6.0	12.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable time from High or Low OEA to A	Waveform 4.5	8.0 8.5	10.5 12.0	14.5 14.5	7.5 8.5	15.5 17.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low OEA to A	Waveform 4.5	2.0 2.0	4.5 4.5	7.0 7.5	2.0 2.0	7.5 8.0	ns

SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_D = 30pF$ $R_U = 9\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_D = 30pF$ $R_U = 9\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A to B	Waveform 1, 2	2.0 3.5	4.0 6.0	7.0 8.0	2.0 3.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to B	Waveform 1, 2	3.0 4.0	5.0 6.0	8.5 9.0	2.5 3.0	10.0 9.5	ns
t_{PLH} t_{PHL}	Enable/disable time $\overline{OEB}_n$ to B	Waveform 1, 2	2.5 4.5	4.5 7.5	7.5 10.5	1.5 3.5	8.5 10.5	ns
t_{TLH} t_{THL}	Transition time, B Port 1.3V to 1.7 V, 1.7V to 1.3V	Test Circuit and Waveform	0.5 0.5	2.0 2.0	4.5 4.5	0.5 0.5	4.5 4.5	ns

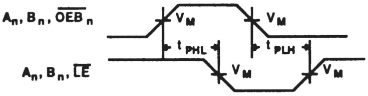
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Set-up time A to $\overline{LE}$	Waveform 3	5.0 5.0			5.0 5.0		ns
t_h(H) t_h(L)	Hold time A to $\overline{LE}$	Waveform 3	0.0 0.0			0.0 0.0		ns
t_w(L)	$\overline{LE}$ Pulse width, Low	Waveform 3	6.0			6.0		ns

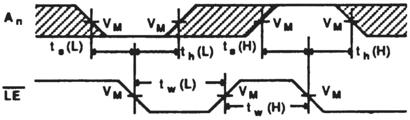
AC WAVEFORMS


A_n, B_n, $\overline{OEB}_n$
V_M
V_M
t_{PLH}
t_{PHL}
A_n, B_n, $\overline{LE}$
V_M
V_M

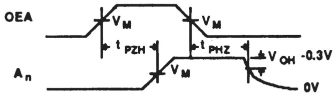
Waveform 1. Propagation Delay For Data To Output


A_n, B_n, $\overline{OEB}_n$
V_M
V_M
t_{PHL}
t_{PLH}
A_n, B_n, $\overline{LE}$
V_M
V_M

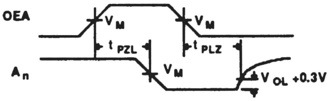
Waveform 2. Propagation Delay For Data To Output


A_n
V_M
V_M
V_M
V_M
$t_s(L)$
$t_h(L)$
$t_s(H)$
$t_h(H)$
$\overline{LE}$
V_M
$t_w(L)$
V_M
V_M
$t_w(H)$

Waveform 3. Data Setup And Hold Times And $\overline{LE}$ Pulse Widths


OEA
V_M
V_M
t_{PZH}
t_{PHZ}
V_{OH} -0.3V
A_n
V_M
0V

Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level

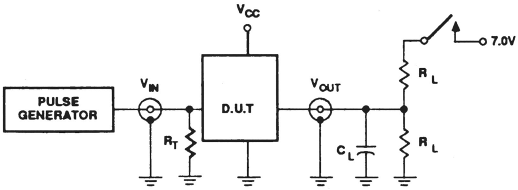

OEA
V_M
V_M
t_{PZL}
t_{PLZ}
A_n
V_M
V_{OL} +0.3V

Waveform 5 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

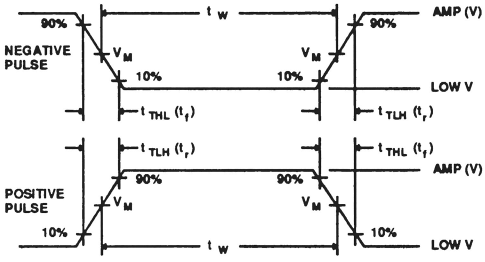
NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
7.0V
PULSE GENERATOR
V_{IN}
D.U.T
V_{OUT}
R_L
R_T
C_L
R_L

Test Circuit For 3-State Outputs On A Port

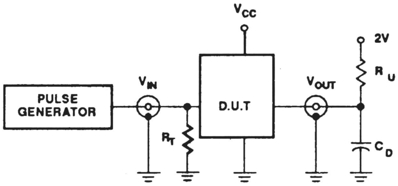

t_W
AMP (V)
90%
90%
NEGATIVE PULSE
V_M
V_M
10%
10%
LOW V
t_{THL} (t_f)
t_{TLH} (t_r)
t_{TLH} (t_r)
t_{THL} (t_f)
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
LOW V
t_W

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open


V_{CC}
2V
R_U
PULSE GENERATOR
V_{IN}
D.U.T
V_{OUT}
R_T
C_D

Test Circuit For Outputs On B Port

FAMILY 74F	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_U = Pull up resistor; see AC CHARACTERISTICS for value.

FAST 74F779, 74F779A Counters

8-Bit Bidirectional Binary Counter (3-state)

Preliminary Specification for 74F779A
Product Specification for 74F779

FEATURES

- **Multiplexed 3-state I/O ports for bus oriented applications**
- **Built-in look-ahead carry capability**
- **Center power pins to reduce effects of package inductance**
- **Count frequency 145MHz typical**
- **Supply current 90mA typical**
- **See 'F269 for 24 pin separate I/O port version**
- **See 'F579 for 20 pin version**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F779/779A	145MHz	90mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F779N, N74F779AN
16-Pin Plastic SOL	N74F779D, N74F779AD

DESCRIPTION

The 74F779/74F779A are fully synchronous 8-stage Up/Down Counter with multiplexed 3-state I/O ports for bus-oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pins (S_0,S_1). The device also features carry look-ahead for easy cascading. All state changes are initiated by the rising edge of the clock. When $\overline{\text{CET}}$ is High the data outputs are held in their current state and $\overline{\text{TC}}$ is held High. The $\overline{\text{TC}}$ output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

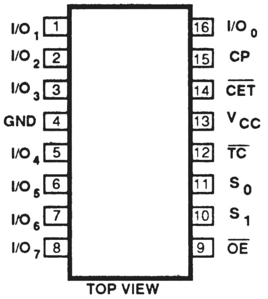
The 74F779A differs from 74F779 in that it has an additional hold mode as described in the Function Table.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/O_n	Data inputs	3.5/1.0	70μA/0.6mA
	Data outputs	150/40	3.0mA/24mA
S_0,S_1	Select inputs	1.0/1.0	20μA/0.6mA
$\overline{\text{OE}}$	Output enable input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{\text{CET}}$	Count Enable Trickle input (active Low)	1.0/1.0	20μA/0.6mA
CP	Clock input	1.0/1.0	20μA/0.6mA
$\overline{\text{TC}}$	Terminal count output (active Low)	50/33	1.0mA/20mA

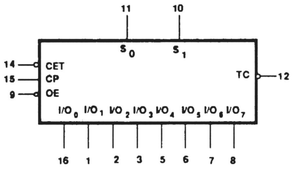
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



I/O_1 1
I/O_2 2
I/O_3 3
GND 4
I/O_4 5
I/O_5 6
I/O_6 7
I/O_7 8
16 I/O_0
15 CP
14 $\overline{\text{CET}}$
13 V_{CC}
12 $\overline{\text{TC}}$
11 S_0
10 S_1
9 $\overline{\text{OE}}$
TOP VIEW

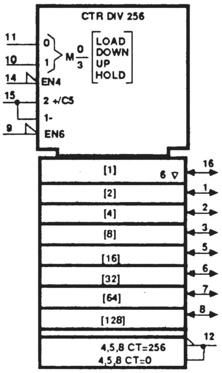
LOGIC SYMBOL



11
10
S_0
S_1
14 CET
15 CP
9 OE
TC 12
I/O_0 I/O_1 I/O_2 I/O_3 I/O_4 I/O_5 I/O_6 I/O_7
16 1 2 3 5 6 7 8

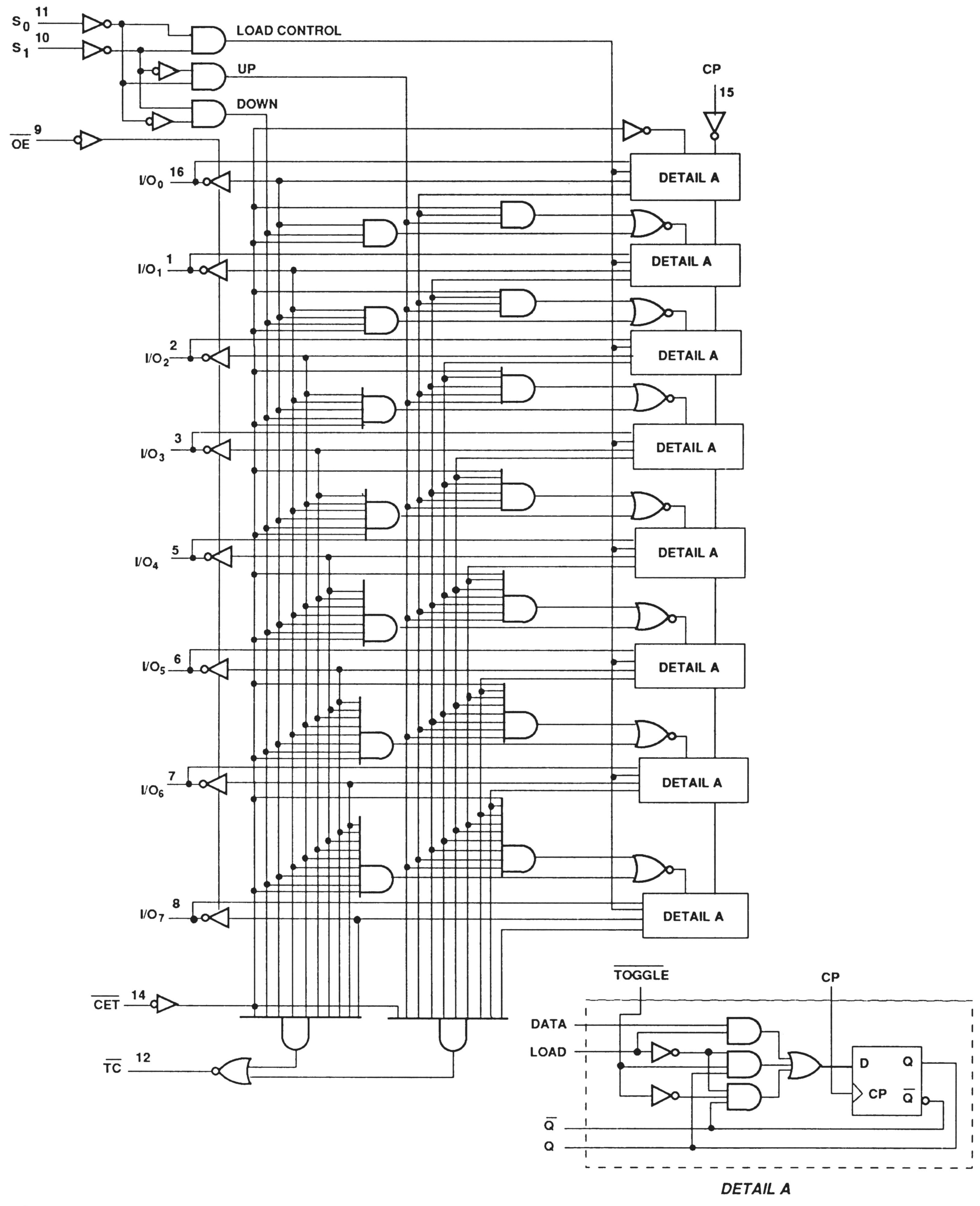
V_{CC} = Pin 13
GND = Pin 4

LOGIC SYMBOL(IEEE/IEC)



CTR DIV 256
11
10
0
1
M $\frac{0}{3}$
LOAD
DOWN
UP
HOLD
14 EN4
15 2 +/C5
1-
9 EN6
[1] 6 ▽
[2]
[4]
[8]
[16]
[32]
[64]
[128]
16
1
2
3
5
6
7
8
4,5,8 CT=256
4,5,8 CT=0
12

LOGIC DIAGRAM


S0
11
S1
10
LOAD CONTROL
UP
DOWN
OE
9
CP
15
I/O0
16
I/O1
1
I/O2
2
I/O3
3
I/O4
5
I/O5
6
I/O6
7
I/O7
8
DETAIL A
CET
14
TC
12
TOGGLE
CP
DATA
LOAD
D
Q
CP
Q̄
Q̄
Q
DETAIL A

V_{CC} = pin 13
GND= pin 4

FUNCTION TABLE

INPUTS					OPERATING MODE
S_1	S_0	$\overline{CET}$	$\overline{OE}$	CP	
X	X	X	H	X	I/O_0 to I/O_7 in high impedance
X	X	X	L	X	Flip-flop outputs appears on I/O lines
L	L	X	H	↑	Parallel load all flip-flops
(not LL)		H	X	↑	Hold ($\overline{TC}$ held High)
H	H	X	X	↑	Hold (for 779A only)
H	L	L	X	↑	Count up
L	H	L	X	↑	Count down

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
(not LL) = S_0 and S_1 should never be Low voltage level at the same time in the hold mode only.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	$\overline{TC}$	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	$\overline{TC}$			-1	mA
		I/O_n			-3	mA
I_{OL}	Low-level output current	$\overline{TC}$			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$\overline{TC}$	V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OL}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O_n		I_{OL}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage	I/O_n	V_{CC} = 5.5V, V_I = 5.5V					1	mA
		others	V_{CC} = 5.5V, V_I =7.0V					100	μA
I_{IH}	High-level input current	except I/O_n	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
$I_{IH}+I_{OZH}$	Off-state output current High-level voltage applied	I/O_n	V_{CC} = MAX, V_O= 2.7V					70	μA
$I_{IL}+I_{OZL}$	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-600	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				82	116	mA
		I_{CCL}					91	128	mA
		I_{CCZ}					97	136	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

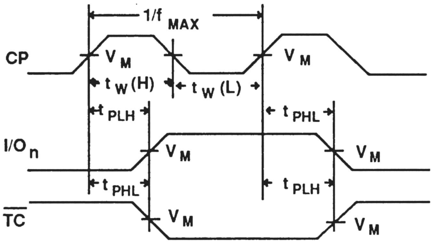
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	limits					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	125	145		115		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	4.5 5.5	7.0 8.0	10.5 10.5	4.5 5.5	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	4.5 4.5	7.0 7.0	9.0 9.0	4.5 4.5	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	3.0 3.0	4.5 5.5	6.5 7.5	2.5 2.5	7.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time from High or Low level	Waveform 4 Waveform 5	1.0 1.0	3.0 4.0	6.5 7.0	1.0 1.0	8.0 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 4 Waveform 5	2.5 4.5	4.5 6.5	7.0 9.0	2.5 4.5	8.0 8.5	ns

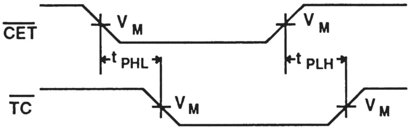
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n to CP	Waveform 3	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CET}$ to CP	Waveform 3	5.0 5.5			5.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CET}$ to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_n to CP	Waveform 3	8.0 8.0			8.5 8.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_n to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 4.0			4.0 4.0		ns

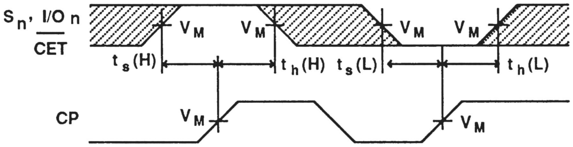
AC WAVEFORMS


1/f MAX
CP
V M
t W (H)
t W (L)
t PLH
t PHL
I/O n
TC
V M

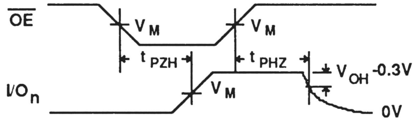
Waveform 1.
Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency


CET
V M
t PHL
t PLH
TC
V M

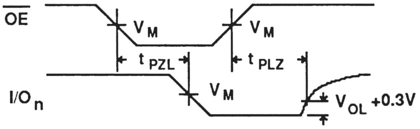
Waveform 2.
Propagation Delay, CET input to Terminal Count Output


S n, I/O n
CET
V M
t s (H)
t h (H)
t s (L)
t h (L)
CP
V M

Waveform 3. Data Setup And Hold Times


OE
V M
t PZH
t PHZ
V OH -0.3V
I/O n
0V

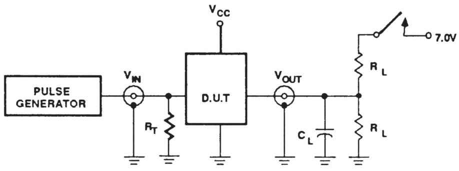
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level


OE
V M
t PZL
t PLZ
I/O n
V OL +0.3V

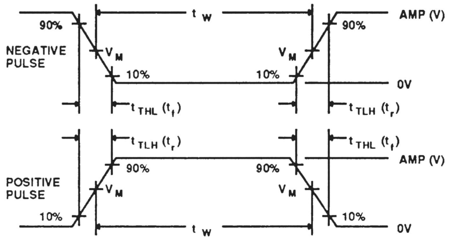
Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V CC
7.0V
R L
PULSE GENERATOR
V IN
D.U.T
V OUT
R T
C L
R L

Test Circuit For 3-State Outputs


t w
90%
AMP (V)
NEGATIVE PULSE
V M
10%
0V
t THL (t f)
t TLH (t r)
POSITIVE PULSE
90%
10%
AMP (V)
0V

V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F786

4-Input Asynchronous Bus Arbiter

Product Specification

TYPE	TYPICAL PROP DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F786	6.6ns	55mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC}=5V\pm10\%$; $T_A=0°C$ to $+70°C$
16-Pin Plastic DIP	74F786N
16-Pin Plastic SO	74F786D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{BR}_1$ - $\overline{BR}_4$	Bus Request inputs (active Low)	1.0/3.0	20µA/1.8mA
A, B, C, D	AND gate inputs	1.0/1.0	20µA/0.6mA
$\overline{EN}$	Common Bus Grant output enable input (active Low)	1.0/1.0	20µA/0.6mA
Y_{OUT}	AND gate output	150/40	3.0mA/24mA
$\overline{BG}_1$ - $\overline{BG}_4$	Bus Grant outputs (active Low)	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

FEATURES

- **Arbitrates between 4 asynchronous inputs**
- **Separate grant output for each input**
- **Common output enable**
- **On-board 4 input AND gate**
- **Metastable-free outputs**

DESCRIPTION

The 74F786 is an asynchronous 4-bit arbiter designed for high speed real-time applications. The priority of arbitration is determined on a first-come first-served basis. Separate Bus Grant ($\overline{BG}_n$) outputs are available to indicate which one of the request inputs is served by the arbitration logic. All $\overline{BG}_n$ outputs are enabled by a common enable ($\overline{EN}$) pin. In order to generate a bus request signal, a separate 4-input AND gate is provided which may also be used as an independent AND gate. Unused Bus Request ($\overline{BR}_n$) inputs may be disabled by tying them High.

The 'F786 is designed so that contention between two or more $\overline{BR}_n$ inputs will not cause the $\overline{BG}_n$ outputs to glitch or display a metastable condition. In this situation however, an increase in the $\overline{BR}_n$ to $\overline{BG}_n$ propagation delay (t_{PHL}) may be observed. A typical 'F786 has an h = 6.6ns, τ = .41ns and T_0 = 5µsec. Where:

h= Typical propagation delay through the device.

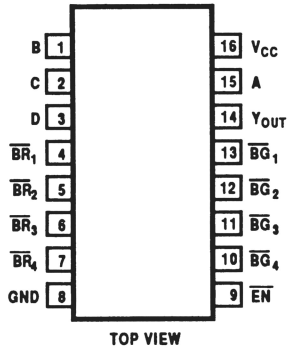
τ= Rate at which a latch in a metastable state resolves that condition.

& T_0= The measurement of the propensity of a latch to enter a metastable state.

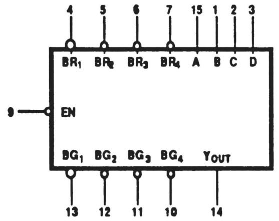
For further information, please refer to the 'F786 application note.

The $\overline{BR}_n$ inputs have no inherent priority. The arbiter assigns priority to the incoming requests as they are received, therefore, the first $\overline{BR}_n$ asserted will have the highest priority. When a bus request is received its corresponding bus grant becomes active, provided that $\overline{EN}$ is Low. If additional bus requests are made during this time they are queued. When the first request is removed, the arbiter services the bus request with the next highest priority. If a request is removed while a previous request is being serviced, it loses its priority. For example, if $\overline{BR}_1$ is the first request received, followed by $\overline{BR}_2$ and finally by $\overline{BR}_3$, $\overline{BR}_2$ will have priority over $\overline{BR}_3$. However, if $\overline{BR}_2$ is removed before $\overline{BR}_1$ is negated, it will lose its place and $\overline{BR}_3$ will become next in priority. If three or more requests are asserted precisely at the same time, and one of them is re-

PIN CONFIGURATION



LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

moved prior to being serviced, it may cause premature termination of the present grant and assertion of another grant. Therefore, the user should not remove ungranted requests when arbitrating between three or four requests. This does not apply to arbitration between two requests.

If two or more $\overline{BR}_n$ inputs are asserted at precisely the same time, one of them will be selected at random, and all $\overline{BG}_n$ outputs will be held in the High state until the selection is made. This guarantees that an erroneous $\overline{BG}_n$ will not be generated even though a metastable condition may occur internal to the device.

When the $\overline{EN}$ input is High, all $\overline{BG}_n$ outputs are forced High.

PIN DESCRIPTION

SYMBOL	PINS	TYPE	NAME AND FUNCTION
$\overline{BR}_1$ - $\overline{BR}_4$	4 - 7	I	Bus Request inputs (Active Low) - The logic of this device arbitrates between these four inputs. Unused inputs should be tied high.
$\overline{BG}_1$ - $\overline{BG}_4$	13 - 10	O	Bus Grant outputs (Active Low) - These outputs indicate the selected bus request. $\overline{BG}_1$ corresponds to $\overline{BR}_1$, $\overline{BG}_2$ to $\overline{BR}_2$, etc1
A, B, C, D	15, 1 - 3	I	Inputs of the 4-input AND gate.
Y_{OUT}	14	O	Output of the 4-input AND gate.
$\overline{EN}$	9	I	Enable input - When Low it enables the $\overline{BR}_1$ - $\overline{BR}_4$ outputs.

ARBITER FUNCTION TABLE

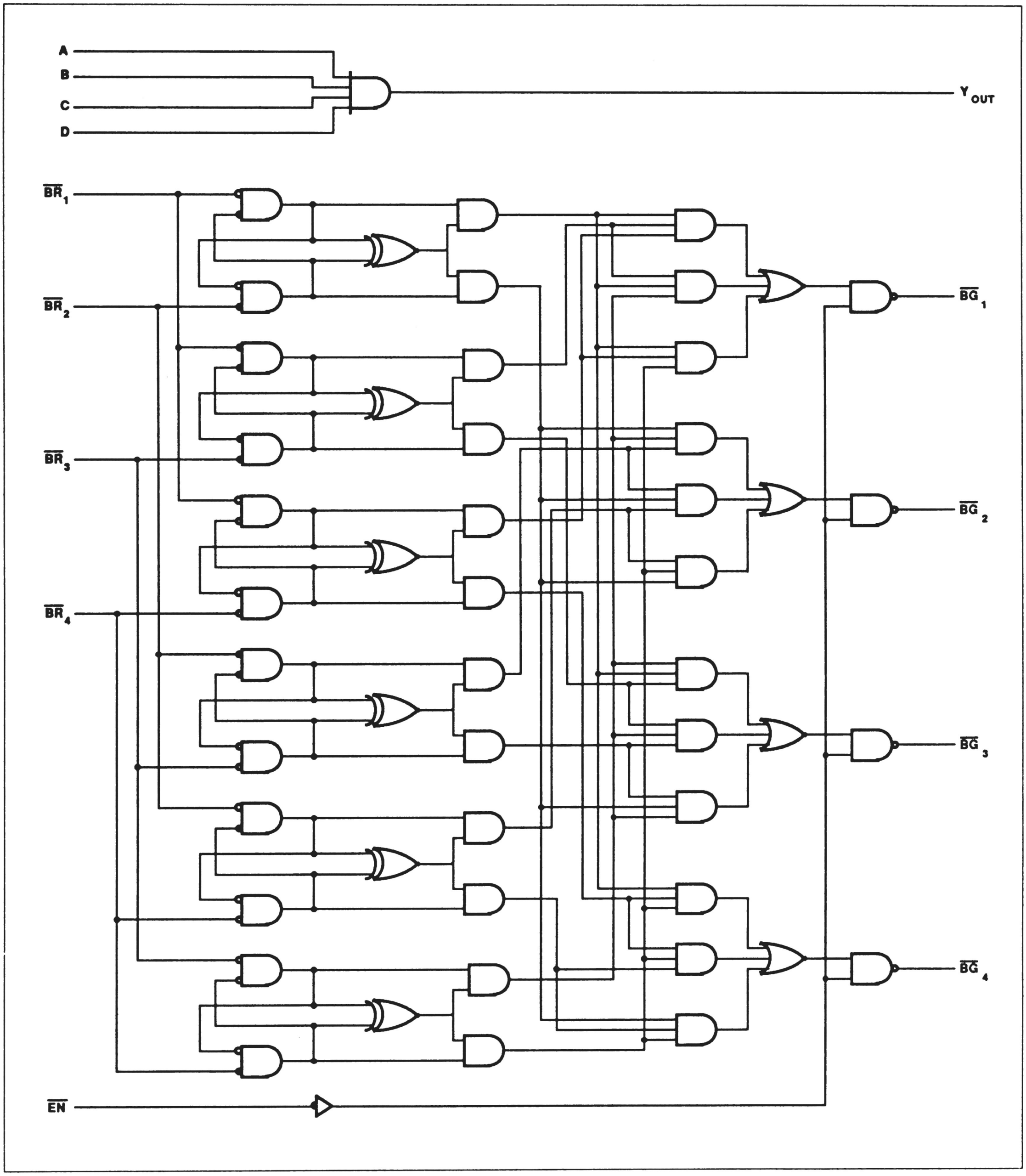
INPUTS					OUTPUTS			
$\overline{EN}$	$\overline{BR}_1$	$\overline{BR}_2$	$\overline{BR}_3$	$\overline{BR}_4$	$\overline{BG}_1$	$\overline{BG}_2$	$\overline{BG}_3$	$\overline{BG}_4$
L	1	X	X	X	L	H	H	H
L	X	1	X	X	H	L	H	H
L	X	X	1	X	H	H	L	H
L	X	X	X	1	H	H	H	L
H	X	X	X	X	H	H	H	H

L = Low voltage level
H = High voltage level
X = Don't care
1 = First of inputs to go Low

AND FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y_{OUT}
L	L	L	L	L
L	L	L	H	L
L	L	H	L	L
L	L	H	H	L
L	H	L	L	L
L	H	L	H	L
L	H	H	L	L
L	H	H	H	L
H	L	L	L	L
H	L	L	H	L
H	L	H	L	L
H	L	H	H	L
H	H	L	L	L
H	H	L	H	L
H	H	H	L	L
H	H	H	H	H

LOGIC DIAGRAM


A
B
C
D
Y_{OUT}
$\overline{BR}_1$
$\overline{BR}_2$
$\overline{BR}_3$
$\overline{BR}_4$
$\overline{BG}_1$
$\overline{BG}_2$
$\overline{BG}_3$
$\overline{BG}_4$
$\overline{EN}$

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	A-D, $\overline{EN}$	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		$\overline{BR}_n$					-1.8	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			55	80	mA

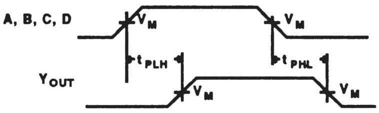
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

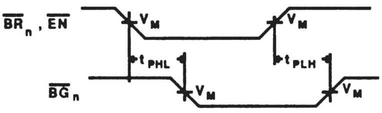
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D to Y_{OUT}	Waveform 1	2.5 2.5	4.5 4.5	7.5 7.5	2.0 2.5	8.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{BR}_n$ to $\overline{BG}_n$	Waveform 2	5.0 4.5	7.0 6.5	10.0 9.5	4.5 4.0	10.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EN}$ to $\overline{BG}_n$	Waveform 2	3.0 2.5	5.0 4.5	8.0 7.5	2.5 2.5	8.5 8.0	ns
t_{PHL}	Propagation delay, $\overline{BR}_a$ to $\overline{BG}_b$	Waveform 3	5.0	7.0	10.0	4.5	10.5	ns

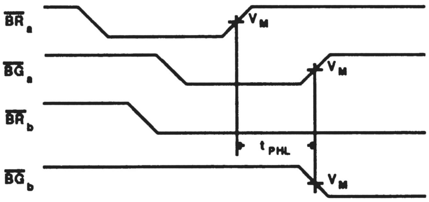
AC WAVEFORMS


A, B, C, D
V_M
V_M
t_{PLH}
t_{PHL}
Y_{OUT}
V_M
V_M

Waveform 1. AND Gate Input to Output Delays


$\overline{BR}_n$, $\overline{EN}$
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{BG}_n$
V_M
V_M

Waveform 2. Bus Request or Enable to Bus Grant Delays

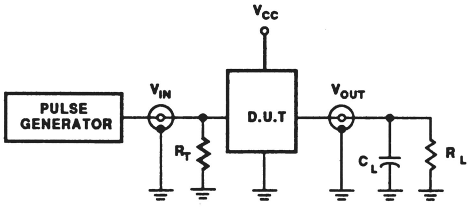

$\overline{BR}_a$
V_M
$\overline{BG}_a$
V_M
$\overline{BR}_b$
t_{PHL}
$\overline{BG}_b$
V_M

Waveform 3. Bus Request to Bus Grant Delay

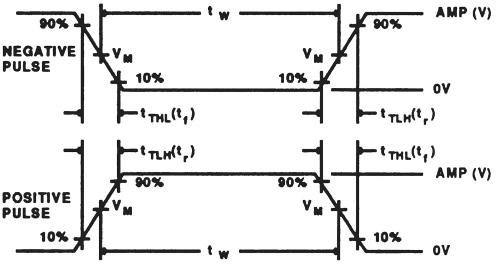
NOTE: a and b represent any of the Bus Requests or Grants. $\overline{BG}_a$ Low-to-High transition and the $\overline{BG}_b$ High-to-Low transition occur simultaneously.

For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
V_{IN}
PULSE GENERATOR
D.U.T
V_{OUT}
R_T
C_L
R_L

Test Circuit For Totem-Pole Outputs


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
V_M
t_W
t_{THL}(t_f)
t_{TLH}(t_r)
AMP (V)
0V

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	**Rep. Rate**	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F804, F1804
NAND DRIVERS

74F804-Hex Two-Input NAND Driver
74F1804-Hex Two-Input NAND Driver
Product Specification

FEATURES

- **High capacitive drive capability**
- **Choice of configuration**
  Corner V_{CC} and GND-- 'F804
  Center V_{CC} and GND-- 'F1804
- **Typical propagation delay of 2.5ns**

TYPE	TYPICAL PRPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F804	2.5ns	9mA
74F1804	2.5ns	9mA

ORDERING INFORMATION

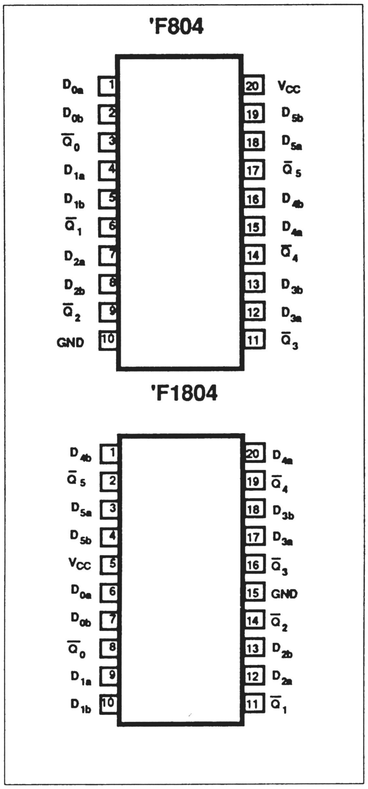
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F804N, N74F1804N
20-Pin Plastic SOL	N74F804D, N74F1804D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

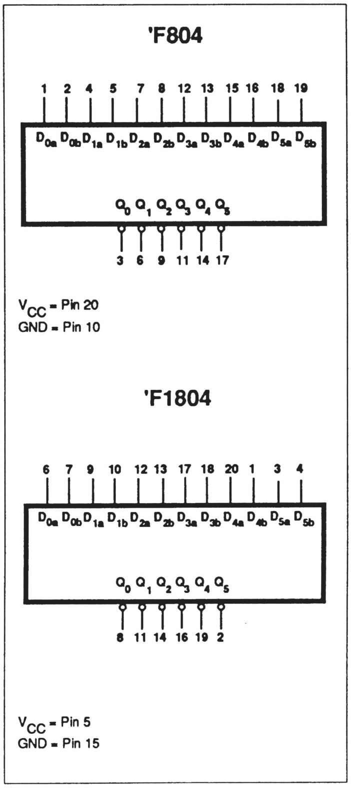
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na} - D_{nb}	Data inputs	1.0/0.033	20µA/20µA
$\overline{Q}_0$ - $\overline{Q}_5$	Data outputs	2400/80	48mA/48mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION


'F804
D0a 1
D0b 2
Q̄0 3
D1a 4
D1b 5
Q̄1 6
D2a 7
D2b 8
Q̄2 9
GND 10
20 VCC
19 D5b
18 D5a
17 Q̄5
16 D4b
15 D4a
14 Q̄4
13 D3b
12 D3a
11 Q̄3
'F1804
D4b 1
Q̄5 2
D5a 3
D5b 4
VCC 5
D0a 6
D0b 7
Q̄0 8
D1a 9
D1b 10
20 D4a
19 Q̄4
18 D3b
17 D3a
16 Q̄3
15 GND
14 Q̄2
13 D2b
12 D2a
11 Q̄1

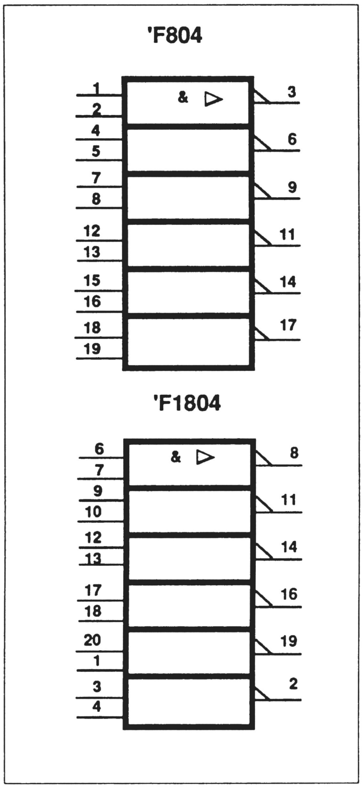
LOGIC SYMBOL


'F804
1 2 4 5 7 8 12 13 15 16 18 19
D0a D0b D1a D1b D2a D2b D3a D3b D4a D4b D5a D5b
Q0 Q1 Q2 Q3 Q4 Q5
3 6 9 11 14 17
'F1804
6 7 9 10 12 13 17 18 20 1 3 4
D0a D0b D1a D1b D2a D2b D3a D3b D4a D4b D5a D5b
Q0 Q1 Q2 Q3 Q4 Q5
8 11 14 16 19 2

V_{CC} = Pin 20
GND = Pin 10

V_{CC} = Pin 5
GND = Pin 15

LOGIC SYMBOL(IEEE/IEC)


'F804
& ▷
1 2 → 3
4 5 → 6
7 8 → 9
12 13 → 11
15 16 → 14
18 19 → 17
'F1804
& ▷
6 7 → 8
9 10 → 11
12 13 → 14
17 18 → 16
20 1 → 19
3 4 → 2

FUNCTION TABLE

INPUTS		OUTPUT
Da	Db	$\overline{Q}$
L	X	H
X	L	H
H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	96	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-48	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.0			V
				±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.38	0.55	V
				±5%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input clamp current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-20	μA
I_O	Output current[3]		V_{CC} = MAX, V_O=2.25V		-60		-160	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} =GND		2.0	3.0	mA
		I_{CCL}		V_{IN} =4.5V		15	20	mA

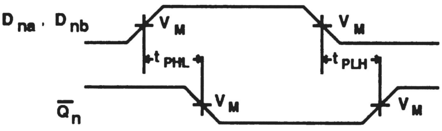
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to $\overline{Q}_n$	Waveform 1	1.0 1.0	2.0 3.0	4.0 4.5	1.0 1.0	4.0 5.0	ns

AC WAVEFORMS

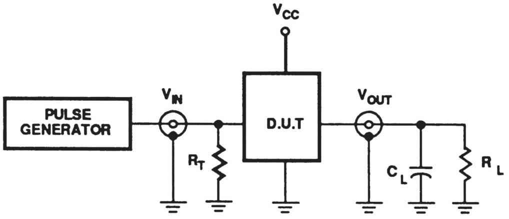

D na , D nb
V M
t PHL
t PLH
V M
Q̄n
V M
V M

Waveform 1.

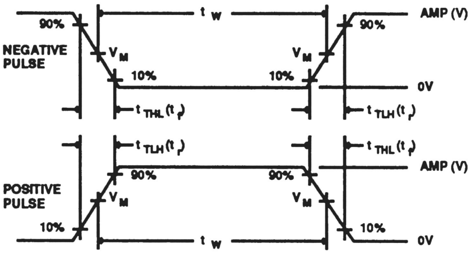
Propagation Delay for Input to Output

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
VIN
VOUT
PULSE GENERATOR
D.U.T
RT
CL
RL

Test Circuit For Totem-Pole Outputs


tw
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tw

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAST 74F805, 74F1805

NOR Drivers

74F805-Hex Two-Input NOR Driver
74F1805-Hex Two-Input NOR Driver
Preliminary Specification

FEATURES

- **High capacitive drive capability**
- **Choice of configuration**
  Corner V_{CC} and GND-- 'F805
  Center V_{CC} and GND-- 'F1805
- **Typical propagation delay of 2.6ns**

TYPE	TYPICAL PRPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F805	2.6ns	11mA
74F1805	2.6ns	11mA

ORDERING INFORMATION

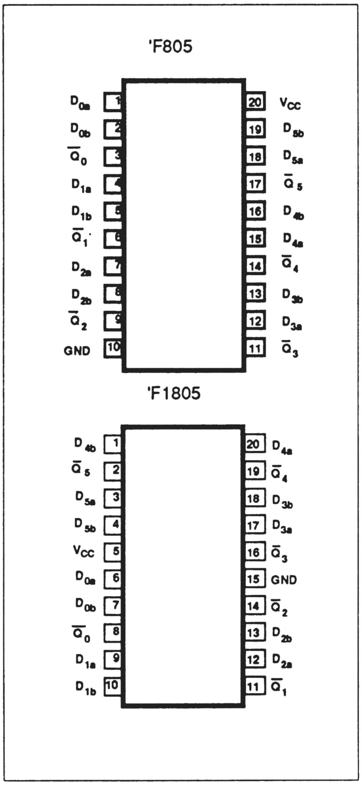
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F805N, N74F1805N
20-Pin Plastic SOL	N74F805D, N74F1805D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

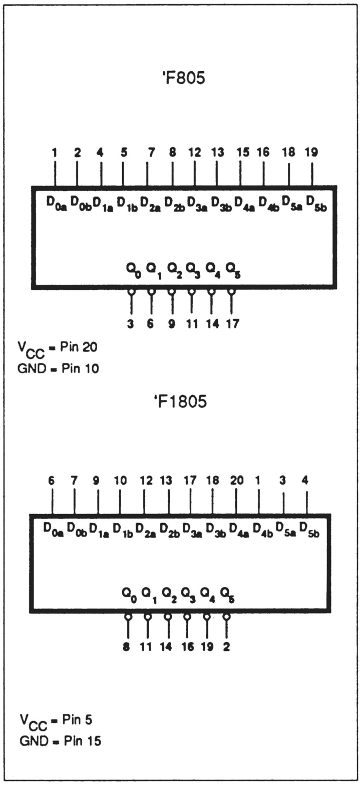
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na} - D_{nb}	Data inputs	1.0/0.033	20µA/20µA
$\overline{Q}_0$ - $\overline{Q}_5$	Data outputs	2400/80	48mA/48mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

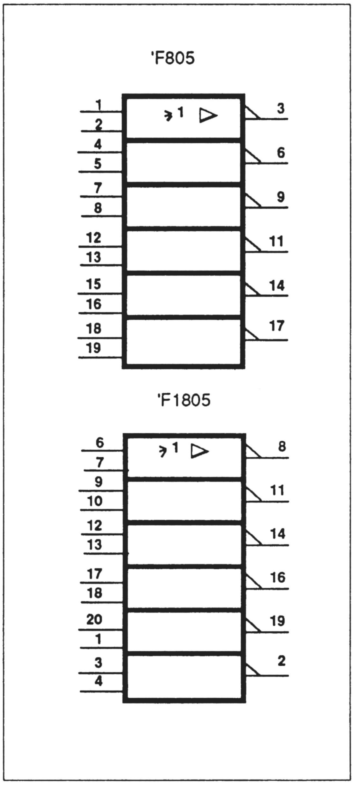
PIN CONFIGURATION


'F805
D0a 1
D0b 2
Q̄0 3
D1a 4
D1b 5
Q̄1 6
D2a 7
D2b 8
Q̄2 9
GND 10
20 VCC
19 D5b
18 D5a
17 Q̄5
16 D4b
15 D4a
14 Q̄4
13 D3b
12 D3a
11 Q̄3
'F1805
D4b 1
Q̄5 2
D5a 3
D5b 4
VCC 5
D0a 6
D0b 7
Q̄0 8
D1a 9
D1b 10
20 D4a
19 Q̄4
18 D3b
17 D3a
16 Q̄3
15 GND
14 Q̄2
13 D2b
12 D2a
11 Q̄1

LOGIC SYMBOL


'F805
1 2 4 5 7 8 12 13 15 16 18 19
D0a D0b D1a D1b D2a D2b D3a D3b D4a D4b D5a D5b
Q0 Q1 Q2 Q3 Q4 Q5
3 6 9 11 14 17
VCC = Pin 20
GND = Pin 10
'F1805
6 7 9 10 12 13 17 18 20 1 3 4
D0a D0b D1a D1b D2a D2b D3a D3b D4a D4b D5a D5b
Q0 Q1 Q2 Q3 Q4 Q5
8 11 14 16 19 2
VCC = Pin 5
GND = Pin 15

LOGIC SYMBOL(IEEE/IEC)


'F805
≥1
1 2 3
4 5 6
7 8 9
12 13 11
15 16 14
18 19 17
'F1805
≥1
6 7 8
9 10 11
12 13 14
17 18 16
20 1 19
3 4 2

January 14, 1988

FUNCTION TABLE

INPUTS		OUTPUT
D_{na}	D_{nb}	$\overline{Q}_n$
H	X	L
X	H	L
L	L	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	96	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-48	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.0			V
				±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.38	0.55	V
				±5%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input clamp current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-20	μA
I_O	Output current[3]		V_{CC} = MAX, V_O=2.25V		-60		-160	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} =GND		5	9	mA
		I_{CCL}		V_{IN} =4.5V		18	32	mA

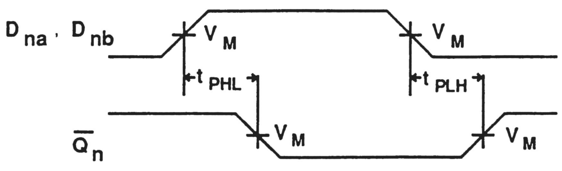
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to $\overline{Q}_n$	Waveform 1	1.0 1.0	1.7 1.6	3.5 3.5	1.0 1.0	4.0 4.0	ns

AC WAVEFORMS

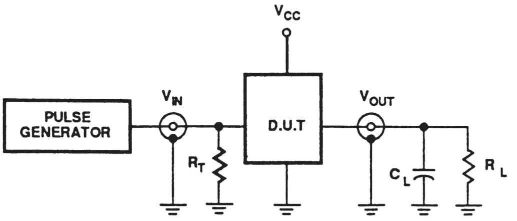

D na , D nb
V M
t PHL
V M
t PLH
Q̄ n
V M
V M

Waveform 1.

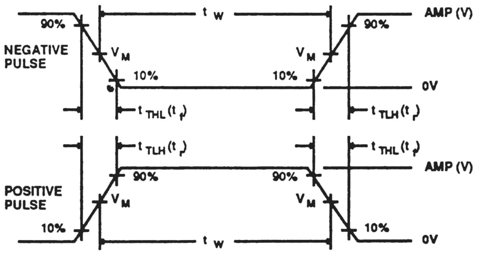
Propagation Delay for Input to Output

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
RT
D.U.T
VOUT
CL
RL

Test Circuit For Totem-Pole Outputs


tW
90%
AMP (V)
NEGATIVE PULSE
VM
10%
0V
tTHL (tf)
tTLH (tr)
POSITIVE PULSE
90%
AMP (V)
VM
10%
0V
tW

V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F808, 74F1808
AND DRIVERS

74F808-Hex Two-Input AND Driver
74F1808-Hex Two-Input AND Driver
Preliminary Specification

FEATURES

- High capacitive drive capability
- Choice of configuration
  Corner V_{CC} and GND-- 'F808
  Center V_{CC} and GND-- 'F1808
- Typical propagation delay of 2.6ns

TYPE	TYPICAL PRPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F808	2.6ns	11mA
74F1808	2.6ns	11mA

ORDERING INFORMATION

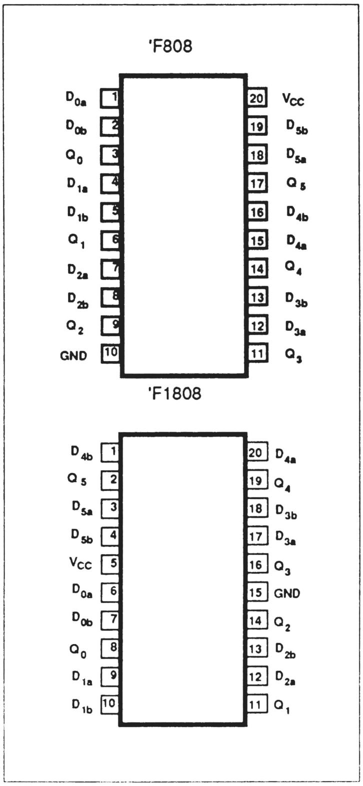
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F808N, N74F1808N
20-Pin Plastic SOL	N74F808D, N74F1808D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

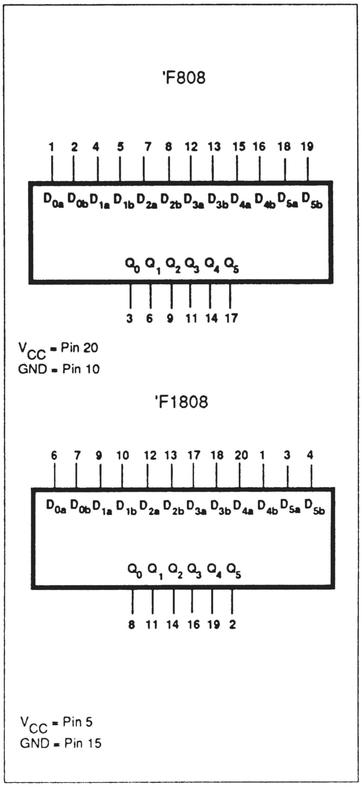
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na} - D_{nb}	Data inputs	1.0/0.033	20μA/20μA
Q_0 - Q_5	Data outputs	2400/80	48mA/48mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

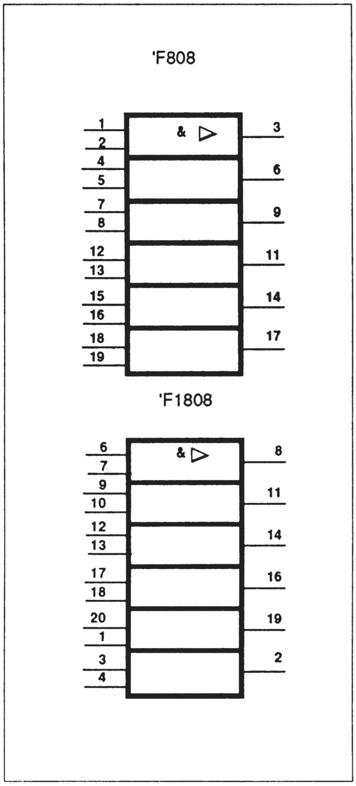
PIN CONFIGURATION


'F808
D0a 1
D0b 2
Q0 3
D1a 4
D1b 5
Q1 6
D2a 7
D2b 8
Q2 9
GND 10
20 VCC
19 D5b
18 D5a
17 Q5
16 D4b
15 D4a
14 Q4
13 D3b
12 D3a
11 Q3
'F1808
D4b 1
Q5 2
D5a 3
D5b 4
VCC 5
D0a 6
D0b 7
Q0 8
D1a 9
D1b 10
20 D4a
19 Q4
18 D3b
17 D3a
16 Q3
15 GND
14 Q2
13 D2b
12 D2a
11 Q1

LOGIC SYMBOL


'F808
1 2 4 5 7 8 12 13 15 16 18 19
D0a D0b D1a D1b D2a D2b D3a D3b D4a D4b D5a D5b
Q0 Q1 Q2 Q3 Q4 Q5
3 6 9 11 14 17
VCC = Pin 20
GND = Pin 10
'F1808
6 7 9 10 12 13 17 18 20 1 3 4
D0a D0b D1a D1b D2a D2b D3a D3b D4a D4b D5a D5b
Q0 Q1 Q2 Q3 Q4 Q5
8 11 14 16 19 2
VCC = Pin 5
GND = Pin 15

LOGIC SYMBOL(IEEE/IEC)


'F808
&
1 2 3
4 5 6
7 8 9
12 13 11
15 16 14
18 19 17
'F1808
&
6 7 8
9 10 11
12 13 14
17 18 16
20 1 19
3 4 2

FUNCTION TABLE

INPUTS		OUTPUT
D_{na}	D_{nb}	Q_n
L	X	L
X	L	L
H	H	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	96	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-48	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.0			V
				±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.38	0.55	V
				±5%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input clamp current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-20	µA
I_O	Output current[3]		V_{CC} = MAX, V_O=2.25V		-60		-160	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} =GND		6.5	11	mA
		I_{CCL}		V_{IN} =4.5V		19	32	mA

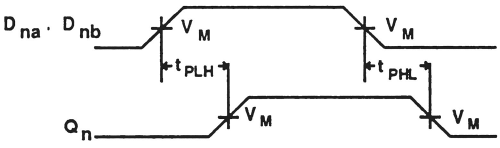
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to Q_n	Waveform 1	1.0 1.0	2.5 2.4	4.5 4.5	1.0 1.0	5.0 5.0	ns

AC WAVEFORMS



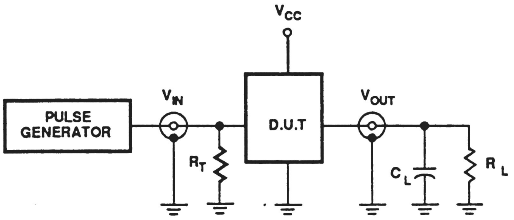
D na · D nb
V M
V M
t PLH
t PHL
Q n
V M
V M

Waveform 1.

Propagation Delay for Input to Output

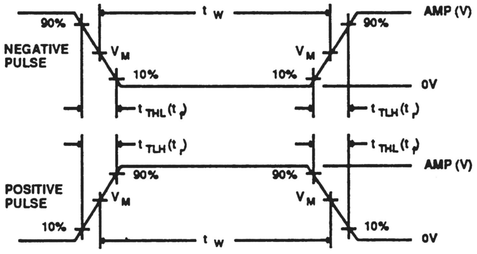
NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



V CC
PULSE GENERATOR
V IN
R T
D.U.T
V OUT
C L
R L

Test Circuit For Totem-Pole Outputs



t W
AMP (V)
90%
90%
NEGATIVE PULSE
V M
V M
10%
10%
0V
t THL (t f)
t TLH (t r)
t TLH (t r)
t THL (t f)
AMP (V)
90%
90%
POSITIVE PULSE
V M
V M
10%
10%
t W
0V

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAST 74F821/822/823/ 824/825/826

Bus Interface Registers

'F821/'F822 10-Bit Bus Interface Registers, NINV/INV (3-State)
'F823/'F824 9-Bit Bus Interface Registers, NINV/INV (3-State)
'F825/'F826 8-Bit Bus Interface Registers, NINV/INV (3-State)
Product Specification

FEATURES

- **High speed parallel registers with positive edge-triggered D-type flip-flops**
- **High performance bus interface buffering for wide data/address paths or busses carrying parity**
- **High impedance PNP base inputs for reduced loading (20µA in High and Low states)**
- **I_{IL} is 20µA vs 1000µA for AM29821 series**
- **Buffered control inputs to reduce AC effects**
- **Ideal where high speed, light loading, or increased fan-in as required with MOS microprocessors**
- **Positive and negative over-shoots are clamped to ground**
- **3-state outputs glitch free during power-up and power-down**
- **Slim Dip 300 mil package**
- **Broadside pinout compatible with AMD AM 29821-29826 series**
- **Outputs sink 64mA and source 24mA**

DESCRIPTION

The 74F821 series Bus Interface Registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of busses carrying parity.

The 'F821/'F822 are buffered 10-bit wide versions of the popular 'F374/'F534 functions.
The 'F822 is the inverted output version of 'F821.

The74F823 and 74F824 are 9-bit wide buffered registers with Clock Enable($\overline{CE}$) and Master Reset ($\overline{MR}$) which are ideal for parity bus interfacing in high microprogrammed systems.
The 'F 824 is the inverted output version of 'F823.

The74F825 and 74F826 are 8-bit buffered registers with all the 'F823/'F824 controls plus Output Enable ($\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring High I_{OL}/I_{OH}.
The 'F826 is the inverted output version of 'F825.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F821, 74F822	180MHz	75mA
74F823, 74F824	180MHz	70mA
74F825, 74F826	180MHz	65mA

ORDERING INFORMATION

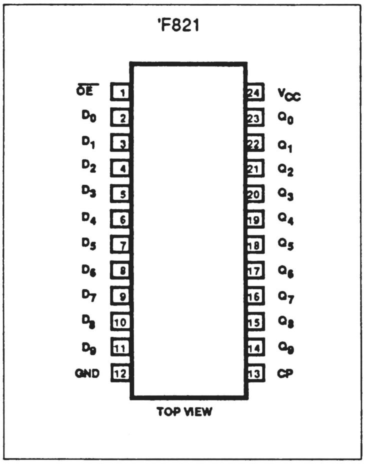
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic SLIM DIP (300mil)	N74F821N, N74F822N, N74F823N, N74F824N, N74F825N, N74F826N
24-Pin Plastic SOL	N74F821D, N74F822D, N74F823D, N74F824D, N74F825D, N74F826D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

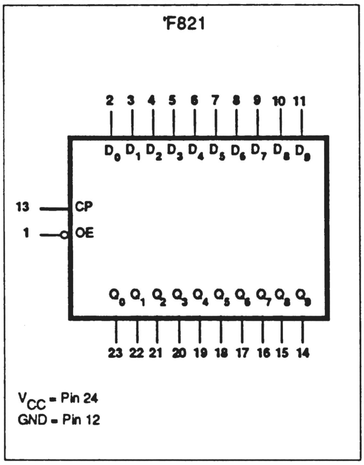
PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F821 'F822	D_n	Data inputs	1.0/0.033	20µA/20µA
	CP	Clock input	1.0/0.033	20µA/20µA
	$\overline{OE}$	Output enable input (activeLow)	1.0/0.033	20µA/20µA
	Q_n, $\overline{Q}_n$	Data output	1200/106.7	24mA/64mA
'F823 'F824	D_n	Data inputs	1.0/0.033	20µA/20µA
	CP	Clock input	1.0/0.033	20µA/20µA
	$\overline{CE}$	Clock enable input (active Low)	1.0/0.033	20µA/20µA
	$\overline{MR}$	Master reset input (active Low)	1.0/0.033	20µA/20µA
	$\overline{OE}$	Output enable input (active Low)	1.0/0.033	20µA/20µA
	Q_n, Q_n	Data outputs	1200/106.7	24mA/64mA
'F825 'F826	D_n	Data inputs	1.0/0.033	20µA/20µA
	CP	Clock input	1.0/0.033	20µA/20µA
	$\overline{CE}$	Clock enable input (active Low)	1.0/0.033	20µA/20µA
	$\overline{MR}$	Master reset input (active Low)	1.0/0.033	20µA/20µA
	$\overline{OE}_n$	Output enable inputs (active Low)	1.0/0.033	20µA/20µA
	Q_n, $\overline{Q}_n$	Data outputs	1200/106.7	24mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

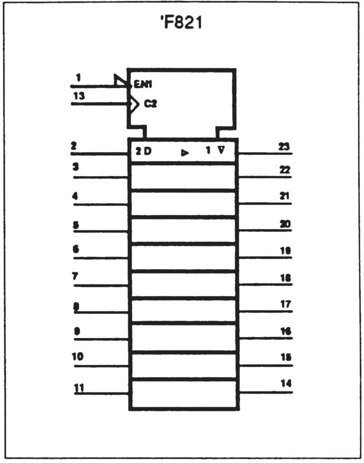

'F821
OE 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
D8 10
D9 11
GND 12
24 VCC
23 Q0
22 Q1
21 Q2
20 Q3
19 Q4
18 Q5
17 Q6
16 Q7
15 Q8
14 Q9
13 CP
TOP VIEW

LOGIC SYMBOL

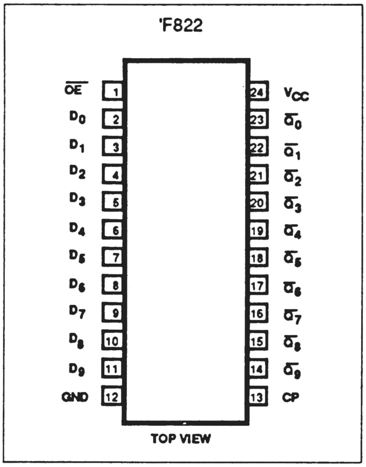

'F821
2 3 4 5 6 7 8 9 10 11
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9
13 CP
1 OE
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9
23 22 21 20 19 18 17 16 15 14

V_{CC} = Pin 24
GND = Pin 12

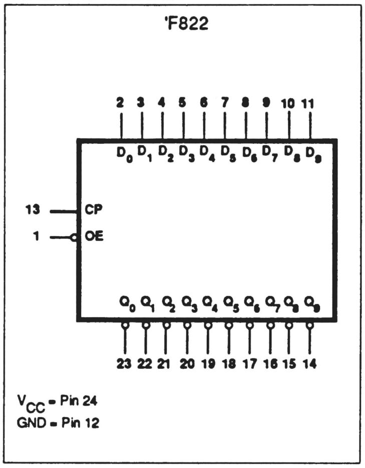
LOGIC SYMBOL(IEEE/IEC)


'F821
1
13
EN1
C2
2D
1
2 3 4 5 6 7 8 9 10 11
23 22 21 20 19 18 17 16 15 14

PIN CONFIGURATION

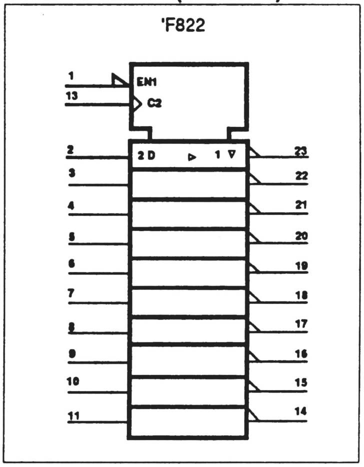

'F822
OE 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
D8 10
D9 11
GND 12
24 VCC
23 Q̄0
22 Q̄1
21 Q̄2
20 Q̄3
19 Q̄4
18 Q̄5
17 Q̄6
16 Q̄7
15 Q̄8
14 Q̄9
13 CP
TOP VIEW

LOGIC SYMBOL

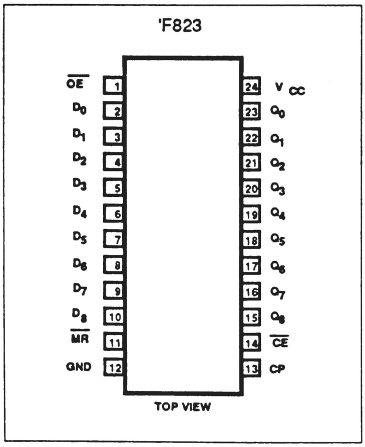

'F822
2 3 4 5 6 7 8 9 10 11
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9
13 CP
1 OE
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9
23 22 21 20 19 18 17 16 15 14

V_{CC} = Pin 24
GND = Pin 12

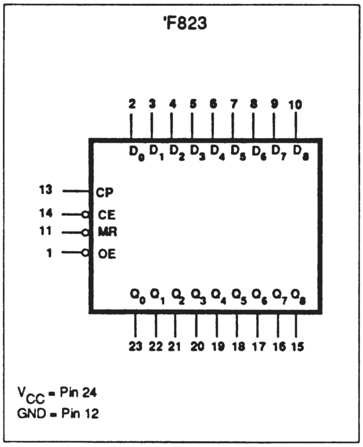
LOGIC SYMBOL(IEEE/IEC)


'F822
1
13
EN1
C2
2D
1
2 3 4 5 6 7 8 9 10 11
23 22 21 20 19 18 17 16 15 14

PIN CONFIGURATION

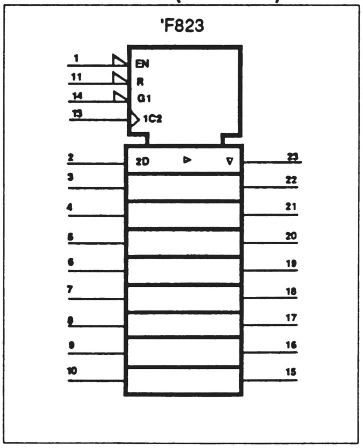

'F823
OE 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
D8 10
MR 11
GND 12
24 VCC
23 Q0
22 Q1
21 Q2
20 Q3
19 Q4
18 Q5
17 Q6
16 Q7
15 Q8
14 CE
13 CP
TOP VIEW

LOGIC SYMBOL

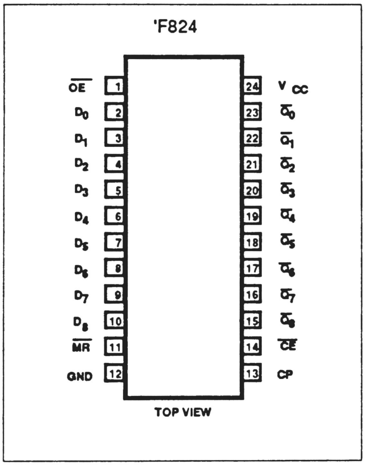

'F823
2 3 4 5 6 7 8 9 10
D0 D1 D2 D3 D4 D5 D6 D7 D8
13 CP
14 CE
11 MR
1 OE
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8
23 22 21 20 19 18 17 16 15

V_{CC} = Pin 24
GND = Pin 12

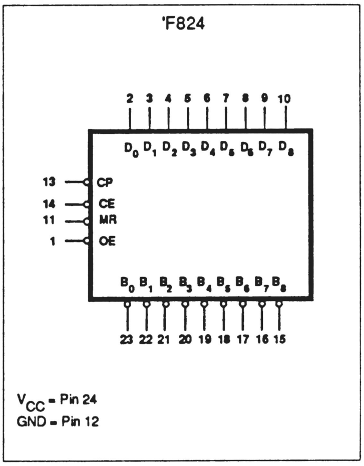
LOGIC SYMBOL(IEEE/IEC)


'F823
1
11
14
13
EN
R
G1
1C2
2D
2 3 4 5 6 7 8 9 10
23 22 21 20 19 18 17 16 15

PIN CONFIGURATION

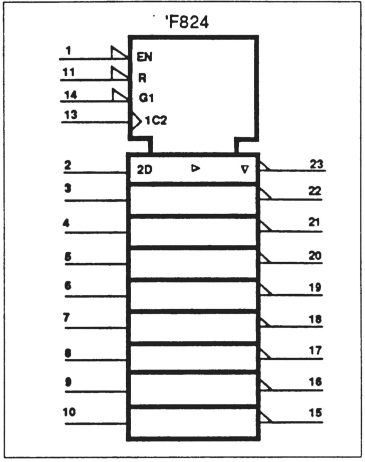

'F824
OE 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
D8 10
MR 11
GND 12
24 VCC
23 Q̄0
22 Q̄1
21 Q̄2
20 Q̄3
19 Q̄4
18 Q̄5
17 Q̄6
16 Q̄7
15 Q̄8
14 CE
13 CP
TOP VIEW

LOGIC SYMBOL

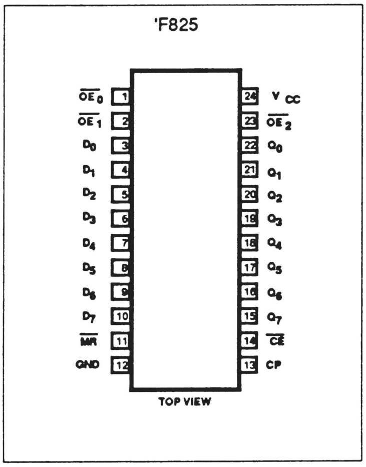

'F824
2 3 4 5 6 7 8 9 10
D0 D1 D2 D3 D4 D5 D6 D7 D8
13 CP
14 CE
11 MR
1 OE
B0 B1 B2 B3 B4 B5 B6 B7 B8
23 22 21 20 19 18 17 16 15

V_{CC} = Pin 24
GND = Pin 12

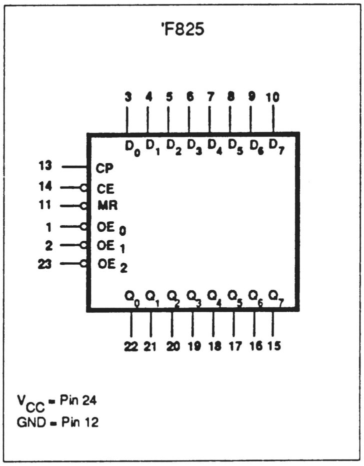
LOGIC SYMBOL(IEEE/IEC)


'F824
1 EN
11 R
14 G1
13 1C2
2 2D
23
3 22
4 21
5 20
6 19
7 18
8 17
9 16
10 15

PIN CONFIGURATION

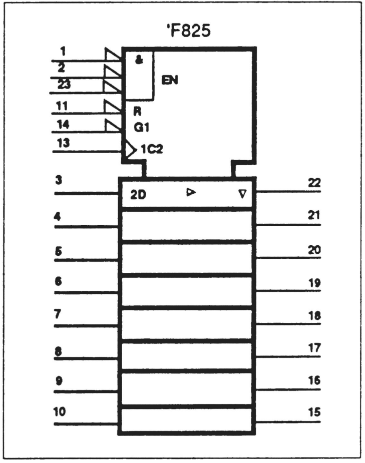

'F825
OE0 1
OE1 2
D0 3
D1 4
D2 5
D3 6
D4 7
D5 8
D6 9
D7 10
MR 11
GND 12
24 VCC
23 OE2
22 Q0
21 Q1
20 Q2
19 Q3
18 Q4
17 Q5
16 Q6
15 Q7
14 CE
13 CP
TOP VIEW

LOGIC SYMBOL

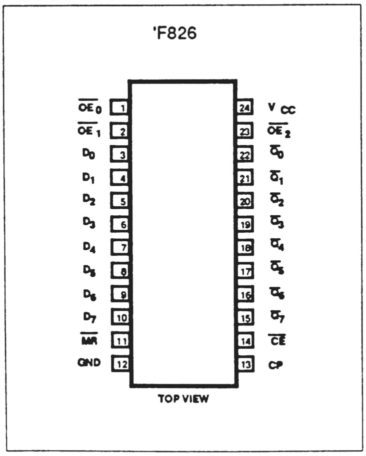

'F825
3 4 5 6 7 8 9 10
D0 D1 D2 D3 D4 D5 D6 D7
13 CP
14 CE
11 MR
1 OE0
2 OE1
23 OE2
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
22 21 20 19 18 17 16 15

V_{CC} = Pin 24
GND = Pin 12

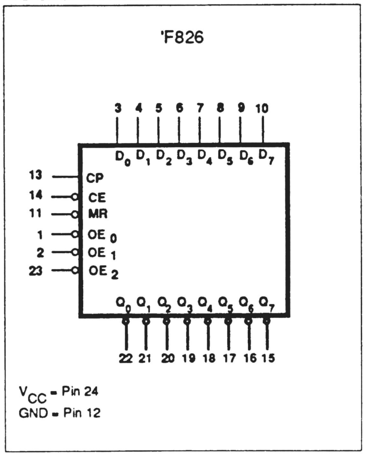
LOGIC SYMBOL(IEEE/IEC)


'F825
1
2
23
&
EN
11 R
14 G1
13 1C2
3 2D
22
4 21
5 20
6 19
7 18
8 17
9 16
10 15

PIN CONFIGURATION

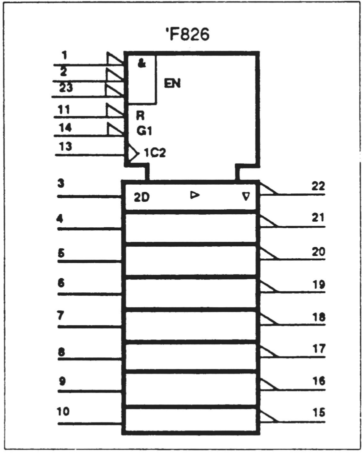

'F826
OE0 1
OE1 2
D0 3
D1 4
D2 5
D3 6
D4 7
D5 8
D6 9
D7 10
MR 11
GND 12
24 VCC
23 OE2
22 Q̄0
21 Q̄1
20 Q̄2
19 Q̄3
18 Q̄4
17 Q̄5
16 Q̄6
15 Q̄7
14 CE
13 CP
TOP VIEW

LOGIC SYMBOL

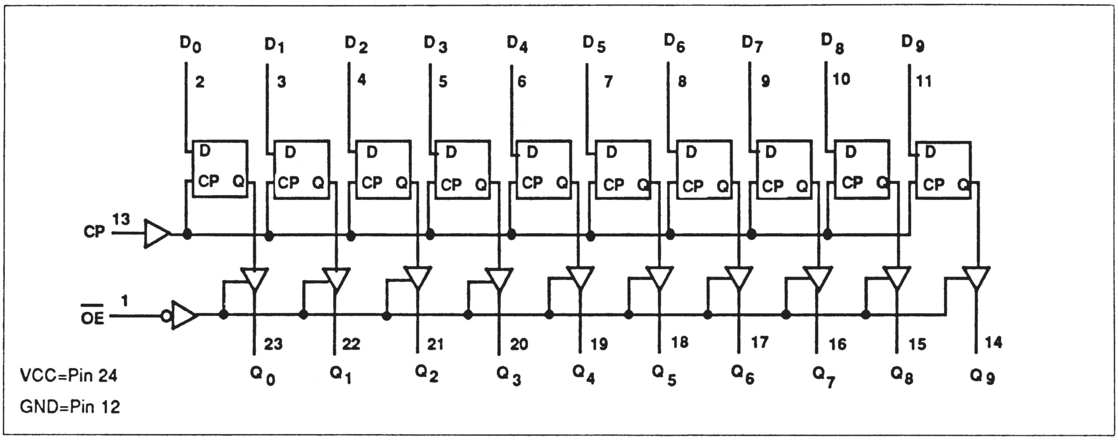

'F826
3 4 5 6 7 8 9 10
D0 D1 D2 D3 D4 D5 D6 D7
13 CP
14 CE
11 MR
1 OE0
2 OE1
23 OE2
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
22 21 20 19 18 17 16 15

V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

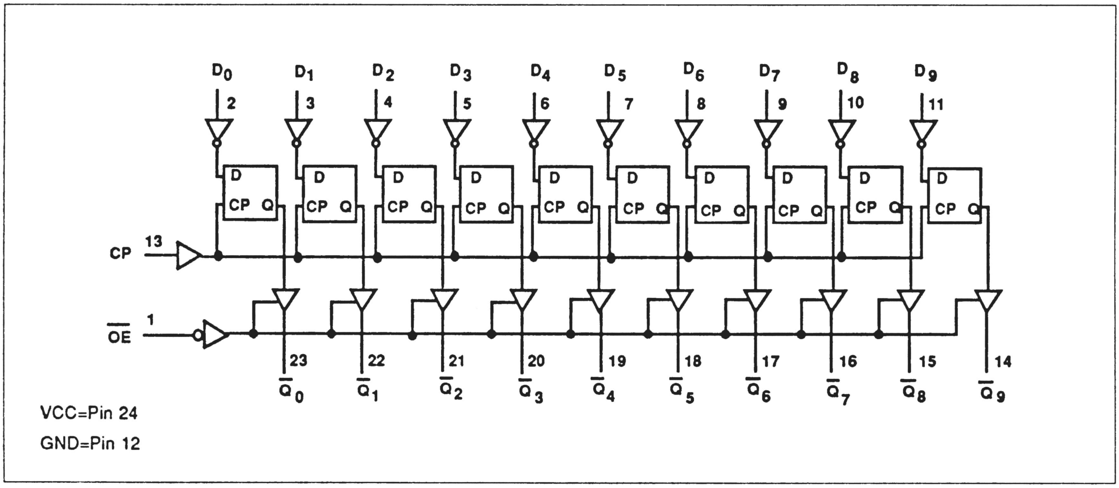

'F826
1
2
23
&
EN
11 R
14 G1
13 1C2
3 2D
22
4 21
5 20
6 19
7 18
8 17
9 16
10 15

LOGIC DIAGRAM for 'F821


D0 D1 D2 D3 D4 D5 D6 D7 D8 D9
2 3 4 5 6 7 8 9 10 11
D
CP Q
CP
13
$\overline{OE}$
1
23 22 21 20 19 18 17 16 15 14
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9

VCC=Pin 24
GND=Pin 12

LOGIC DIAGRAM for 'F822


D0 D1 D2 D3 D4 D5 D6 D7 D8 D9
2 3 4 5 6 7 8 9 10 11
D
CP Q
CP
13
$\overline{OE}$
1
23 22 21 20 19 18 17 16 15 14
$\overline{Q}_0$ $\overline{Q}_1$ $\overline{Q}_2$ $\overline{Q}_3$ $\overline{Q}_4$ $\overline{Q}_5$ $\overline{Q}_6$ $\overline{Q}_7$ $\overline{Q}_8$ $\overline{Q}_9$

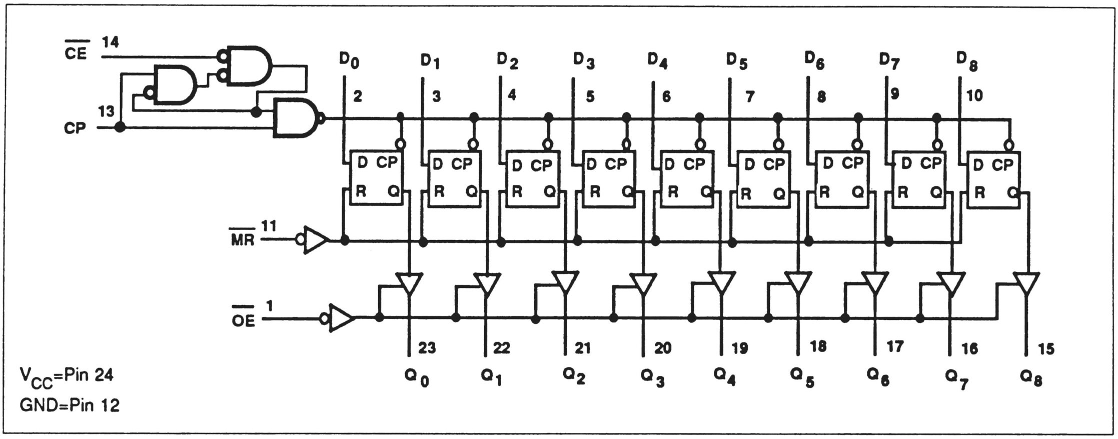
VCC=Pin 24
GND=Pin 12

FUNCTION TABLE for 'F821 and 'F822

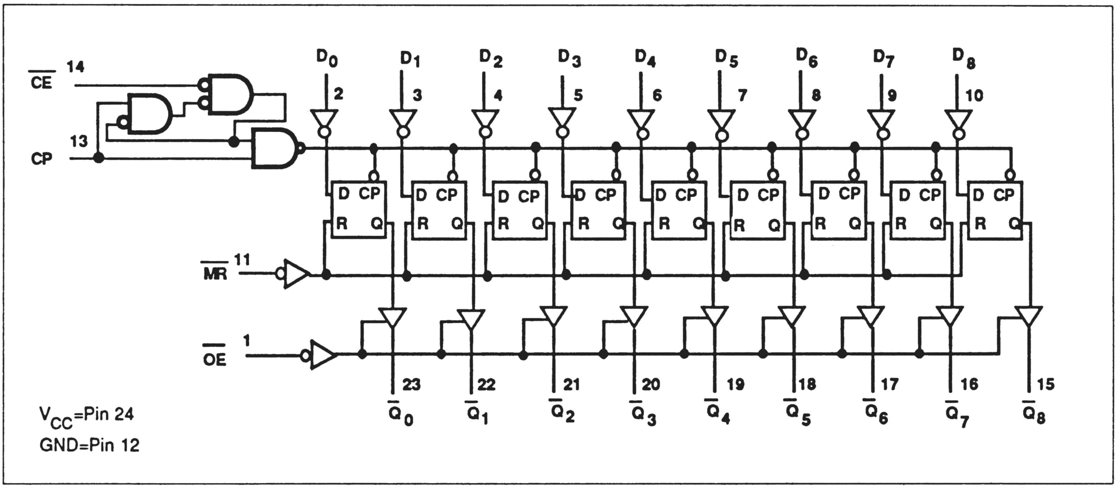
INPUTS			OUTPUTS		OPERATING MODE
			'F821	'F822	
$\overline{OE}$	CP	D_n	Q	$\overline{Q}$	
L	↑	l	L	H	Transparent
L	↑	h	H	L	
L	‡	X	NC	NC	Hold
H	X	X	Z	Z	High impedance

H = High voltage level
L = Low voltage level
h = High state must be present one setup time before the Low-to-High clock transition
l =Low state must be present one setup time before the Low-to -High clock transition
↑ =Low-to-High clock transition
‡ = Not a Low-to-High clock transition
X =Don't care
NC =No change
Z =High impedance "off" state

LOGIC DIAGRAM for 'F823


CE 14
CP 13
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
D8 10
D CP
R Q
MR 11
OE 1
23 Q0
22 Q1
21 Q2
20 Q3
19 Q4
18 Q5
17 Q6
16 Q7
15 Q8
VCC=Pin 24
GND=Pin 12

LOGIC DIAGRAM for 'F824

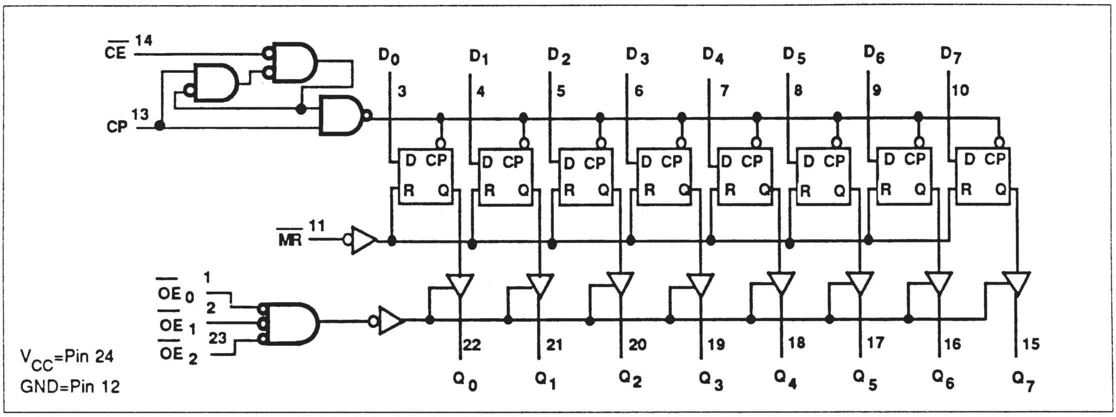

CE 14
CP 13
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
D8 10
D CP
R Q
MR 11
OE 1
23 Q̄0
22 Q̄1
21 Q̄2
20 Q̄3
19 Q̄4
18 Q̄5
17 Q̄6
16 Q̄7
15 Q̄8
VCC=Pin 24
GND=Pin 12

FUNCTION TABLE for 'F823 and 'F824

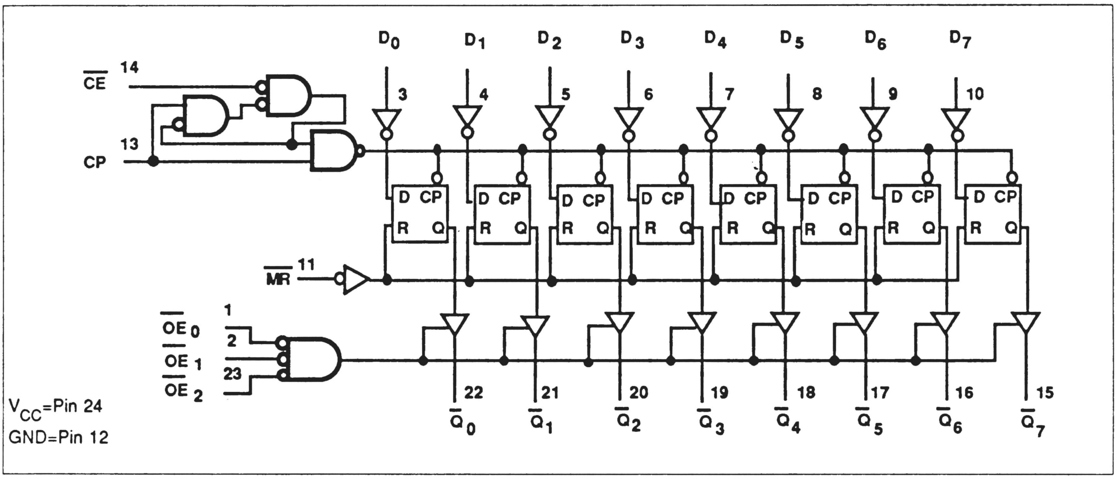
INPUTS					OUTPUTS		OPERATING MODE
					'F823	'F824	
$\overline{OE}$	$\overline{MR}$	$\overline{CE}$	CP	D_n	Q	$\overline{Q}$	
L	L	X	X	X	L	L	Clear
L	H	L	↑	h	H	L	Transparent
L	H	L	↑	l	L	H	
L	H	H	↑̸	X	NC	NC	Hold
H	X	X	X	X	Z	Z	High impedance

H = High voltage level
L = Low voltage level
h = High state must be present one setup time before the Low-to-High clock transition
l =Low state must be present one setup time before the Low-to -High clock transition
↑ =Low-to-High clock transition
↑̸ =Not a Low-to-High clock transition
X =Don't care
NC =No change
Z =High impedance "off" state

LOGIC DIAGRAM for 'F825


$\overline{CE}$ 14
CP 13
D_0 3
D_1 4
D_2 5
D_3 6
D_4 7
D_5 8
D_6 9
D_7 10
D CP
R Q
$\overline{MR}$ 11
$\overline{OE}_0$ 1
$\overline{OE}_1$ 2
$\overline{OE}_2$ 23
V_{CC}=Pin 24
GND=Pin 12
22 Q_0
21 Q_1
20 Q_2
19 Q_3
18 Q_4
17 Q_5
16 Q_6
15 Q_7

LOGIC DIAGRAM for 'F826


$\overline{CE}$ 14
CP 13
D_0 3
D_1 4
D_2 5
D_3 6
D_4 7
D_5 8
D_6 9
D_7 10
D CP
R Q
$\overline{MR}$ 11
$\overline{OE}_0$ 1
$\overline{OE}_1$ 2
$\overline{OE}_2$ 23
V_{CC}=Pin 24
GND=Pin 12
22 $\overline{Q}_0$
21 $\overline{Q}_1$
20 $\overline{Q}_2$
19 $\overline{Q}_3$
18 $\overline{Q}_4$
17 $\overline{Q}_5$
16 $\overline{Q}_6$
15 $\overline{Q}_7$

FUNCTION TABLE for 'F825 and 'F826

INPUTS					OUTPUTS		OPERATING MODE
					'F825	'F826	
$\overline{OE}_n$	$\overline{MR}$	$\overline{CE}$	CP	D_n	Q	$\overline{Q}$	
L	L	X	X	X	L	L	Clear
L	H	L	↑	h	H	L	Transparent
L	H	L	↑	l	L	H	
L	H	H	‡	X	NC	NC	Hold
H	X	X	X	X	Z	Z	High impedance

H = High voltage level
L = Low voltage level
h = High state must be present one setup time before the Low-to-High clock transition
l = Low state must be present one setup time before the Low-to -High clock transition
↑ = Low-to-High clock transition
‡ = Not a Low-to-High clock transition
X = Don't care
NC = No change
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-24	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} =-15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
				V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} =-24mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
					I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-20	μA
I_{OZH}	Off-state output current, High voltage applied			V_{CC} = MAX, V_O = 2.7V					50	μA
I_{OZL}	Off-state output current, Low voltage applied			V_{CC} = MAX, V_O = 0.5V					-50	μA
I_{OS}	Short circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F821 'F822	I_{CCH}	V_{CC} = MAX				75	105	mA
			I_{CCL}					75	105	mA
			I_{CCZ}					75	115	mA
		'F823 'F824	I_{CCH}	V_{CC} = MAX				65	100	mA
			I_{CCL}					70	105	mA
			I_{CCZ}					75	110	mA
		'F825 'F826	I_{CCH}	V_{CC} = MAX				60	85	mA
			I_{CCL}					60	90	mA
			I_{CCZ}					65	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

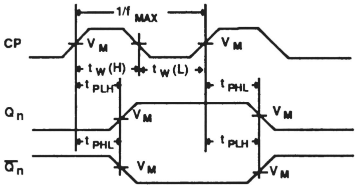
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	150	180		140		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	'F821 'F823 'F825 'F826	Waveform 1	4.0 4.0	6.5 6.0	8.5 8.5	4.0 3.5	9.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_n$	'F822 'F824	Waveform 1	4.5 4.5	6.5 6.5	9.0 9.0	4.5 4.5	10.0 9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n or $\overline{Q}_n$	'F823 'F824 'F825 'F826	Waveform 2	3.0	5.0	8.0	3.0	8.0	ns
t_{PZH} t_{PZL}	Output Enable time OE_n to Q_n or $\overline{Q}_n$		Waveform 4 Waveform 5	5.0 3.0	7.0 5.0	10.0 8.0	4.0 2.5	11.5 9.0	ns
t_{PHZ} t_{PLZ}	Propagation delay OE_n to Q_n or $\overline{Q}_n$		Waveform 4 Waveform 5	1.5 1.5	3.5 3.5	6.5 6.5	1.5 1.5	7.5 7.5	ns

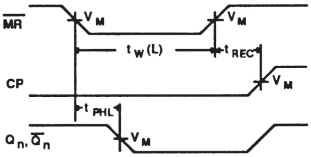
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	'F821 'F822	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	'F823 'F824 'F825 'F826	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP		Waveform 3	2.0 2.0			2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 1	3.5 3.5			4.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CE}$ to CP	'F823 'F824 'F825 'F826	Waveform 3	0.0 2.0			0.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP		Waveform 3	0.0 2.5			0.0 3.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low		Waveform 2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP		Waveform 2	2.5			2.5		ns

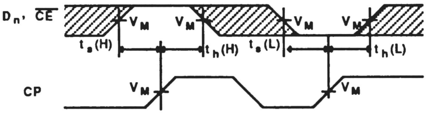
AC WAVEFORMS


1/f MAX
CP
V M
t w (H)
t w (L)
t PLH
t PHL
Q n
Q̄ n
t PHL
t PLH

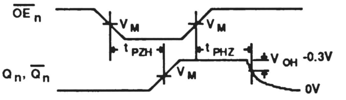
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency


M̄R̄
V M
t w (L)
t REC
CP
t PHL
Q n, Q̄ n

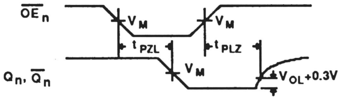
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time


D n, C̄Ē
V M
t s (H)
t h (H)
t s (L)
t h (L)
CP

Waveform 3. Data Setup And Hold Times


ŌĒ n
V M
t PZH
t PHZ
V OH -0.3V
0V
Q n, Q̄ n

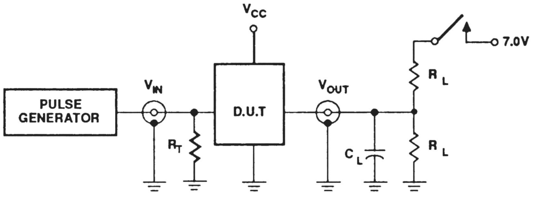
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level


ŌĒ n
V M
t PZL
t PLZ
V OL +0.3V
Q n, Q̄ n

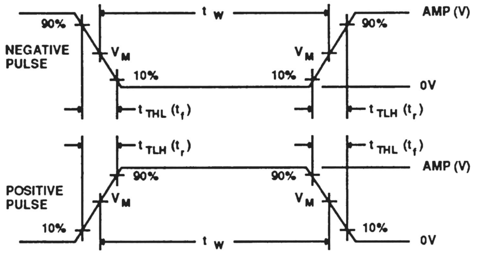
Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V CC
7.0V
PULSE GENERATOR
V IN
R T
D.U.T
V OUT
C L
R L
R L

Test Circuit For 3-State Outputs


t w
AMP (V)
90%
NEGATIVE PULSE
V M
10%
0V
t THL (t f)
t TLH (t r)
POSITIVE PULSE
90%
10%
AMP (V)
0V
t w

$V_M = 1.5V$
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F832, 74F1832

OR Drivers

74F832-Hex Two-Input OR Driver
74F1832-Hex Two-Input OR Driver
PreliminarySpecification

FEATURES

- **High capacitive drive capability**
- **Choice of configuration**
  Corner V_{CC} and GND-- 'F832
  Center V_{CC} and GND-- 'F1832
- **Typical propagation delay of 2.6ns**

TYPE	TYPICAL PRPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F832	2.6ns	11mA
74F1832	2.6ns	11mA

ORDERING INFORMATION

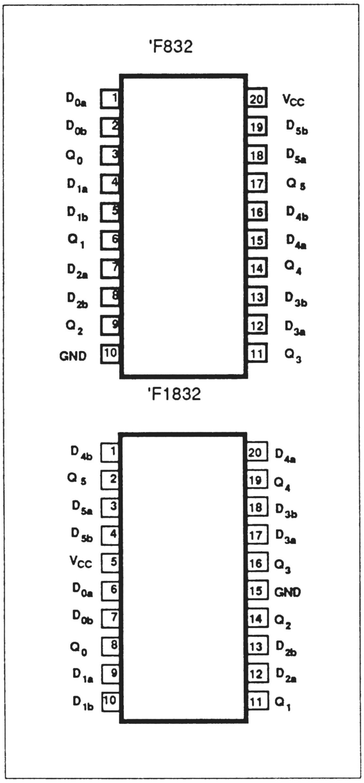
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F832N, N74F1832N
20-Pin Plastic SOL	N74F832D, N74F1832D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

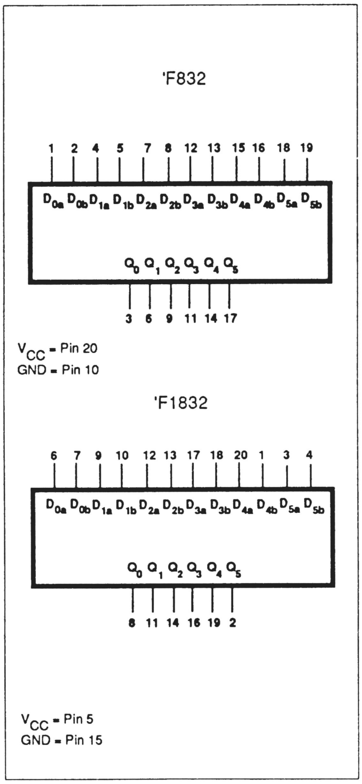
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na} - D_{nb}	Data inputs	1.0/0.033	20μA/20μA
Q_0 - Q_5	Data outputs	2400/80	48mA/48mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION


'F832
D0a 1
D0b 2
Q0 3
D1a 4
D1b 5
Q1 6
D2a 7
D2b 8
Q2 9
GND 10
20 Vcc
19 D5b
18 D5a
17 Q5
16 D4b
15 D4a
14 Q4
13 D3b
12 D3a
11 Q3
'F1832
D4b 1
Q5 2
D5a 3
D5b 4
Vcc 5
D0a 6
D0b 7
Q0 8
D1a 9
D1b 10
20 D4a
19 Q4
18 D3b
17 D3a
16 Q3
15 GND
14 Q2
13 D2b
12 D2a
11 Q1

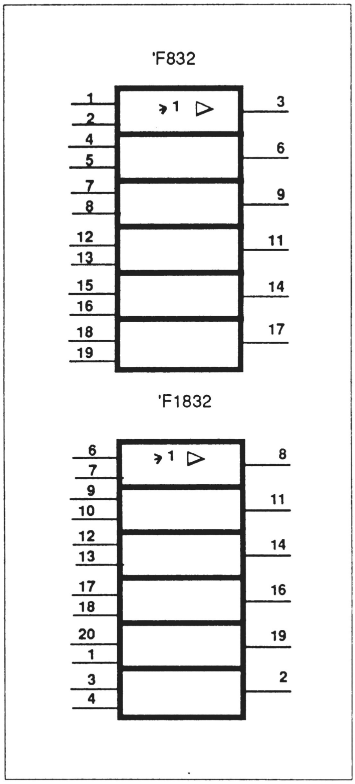
LOGIC SYMBOL


'F832
1 2 4 5 7 8 12 13 15 16 18 19
D0a D0b D1a D1b D2a D2b D3a D3b D4a D4b D5a D5b
Q0 Q1 Q2 Q3 Q4 Q5
3 6 9 11 14 17
'F1832
6 7 9 10 12 13 17 18 20 1 3 4
D0a D0b D1a D1b D2a D2b D3a D3b D4a D4b D5a D5b
Q0 Q1 Q2 Q3 Q4 Q5
8 11 14 16 19 2

V_{CC} = Pin 20
GND = Pin 10

V_{CC} = Pin 5
GND = Pin 15

LOGIC SYMBOL(IEEE/IEC)


'F832
≥1
1
2
3
4
5
6
7
8
9
12
13
11
15
16
14
18
19
17
'F1832
≥1
6
7
8
9
10
11
12
13
14
17
18
16
20
1
19
3
4
2

FUNCTION TABLE

INPUTS		OUTPUT
D_{na}	D_{nb}	Q_n
H	X	H
X	H	H
L	L	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	96	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-48	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.0			V
				±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.38	0.55	V
				±5%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input clamp current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-20	µA
I_O	Output current[3]		V_{CC} = MAX, V_O=2.25V		-60		-160	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} =GND		9	15	mA
		I_{CCL}		V_{IN} =4.5V		22	36	mA

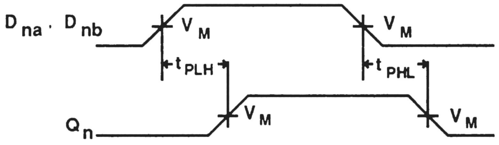
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to Q_n	Waveform 1	1.0 1.0	2.5 2.4	4.5 4.5	1.0 1.0	5.5 5.5	ns

AC WAVEFORMS

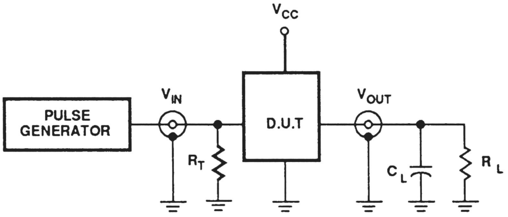

D_{na}, D_{nb}
V_M
V_M
t_{PLH}
t_{PHL}
Q_n
V_M
V_M

Waveform 1.

Propagation Delay for Input to Output

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
R_T
D.U.T
V_{OUT}
C_L
R_L

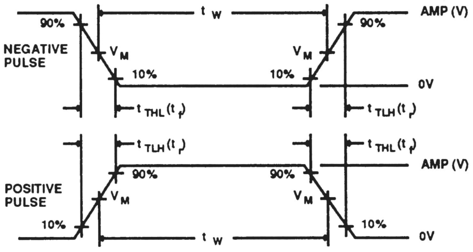
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


NEGATIVE PULSE
90%
V_M
10%
t_W
V_M
10%
90%
AMP (V)
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
POSITIVE PULSE
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
90%
90%
AMP (V)
V_M
V_M
10%
10%
t_W
0V

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F835

Shift Register

8-Bit Shift Register with 2:1 Mux-in, Latched "B" inputs, and Serial Out

Product Specification

FEATURES

- Combines the 'F373, two 'F157s, and the 'F166 functions in one package
- Interleaved loading with 2:1 mux
- Dual 8-bit Parallel inputs
- Transparent Latch on all "B" inputs
- Guaranteed Serial Shift Frequency to 60MHz
- Expandable to 16-bits or more with serial input

DESCRIPTION

The 74F835 is a high speed 8-bit parallel/ serial-in, serial-out shift register whose parallel inputs have been connected to an internal octal two-to-one multiplexer with all the 'B' inputs connected to an octal latch.

It is useful in any design where a 2:1 mux input with a transparent latch is needed.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F835	85MHz	45mA

ORDERING INFORMATION

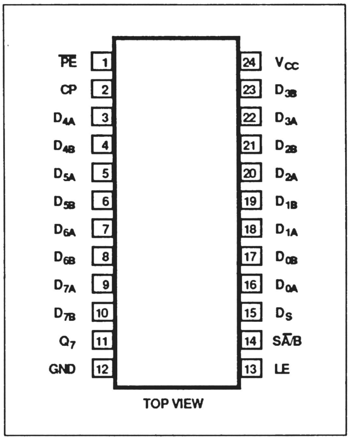
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
24-Pin Plastic Slim DIP (300 mil)	N74F835N
24-Pin Plastic SOL	N74F835D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

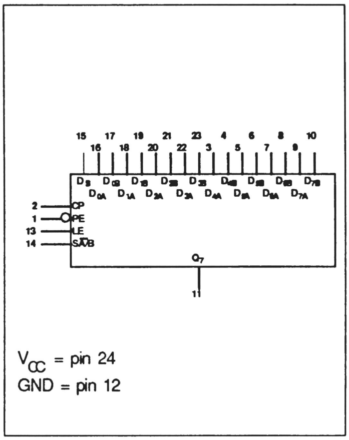
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{0A} - D_{7A}	Parallel data inputs	1.0/1.0	20µA/0.6mA
D_{0B} - D_{7B}	Latched Parallel data inputs	1.0/1.0	20µA/0.6mA
D_S	Serial data input	1.0/1.0	20µA/0.6mA
CP	Shift Register Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$S\bar{A}/B$	Mux Select	1.0/1.0	20µA/0.6mA
LE	Latch Enable input (for B inputs)	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input	1.0/1.0	20µA/0.6mA
Q_7	Output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

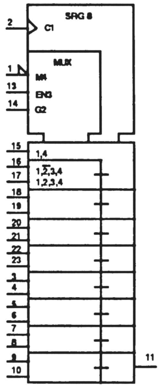

$\overline{PE}$ 1
CP 2
D_{4A} 3
D_{4B} 4
D_{5A} 5
D_{5B} 6
D_{6A} 7
D_{6B} 8
D_{7A} 9
D_{7B} 10
Q_7 11
GND 12
24 V_{CC}
23 D_{3B}
22 D_{3A}
21 D_{2B}
20 D_{2A}
19 D_{1B}
18 D_{1A}
17 D_{0B}
16 D_{0A}
15 D_S
14 $S\bar{A}/B$
13 LE
TOP VIEW

LOGIC SYMBOL


15 17 19 21 23 4 6 8 10
16 18 20 22 3 5 7 9
D_S D_{0B} D_{1B} D_{2B} D_{3B} D_{4B} D_{5B} D_{6B} D_{7B}
D_{0A} D_{1A} D_{2A} D_{3A} D_{4A} D_{5A} D_{6A} D_{7A}
2 CP
1 PE
13 LE
14 $S\bar{A}/B$
Q_7
11

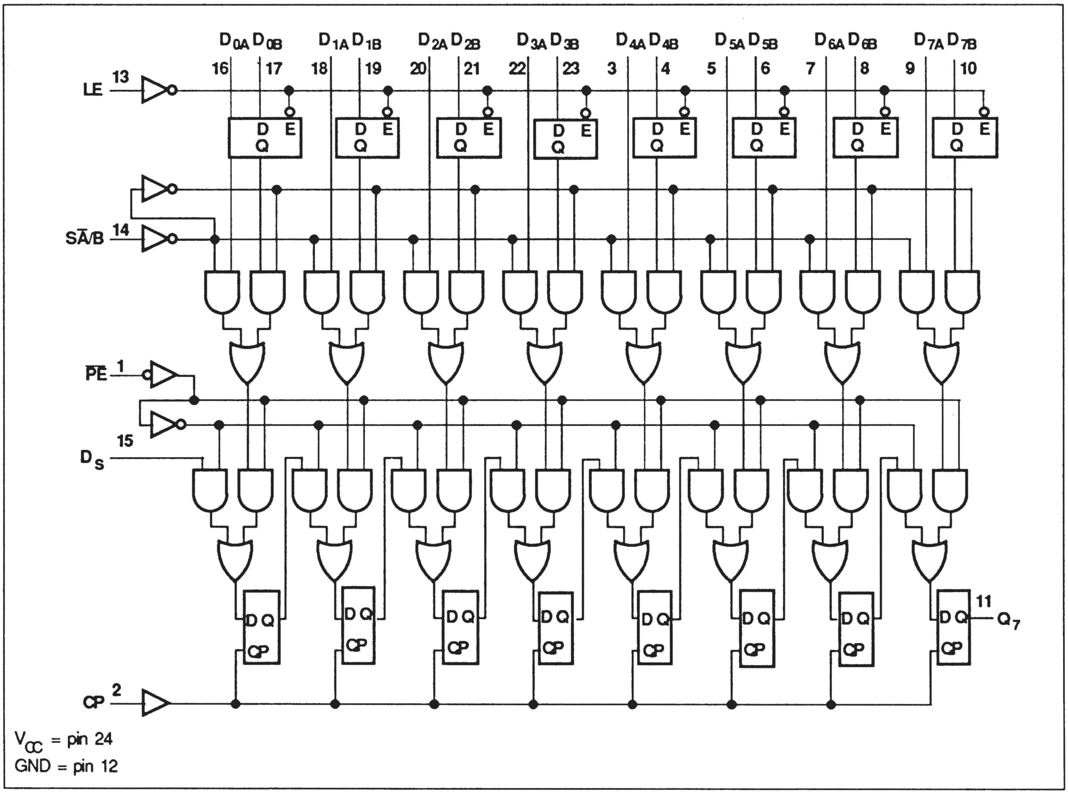
V_{CC} = pin 24
GND = pin 12

LOGIC SYMBOL(IEEE/IEC)


SRG 8
2 C1
MUX
1 M4
13 EN3
14 G2
15 1,4
16 1,Σ,3,4
17 1,2,3,4
18
19
20
21
22
23
3
4
5
6
7
8
9
10
11

June 14, 1988

LOGIC DIAGRAM


D0A D0B
D1A D1B
D2A D2B
D3A D3B
D4A D4B
D5A D5B
D6A D6B
D7A D7B
16 17 18 19 20 21 22 23 3 4 5 6 7 8 9 10
LE 13
SĀ/B 14
P̄Ē 1
DS 15
CP 2
D E Q
D Q CP
11 Q7

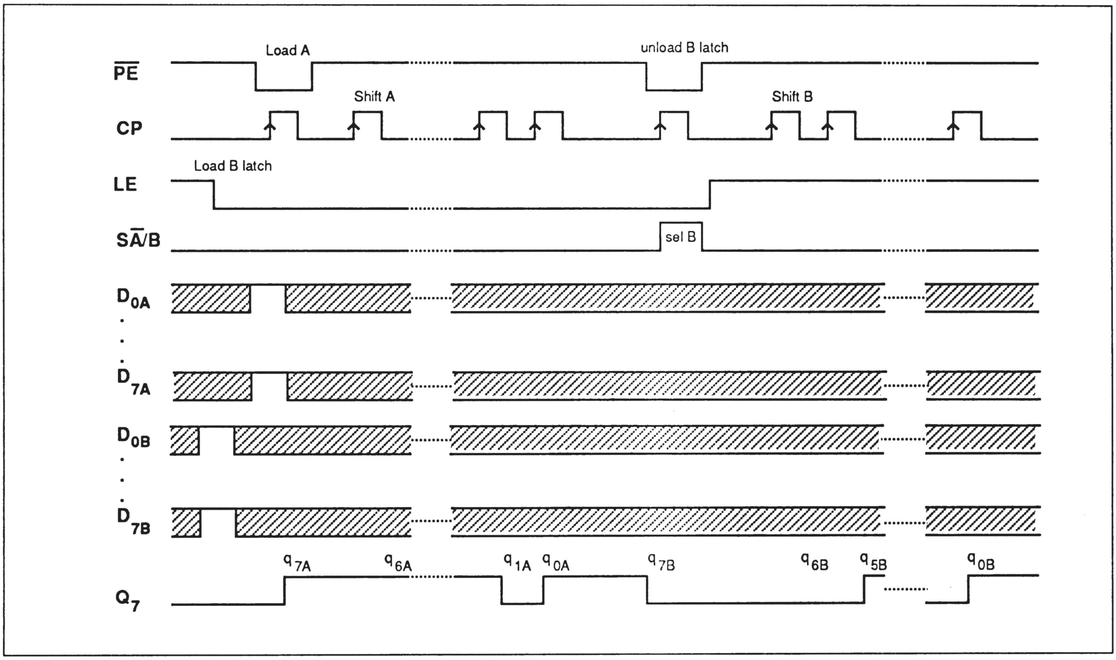
V_{CC} = pin 24
GND = pin 12

FUNCTION TABLE

OPERATING MODE	INPUTS							INTERNAL			OUTPUT
	$\overline{PE}$	CP	LE	$S\overline{A}/B$	D_{nA}	D_{nB}	D_S	B Latch	Serial Reg Q_8	Serial Reg Q_{1-6}	Q_7
Parallel load A data	L	↑	X	L	h	X	X	X	H	H	H
					l	X	X	X	L	L	L
Latch B data	X	X	L	X	X	h	X	H	X	X	X
					X	l	X	L	X	X	X
Parallel load B data (from Latch)	L	↑	L	H	X	X	X	h	H	H	H
					X	X	X	l	L	L	L
Parallel load B data (Transparent Mode)	L	↑	H	H	X	h	X	h	H	H	H
					X	l	X	l	L	L	L
Serial Shift	H	↑	X	X	X	X	h	X	H	q_{n-1}	q_6
					X	X	l	X	L	q_{n-1}	q_6

H = High voltage level
L = Low voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
q_n = Lower case letters indicate the state of the referenced flop cell one cycle prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

TYPICAL TIMING DIAGRAM


$\overline{PE}$
Load A
unload B latch
CP
Shift A
Shift B
LE
Load B latch
$S\overline{A}/B$
sel B
D_{0A}
D_{7A}
D_{0B}
D_{7B}
Q_7
q_{7A}
q_{6A}
q_{1A}
q_{0A}
q_{7B}
q_{6B}
q_{5B}
q_{0B}

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		.30	.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		.30	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX			45	65	mA
	I_{CCL}				45	65	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

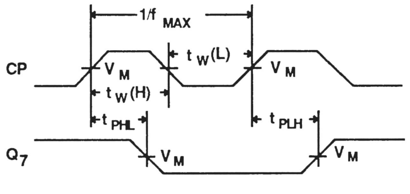
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	70	85		60		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_7 (Load)	Waveform 1	7.0 7.0	9.0 9.0	11.5 11.5	6.5 6.5	12.5 12.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_7 (Shift)	Waveform 1	7.0 7.0	9.0 9.0	11.5 11.5	6.5 6.5	12.5 12.5	ns

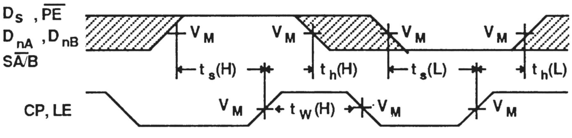
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time D_{nA} or D_{nB} to CP	Waveform 2	2.0 2.0			2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time D_{nA} or D_{nB} to CP	Waveform 2	2.5 2.5			3.0 3.0		ns
$t_s(H)$ $t_s(L)$	Setup time D_S to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_S to CP	Waveform 2	3.5 3.5			4.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time $\overline{PE}$ to CP	Waveform 2	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time $\overline{PE}$ to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_s(H)$ $t_s(L)$	Setup time D_{nB} to LE	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_{nB} to LE	Waveform 2	3.0 3.0			3.5 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time $S\overline{A}/B$ to CP	Waveform 2	3.5 3.5			4.5 4.5		ns
$t_h(H)$ $t_h(L)$	Hold time $S\overline{A}/B$ to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width, High or Low	Waveform 1	6.0 5.0			6.5 5.0		ns
$t_w(H)$	Latch Enable pulse width, High	Waveform 2	4.5			5.0		ns

AC WAVEFORMS



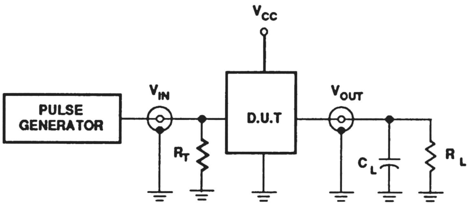
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data and Select Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_CC
PULSE GENERATOR
V_IN
R_T
D.U.T
V_OUT
C_L
R_L

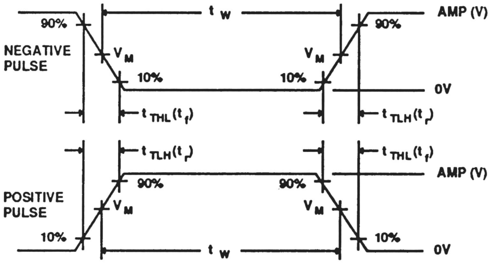
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


NEGATIVE PULSE
90%
V_M
10%
t_W
AMP (V)
0V
t_THL (t_f)
t_TLH (t_r)
POSITIVE PULSE
t_TLH (t_r)
t_THL (t_f)
90%
V_M
10%
t_W
AMP (V)
0V

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F838

Microprogram Sequence Controller

Preliminary Specification

FEATURES

- **5-bit address generator (32 micro-instruction addressability)**
- **Two subroutine branching capability**
- **Interrupt branching**
- **Cascadable for increased addressing**
- **Direct branching over full address range**

DESCRIPTION

The Signetics 74F838 Microprogram Sequence Controller generates addresses to access instructions from a microprogram memory.

This high-speed device provides an efficient means of controlling the flow through a microprogram by providing a powerful set of sequencing functions.

In addition to providing branching facility over the entire address range, the device also supports two subroutines and an interrupt level.

The 74F838 can directly address up to 32 micro-instructions. However, two or more devices may be cascaded for increased addressing. For example, two devices can address 1K and three can address up to 32K of program storage.

Combined with memory, the 74F838 forms a powerful control section for CPUs and I/O controllers.

The device is available in a 20-pin DIP and SOL Packages.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F838	90MHz	65mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F838N
20-Pin Plastic SOL	N74F838D

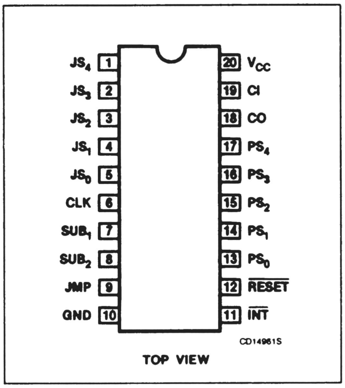
INPUT AND OUTPUT LOADING AND FANOUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$JS_0 - JS_4$	Jump State input	1.0/1.0	20μA/0.6mA
SUB_1, SUB_2	Subroutine input	1.0/1.0	20μA/0.6mA
JMP	Jump input	1.0/2.0	20μA/0.6mA
$\overline{INT}$	Interrupt input (active-Low)	1.0/1.0	20μA/0.6mA
CLK	Clock input	1.0/1.0	20μA/0.6mA
$\overline{RESET}$	Reset input (active-Low)	1.0/1.0	20μA/0.6mA
CI	Cascade In input	1.0/1.0	20μA/0.6mA
CO	Cascade Out output	150/40	3mA/24mA
$PS_0 - PS_4$	Present State output	150/40	3mA/24mA

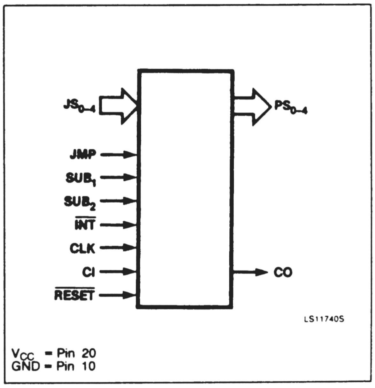
NOTE:

1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6 mA in the Low state.

PIN CONFIGURATION


JS_4 1
JS_3 2
JS_2 3
JS_1 4
JS_0 5
CLK 6
SUB_1 7
SUB_2 8
JMP 9
GND 10
20 V_{CC}
19 CI
18 CO
17 PS_4
16 PS_3
15 PS_2
14 PS_1
13 PS_0
12 $\overline{RESET}$
11 $\overline{INT}$
CD14961S
TOP VIEW

LOGIC SYMBOL


JS_{0-4}
PS_{0-4}
JMP
SUB_1
SUB_2
$\overline{INT}$
CLK
CI
$\overline{RESET}$
CO
LS11740S
V_{CC} = Pin 20
GND = Pin 10

PIN DESCRIPTION

SYMBOL	PIN	TYPE	NAME	FUNCTION
JS_0 JS_1 JS_2 JS_3 JS_4	5 4 3 2 1	Input Input Input Input Input	Jump State	Address on these inputs is transferred to the $PS_0 - PS_4$ outputs if the JMP input is High or the SUB_1 or SUB_2 inputs change from Low-to-High. These inputs are ignored if neither of the above conditions is true.
SUB_1 SUB_2	7 8	Input Input	Subroutine	On a Low-to-High transition, the Present State address ($PS_0 - PS_4$) plus one is saved internally as a return address, and the address on pins $JS_0 - JS_4$ will be transferred to the $PS_0 - PS_4$ outputs. On a High-to-Low transition, the saved return address will be enabled onto the $PS_0 - PS_4$ outputs.
JMP	9	Input	Jump	When JMP is High, the next state address will be $JS_0 - JS_4$.
$\overline{INT}$	11	Input	Interrupt	On a High-to-Low transition, the next address to appear on the $PS_0 - PS_4$ output is saved internally as a return address and $PS_0 - PS_4$ are forced to all ones. If this feature is used, a microcode jump would normally be stored at state address 11111. SUB_1 and SUB_2 inputs are ignored when $\overline{INT}$ is Low. On a Low-to-High transition, the saved return address is enabled onto the $PS_0 - PS_4$ outputs.
CLK	6	Input	Clock	This clock determines the sequence rate of the controller.
$\overline{RESET}$	12	Input	Reset	When Low, all internal registers and $PS_0 - PS_4$ outputs are set to zeros.
CI	19	Input	Cascade In	This input should be tied to V_{CC} for the least significant device. For all other devices, CI is connected to CO of the previous device.
CO	18	Output	Cascade Out	This signal is connected to CI of the next device. One device permits 32 states, two devices allow 1024 states, three devices allow 32,768 states, and so forth.
PS_0 PS_1 PS_2 PS_3 PS_4	13 14 15 16 17	Output	Present State	Present State address outputs.

FUNCTIONAL OPERATION

As shown in the block diagram, the address appearing on the $PS_0 - PS_4$ outputs is selected from five different sources:

- Incremented address
- SUB_1 return address
- SUB_2 return address
- Interrupt return address
- $JS_0 - JS_4$ inputs

The selection of a specific source of address (as explained in the Function Table) is determined by the state of SUB_1, SUB_2, JMP and $\overline{INT}$ inputs. When Low, the $\overline{RESET}$ input unconditionally forces all registers and the $PS_0 - PS_4$ outputs to all zeros. The "increment" function increments the Present State ($PS_0 - PS_4$) by one on the rising edge of the CLK input and automatically wraps around from the highest address (all 1's) to the lowest address (all 0's).

Subroutine Calls

Two subroutine calls, SUB_1 and SUB_2, are supported by the F838. On a Low-to-High transition of SUB_1, $PS_0 - PS_4$ address plus one is stored in the SRA_1 register as a return address and $JS_0 - JS_4$ inputs are transferred to the $PS_0 - PS_4$ outputs on the rising edge of CLK. Similarly, $PS_0 - PS_4$ plus one is stored in the SRA_2 register when SUB_2 makes a Low-to-High transition and $JS_0 - JS_4$ inputs are enabled onto the $PS_0 - PS_4$ outputs on the rising edge of CLK. The rising CLK edge, after the High-to-Low transition on the SUB_1 or SUB_2 inputs, enables the stored return address onto the $PS_0 - PS_4$ outputs. (Please refer to the Function Table for illegal conditions.)

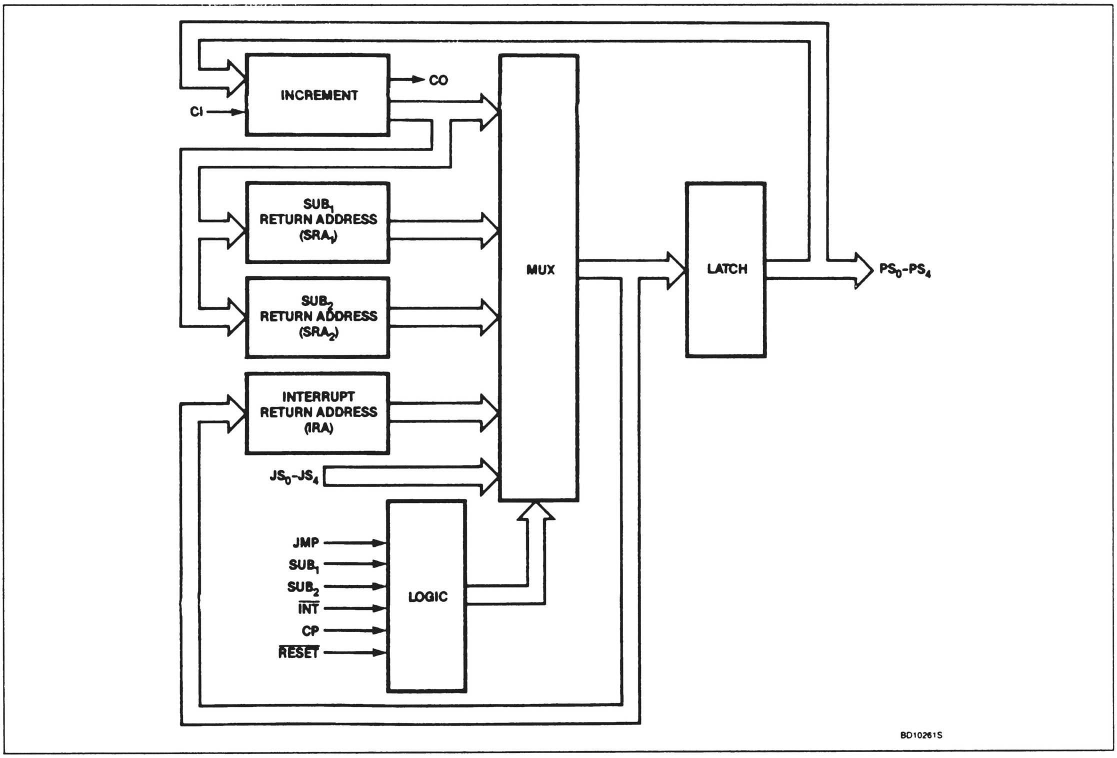
Jump

When this input is High, $PS_0 - PS_4$ outputs are forced to the address indicated by the $JS_0 - JS_4$ inputs. This occurs on the first rising CLK edge after the JMP input has gone High.

Interrupt

The rising CLK edge following a High-to-Low transition on this input will store the next address to appear on the $PS_0 - PS_4$ outputs in the IRA register and force $PS_0 - PS_4$ outputs to all ones (1's). The saved return address is output on the $PS_0 - PS_4$ outputs on the rising CLK edge following a Low-to-High transition on the $\overline{INT}$ input.

BLOCK DIAGRAM


INCREMENT
CO
CI
SUB_1 RETURN ADDRESS (SRA_1)
SUB_2 RETURN ADDRESS (SRA_2)
INTERRUPT RETURN ADDRESS (IRA)
JS_0-JS_4
MUX
LATCH
PS_0-PS_4
JMP
SUB_1
SUB_2
$\overline{INT}$
CP
$\overline{RESET}$
LOGIC
BD10261S

FUNCTION TABLE

INPUTS							OUTPUTS				FUNCTION
$\overline{RESET}$	$\overline{INT}$	JMP	SB_1	SB_2	CP	JS_n	$PS_0 - PS_4$	SRA_1	SRA_2	IRA	
L	X	X	X	X	X	X	00000	0	0	0	RESET
H	H	L	H or L	H or L	↑	X	PS_{n+1}				INCREMENT
H	L	L	X	X	↑	X	PS_{n+1}				
H	L	H	X	X	↑	JS_n	JS_n				JUMP
H	H	H	$\not\downarrow$	$\not\downarrow$	↑	JS_n	JS_n				
H	H	X	↑	H or L	↑	JS_n	JS_n	PS_{n+1}			SUBROUTINE CALL
H	H	X	H or L	↑	↑	JS_n	JS_n		PS_{n+1}		
H	H	X	↑	↑	↑	JS_n	JS_n	PS_{n+1}	PS_{n+1}		
H	H	L	↓	H or L	↑	X	SRA_1				RETURN FROM SUBROUTINE
H	H	L	H or L	↓	↑	X	SRA_2				
H	↓	L	H or L	H or L	↑	X	11111			PS_{n+1}	INTERRUPT CALL
H	↓	H	H or L	H or L	↑	JS_n	11111			JS_n	
H	↓	X	↑	H or L	↑	JS_n	11111	PS_{n+1}		JS_n	
H	↓	X	H or L	↑	↑	JS_n	11111		PS_{n+1}	JS_n	
H	↓	X	↑	↑	↑	JS_n	11111	PS_{n+1}	PS_{n+1}	JS_n	
H	↓	L	↓	H or L	↑	X	11111			SRA_1	
H	↓	L	H or L	↓	↑	X	11111			SRA_2	
H	↑	X	X	X	↑	X	IRA				RETURN FROM INTERRUPT
H	H	H	↓	H or L	↑	JS_n	$JS_n + SRA_1$				ILLEGAL
H	H	H	H or L	↓	↑	JS_n	$JS_n + SRA_2$				
H	H	L	↓	↓	↑	X	$SRA_1 + SRA_2$				
H	H	H	↓	↓	↑	JS_n	$S_n + SRA_1 + SRA_2$				
H	↓	H	↓	H or L	↑	JS_n	11111			$JS_n + SRA_1$	
H	↓	H	H or L	↓	↑	JS_n	11111			$JS_n + SRA_2$	
H	↓	L	↓	↓	↑	X	11111			$SRA_1 + SRA_2$	
H	ϕ	H	↓	↓	↑	JS_n	11111			$JS_n + SRA_1 + SRA_2$	

L = Low voltage level
H = High voltage level
X = Don't care
↓ = High-to-Low transition
↑ = Low-to-High transition
H or L = Either High or Low
$\not\downarrow$ = Anything except a High-to-Low transition
0 = Low Output
1 = High Output

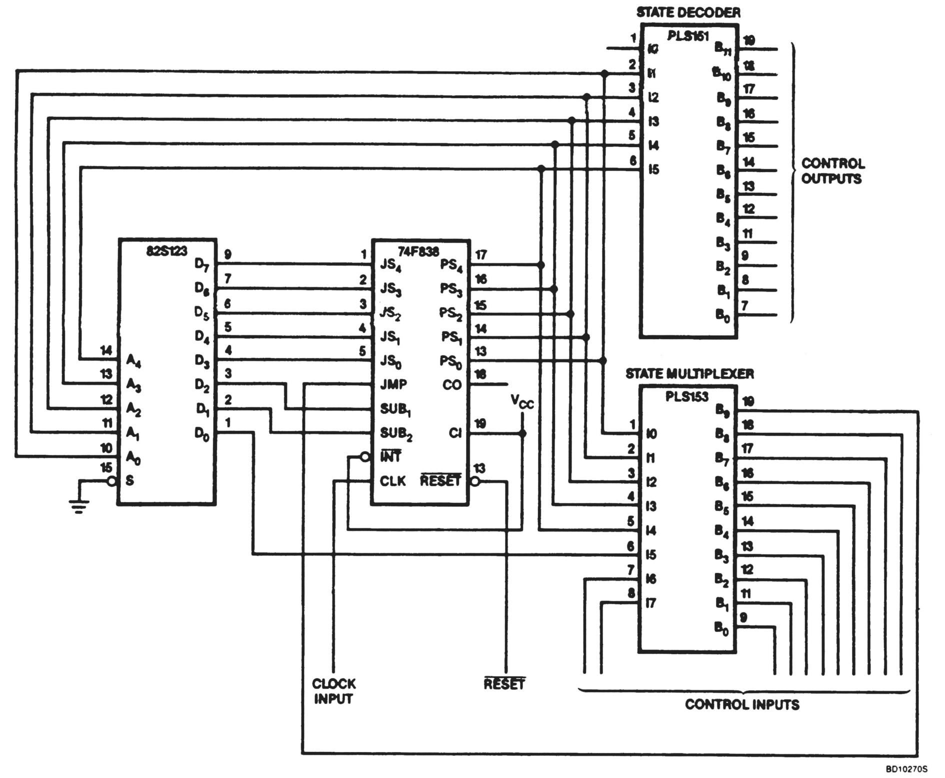

STATE DECODER
PLS151
I0
I1
I2
I3
I4
I5
B11
B10
B9
B8
B7
B6
B5
B4
B3
B2
B1
B0
CONTROL OUTPUTS
82S123
D7
D6
D5
D4
D3
D2
D1
D0
A4
A3
A2
A1
A0
S
74F838
JS4
JS3
JS2
JS1
JS0
JMP
SUB1
SUB2
INT
CLK
PS4
PS3
PS2
PS1
PS0
CO
CI
RESET
VCC
STATE MULTIPLEXER
PLS153
I0
I1
I2
I3
I4
I5
I6
I7
B9
B8
B7
B6
B5
B4
B3
B2
B1
B0
CLOCK INPUT
RESET
CONTROL INPUTS
BD10270S

Figure 1

As shown in Figure 1, a PROM (82S123) paired with the 74F838 creates a state machine. When reset, the $PS_0 - PS_4$ outputs are zero. These outputs are decoded by the PLS151 to generate control outputs. When a state has a branch option based on the state of a control signal, the $PS_0 - PS_4$ outputs are used as address inputs to a multiplexer. This application uses a PLS153 as a state multiplexer. One output of the multiplexer connects to the JMP input of the 74F838. When the proper state is decoded, the associated control input is passed on to the JMP input. In addition, the D_0 output of the PROM is connected to one of the control inputs of the multiplexer to implement an unconditional jump. All input signals to the 74F838 are sampled on the rising edge of the input clock, except the interrupt input ($\overline{INT}$) which is sampled on the falling edge of the Clock.

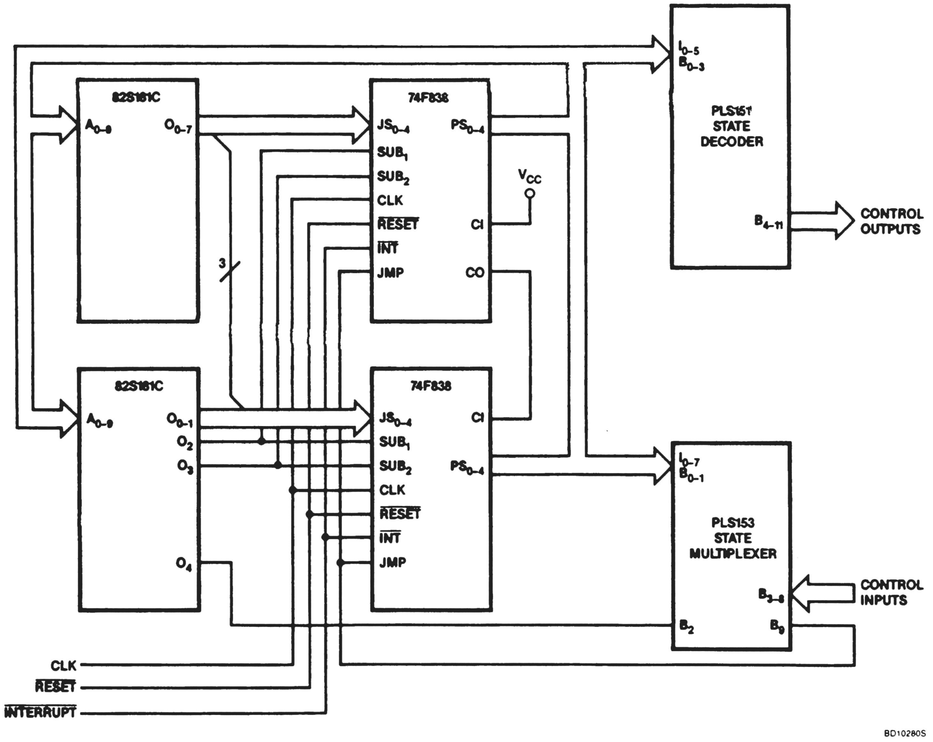

82S181C
A0-9
O0-7
74F838
JS0-4
PS0-4
SUB1
SUB2
CLK
RESET
CI
INT
JMP
CO
VCC
3
82S181C
A0-9
O0-1
O2
O3
O4
74F838
JS0-4
CI
SUB1
SUB2
PS0-4
CLK
RESET
INT
JMP
I0-5
B0-3
PLS151
STATE
DECODER
B4-11
CONTROL
OUTPUTS
I0-7
B0-1
PLS153
STATE
MULTIPLEXER
B3-8
CONTROL
INPUTS
B2
B9
CLK
RESET
INTERRUPT
BD10280S

Figure 2. Cascade Mode Interface

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	LIMITS	UNIT
V_{CC}	Supply voltage	−0.5V to +7.0	V
V_{IN}	Input voltage	−0.5V to +7.0	V
I_{IN}	Input current	−30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output current	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output current	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STD}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10% V_{CC}	2.5			V
				±5% V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10% V_{CC}		0.35	0.50	V
				±5% V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				90	mA
		I_{CCL}					90	mA

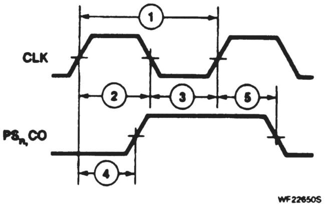
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

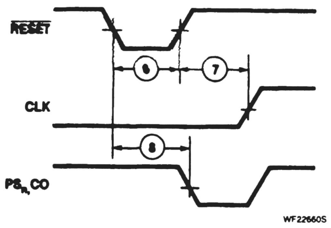
AC ELECTRICAL CHARACTERISTICS

NUMBER	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = 25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
1	Maximum clock frequency	Waveform 1	70	90		60		MHz
2	CLK High time	Waveform 1						ns
3	CLK Low time	Waveform 1						ns
4	CLK to PS_n, CO High delay	Waveform 1						ns
5	CLK to PS_n, CO Low delay	Waveform 1						ns
6	$\overline{RESET}$ Pulse Width	Waveform 2						ns
7	Recovery time $\overline{RESET}$ to CLK	Waveform 2						ns
8	$\overline{RESET}$ to PS_n, CO Low delay	Waveform 2						ns
9	CI Low setup to CLK	Waveform 3						ns
	JS_n Low setup to CLK	Waveform 3						ns
	JMP Low setup to CLK	Waveform 3						ns
	SUB_1, SUB_2 Low setup to CLK	Waveform 3						ns
10	CI Low hold after CLK	Waveform 3						ns
	JS_n Low hold after CLK	Waveform 3						ns
	JMP Low hold after CLK	Waveform 3						ns
	SUB_1, SUB_2 Low hold after CLK	Waveform 3						ns
11	CI High setup to CLK	Waveform 3						ns
	JS_n High setup to CLK	Waveform 3						ns
	JMP High setup to CLK	Waveform 3						ns
	SUB_1, SUB_2 High setup to CLK	Waveform 3						ns
12	CI High hold after CLK	Waveform 3						ns
	JS_n High hold after CLK	Waveform 3						ns
	JMP High hold after CLK	Waveform 3						ns
	SUB_1, SUB_2 High hold after CLK	Waveform 3						ns
13	$\overline{INT}$ Low setup to CLK	Waveform 4						ns
14	$\overline{INT}$ Low Hold after CLK	Waveform 4						ns
15	$\overline{INT}$ High setup to CLK	Waveform 4						ns
16	$\overline{INT}$ High hold after CLK	Waveform 4						ns

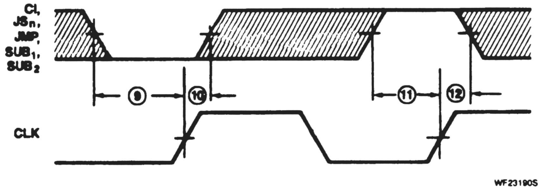
AC WAVEFORMS


CLK
①
②
③
⑤
PS$_n$,CO
④
WF22650S

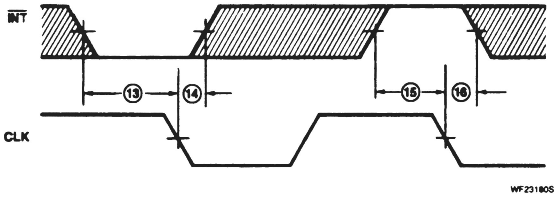
Waveform 1. Clock to Output Delays and Clock Pulse Width


$\overline{\text{RESET}}$
⑥
⑦
CLK
⑧
PS$_n$,CO
WF22660S

Waveform 2. Reset Pulse Width and Output Delays


CI,
JS$_n$,
JMP,
SUB$_1$,
SUB$_2$
⑨
⑩
⑪
⑫
CLK
WF23190S

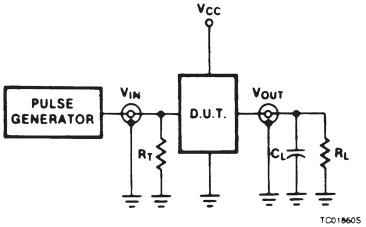
Waveform 3. Setup and Hold Times


$\overline{\text{INT}}$
⑬
⑭
⑮
⑯
CLK
WF23180S

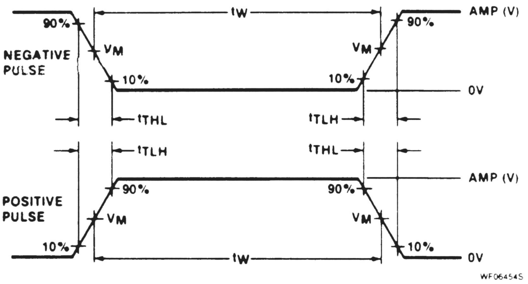
Waveform 4. $\overline{\text{INT}}$ Setup and Hold Times

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_CC
PULSE GENERATOR
V_IN
D.U.T.
V_OUT
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
V_M
t_W
t_THL
t_TLH
AMP (V)
0V
WF06454S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F841/842/843/844/845/846

Bus Interface Latches

'F841/'F842 10-Bit Bus Interface Latches, NINV/INV (3-State)
'F843/'F844 9-Bit Bus Interface Latches, NINV/INV (3-State)
'F845/'F846 8-Bit Bus Interface Latches, NINV/INV (3-State)
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F841, 74F842	5.5ns	60mA
74F843, 74F845	5.5ns	75mA
74F844, 74F846	6.2ns	60mA

FEATURES

- **High speed parallel latches with**
- **Extra data width for wide address/data paths or busses carrying parity**
* **High impedance NPN base input structure minimizes bus loading**
* **I_{IL} is 20μA vs 1000μA for AM29841 series**
- **Buffered control inputs to reduce AC effects**
- **Ideal where high speed, light loading, or increased fan-in is required as with MOS microprocessors**
- **Positive and negative over-shoots are clamped to ground**
- **3-state outputs glitch free during power-up and power-down**
- **48mA sink current**
- **Slim Dip 300 mil package**
- **Broadside pinout**
- **Pin-for-pin and function compatible with AMD AM29841-846 series**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V\pm10\%$; $T_A = 0°C$ to $+70°C$
24-Pin Plastic Slim DIP (300mil)	N74F841N, N74F842N, N74F843N, N74F844N, N74F845N, N74F846N
24-Pin Plastic SOL	N74F841D, N74F842D, N74F843D, N74F844D, N74F845D, N74F846D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_n	Data inputs	1.0/0.033	20μA/20μA
LE	Latch Enable input	1.0/0.033	20 A/20 A
$\overline{OE}$, $\overline{OE}_n$	Output Enable input (active-Low)	1.0/0.033	20μA/20μA
$\overline{MR}$	Master Reset input (active-Low)	1.0/0.033	20μA/20μA
$\overline{PRE}$	Preset input (active-Low)	1.0/0.033	20μA/20μA
Q_n	Data outputs	750/80	15mA/48mA
$\overline{Q}_n$	Data outputs	750/80	15mA/48mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

DESCRIPTION

The 'F841-'846 bus interface latch series are designed to provide extra data width for wider address/data paths of busses carrying parity.

The 'F841-'F842 series are functionally and pin compatible to the AMD AM29841-AM29846 series.

The 'F841 consists of ten D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is High. This allows asynchronous operation, as the output transition follows the data in transition.On the LE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output Enable ($\overline{OE}$) is Low. When $\overline{OE}$ is High the output is in the High-impedance state. The 'F842 is the inverted output version of 'F841.

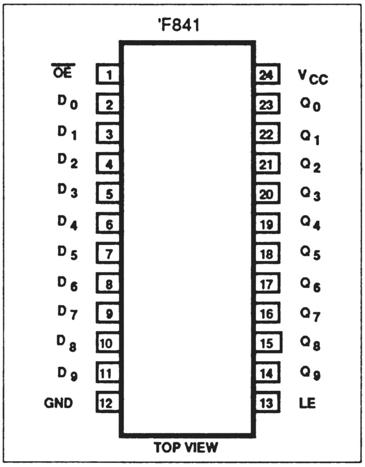
The 'F843 consists of nine D-type latches with 3-state outputs.

In addition to the LE and $\overline{OE}$ pins, the 'F843 has a Master Reset ($\overline{MR}$) pin and Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{MR}$ is Low, the outputs are Low if $\overline{OE}$ is Low. When $\overline{MR}$ is High, data can be entered into the latch. When $\overline{PRE}$ is Low, the outputs are High, if $\overline{OE}$ is Low. $\overline{PRE}$ overrides $\overline{MR}$. The 'F844 is the inverted output version of 'F843.
The 'F845 consists of eight D-type latches with 3-state outputs.

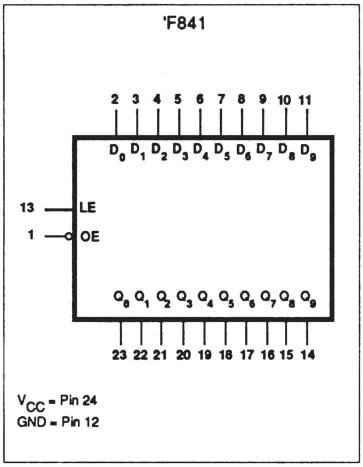
In addition to the LE, $\overline{OE}$, $\overline{MR}$ and $\overline{PRE}$ pins, the 'F845 has two additional $\overline{OE}$ pins making a total of three Output Enables ($\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$) pins.

The multiple Output Enables ($\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$) allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. The'F846 is the inverted output version of 'F845.

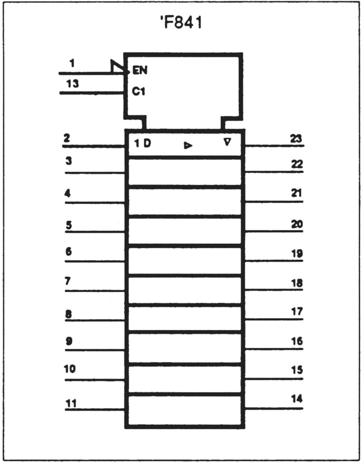
PIN CONFIGURATION


'F841
$\overline{OE}$ 1
D_0 2
D_1 3
D_2 4
D_3 5
D_4 6
D_5 7
D_6 8
D_7 9
D_8 10
D_9 11
GND 12
24 V_{CC}
23 Q_0
22 Q_1
21 Q_2
20 Q_3
19 Q_4
18 Q_5
17 Q_6
16 Q_7
15 Q_8
14 Q_9
13 LE
TOP VIEW

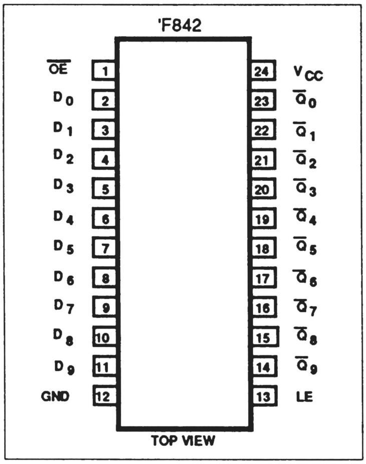
LOGIC SYMBOL


'F841
2 3 4 5 6 7 8 9 10 11
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8 D_9
13 LE
1 OE
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7 Q_8 Q_9
23 22 21 20 19 18 17 16 15 14
V_{CC} = Pin 24
GND = Pin 12

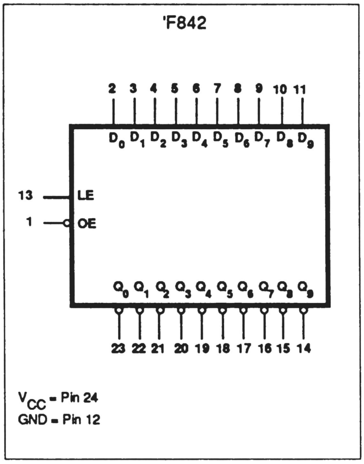
LOGIC SYMBOL(IEEE/IEC)


'F841
1 EN
13 C1
1D
2 3 4 5 6 7 8 9 10 11
23 22 21 20 19 18 17 16 15 14

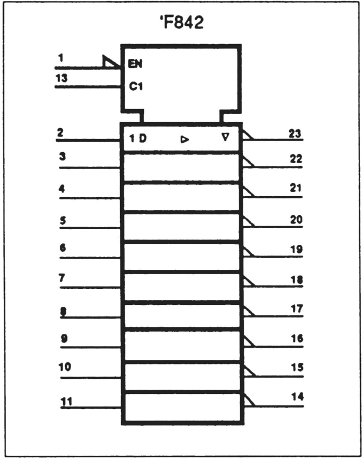
PIN CONFIGURATION


'F842
$\overline{OE}$ 1
D_0 2
D_1 3
D_2 4
D_3 5
D_4 6
D_5 7
D_6 8
D_7 9
D_8 10
D_9 11
GND 12
24 V_{CC}
23 $\overline{Q}_0$
22 $\overline{Q}_1$
21 $\overline{Q}_2$
20 $\overline{Q}_3$
19 $\overline{Q}_4$
18 $\overline{Q}_5$
17 $\overline{Q}_6$
16 $\overline{Q}_7$
15 $\overline{Q}_8$
14 $\overline{Q}_9$
13 LE
TOP VIEW

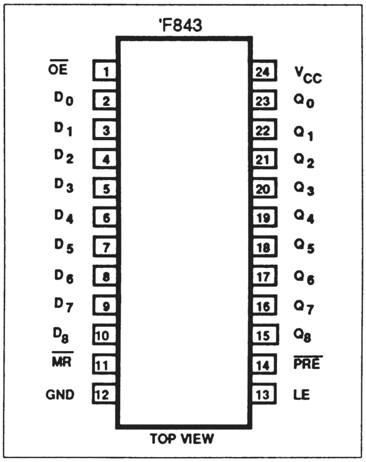
LOGIC SYMBOL


'F842
2 3 4 5 6 7 8 9 10 11
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8 D_9
13 LE
1 OE
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7 Q_8 Q_9
23 22 21 20 19 18 17 16 15 14
V_{CC} = Pin 24
GND = Pin 12

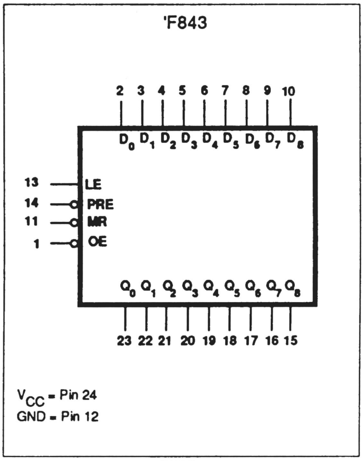
LOGIC SYMBOL(IEEE/IEC)


'F842
1 EN
13 C1
1D
2 3 4 5 6 7 8 9 10 11
23 22 21 20 19 18 17 16 15 14

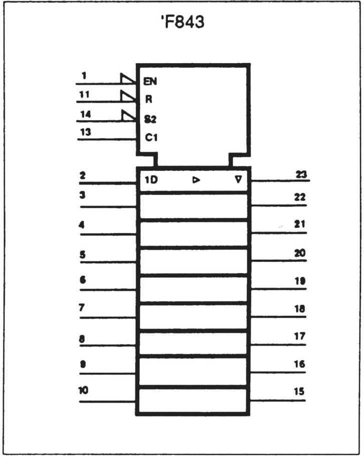
PIN CONFIGURATION


'F843
$\overline{OE}$ 1
D_0 2
D_1 3
D_2 4
D_3 5
D_4 6
D_5 7
D_6 8
D_7 9
D_8 10
$\overline{MR}$ 11
GND 12
24 V_{CC}
23 Q_0
22 Q_1
21 Q_2
20 Q_3
19 Q_4
18 Q_5
17 Q_6
16 Q_7
15 Q_8
14 $\overline{PRE}$
13 LE
TOP VIEW

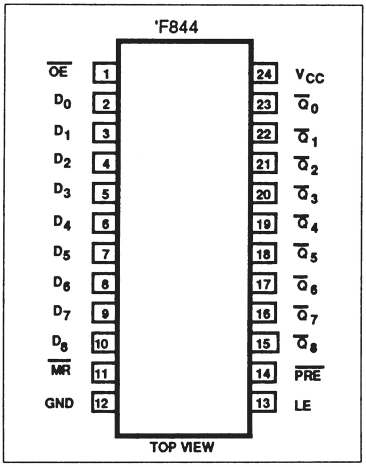
LOGIC SYMBOL


'F843
2 3 4 5 6 7 8 9 10
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8
13 LE
14 PRE
11 MR
1 OE
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7 Q_8
23 22 21 20 19 18 17 16 15
V_{CC} = Pin 24
GND = Pin 12

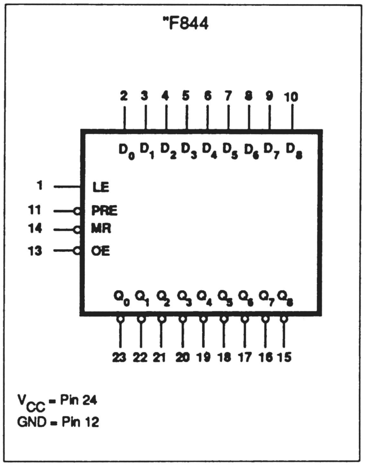
LOGIC SYMBOL(IEEE/IEC)


'F843
1 EN
11 R
14 S2
13 C1
1D
2 3 4 5 6 7 8 9 10
23 22 21 20 19 18 17 16 15

PIN CONFIGURATION

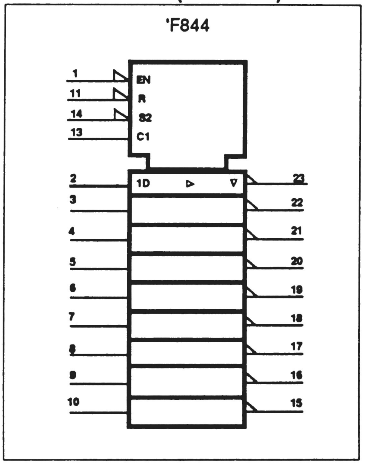

'F844
OE 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
D8 10
MR 11
GND 12
24 VCC
23 Q0
22 Q1
21 Q2
20 Q3
19 Q4
18 Q5
17 Q6
16 Q7
15 Q8
14 PRE
13 LE
TOP VIEW

LOGIC SYMBOL

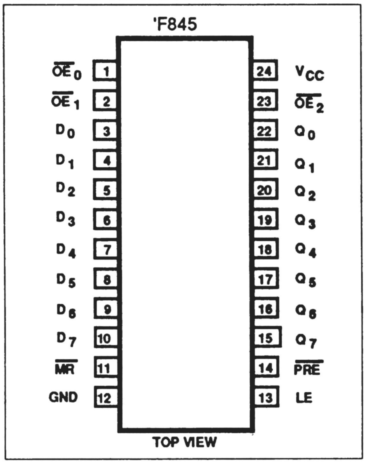

'F844
2 3 4 5 6 7 8 9 10
D0 D1 D2 D3 D4 D5 D6 D7 D8
1 LE
11 PRE
14 MR
13 OE
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8
23 22 21 20 19 18 17 16 15

V_{CC} = Pin 24
GND = Pin 12

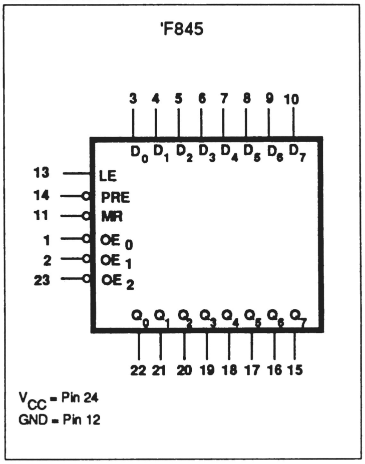
LOGIC SYMBOL(IEEE/IEC)


'F844
1 EN
11 R
14 S2
13 C1
2 1D ▷ ∇ 23
3 22
4 21
5 20
6 19
7 18
8 17
9 16
10 15

PIN CONFIGURATION

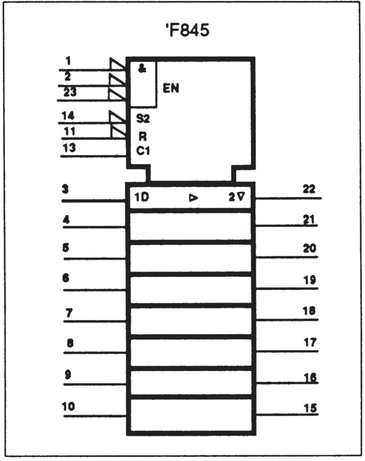

'F845
OE0 1
OE1 2
D0 3
D1 4
D2 5
D3 6
D4 7
D5 8
D6 9
D7 10
MR 11
GND 12
24 VCC
23 OE2
22 Q0
21 Q1
20 Q2
19 Q3
18 Q4
17 Q5
16 Q6
15 Q7
14 PRE
13 LE
TOP VIEW

LOGIC SYMBOL

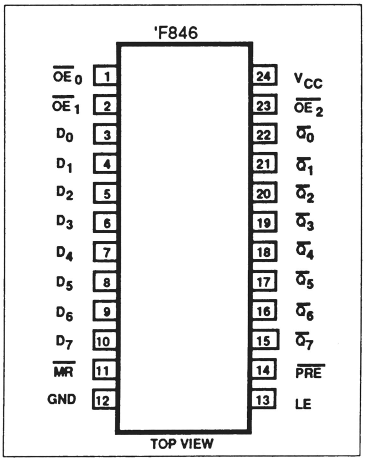

'F845
3 4 5 6 7 8 9 10
D0 D1 D2 D3 D4 D5 D6 D7
13 LE
14 PRE
11 MR
1 OE0
2 OE1
23 OE2
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
22 21 20 19 18 17 16 15

V_{CC} = Pin 24
GND = Pin 12

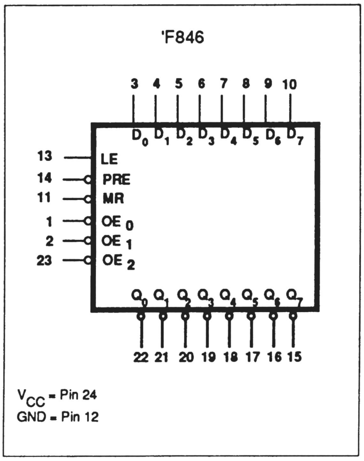
LOGIC SYMBOL(IEEE/IEC)


'F845
1
2
23
&
EN
14 S2
11 R
13 C1
3 1D ▷ 2∇ 22
4 21
5 20
6 19
7 18
8 17
9 16
10 15

PIN CONFIGURATION

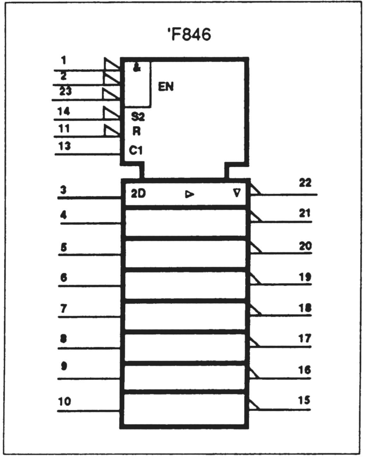

'F846
OE0 1
OE1 2
D0 3
D1 4
D2 5
D3 6
D4 7
D5 8
D6 9
D7 10
MR 11
GND 12
24 VCC
23 OE2
22 Q0
21 Q1
20 Q2
19 Q3
18 Q4
17 Q5
16 Q6
15 Q7
14 PRE
13 LE
TOP VIEW

LOGIC SYMBOL

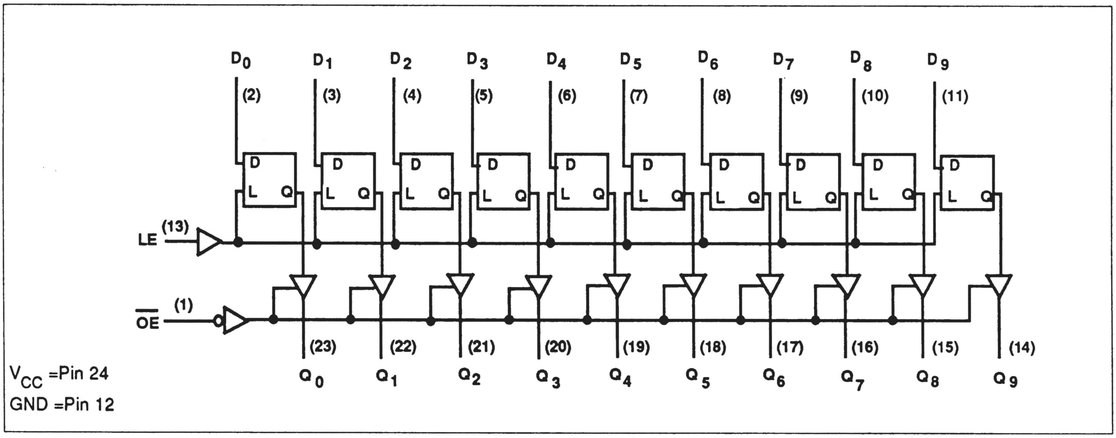

'F846
3 4 5 6 7 8 9 10
D0 D1 D2 D3 D4 D5 D6 D7
13 LE
14 PRE
11 MR
1 OE0
2 OE1
23 OE2
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
22 21 20 19 18 17 16 15

V_{CC} = Pin 24
GND = Pin 12

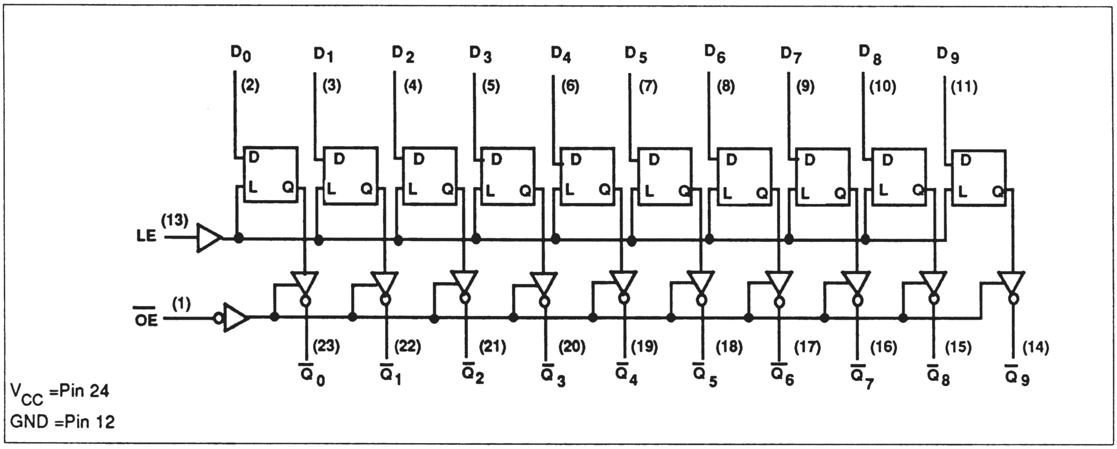
LOGIC SYMBOL(IEEE/IEC)


'F846
1
2
23
&
EN
14 S2
11 R
13 C1
3 2D ▷ ∇ 22
4 21
5 20
6 19
7 18
8 17
9 16
10 15

LOGIC DIAGRAM for 'F841


D_0 (2)
D_1 (3)
D_2 (4)
D_3 (5)
D_4 (6)
D_5 (7)
D_6 (8)
D_7 (9)
D_8 (10)
D_9 (11)
D
L Q
LE (13)
$\overline{OE}$ (1)
(23) Q_0
(22) Q_1
(21) Q_2
(20) Q_3
(19) Q_4
(18) Q_5
(17) Q_6
(16) Q_7
(15) Q_8
(14) Q_9
V_{CC} =Pin 24
GND =Pin 12

LOGIC DIAGRAM for 'F842

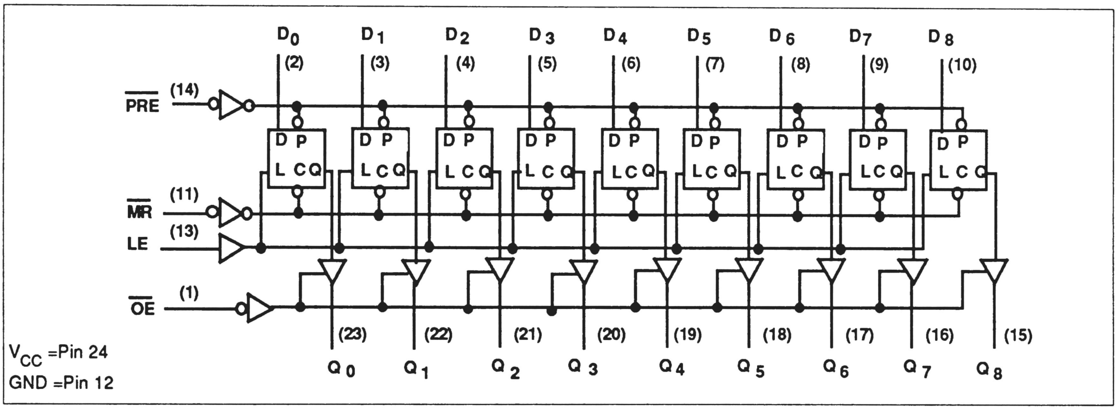

D_0 (2)
D_1 (3)
D_2 (4)
D_3 (5)
D_4 (6)
D_5 (7)
D_6 (8)
D_7 (9)
D_8 (10)
D_9 (11)
D
L Q
LE (13)
$\overline{OE}$ (1)
(23) $\overline{Q}_0$
(22) $\overline{Q}_1$
(21) $\overline{Q}_2$
(20) $\overline{Q}_3$
(19) $\overline{Q}_4$
(18) $\overline{Q}_5$
(17) $\overline{Q}_6$
(16) $\overline{Q}_7$
(15) $\overline{Q}_8$
(14) $\overline{Q}_9$
V_{CC} =Pin 24
GND =Pin 12

FUNCTION TABLE for 'F841 and 'F842

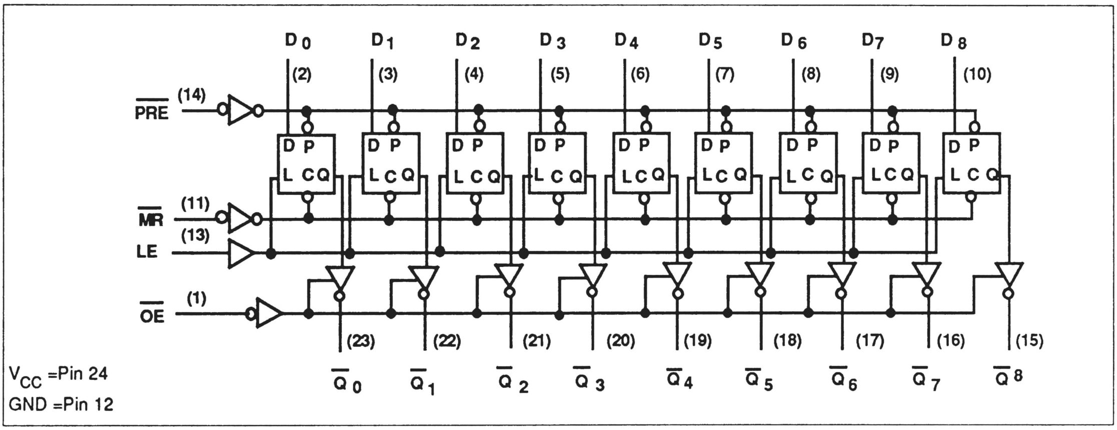
INPUTS			OUTPUTS		OPERATING MODE
			'F841	'F842	
$\overline{OE}$	LE	D_n	Q	$\overline{Q}$	
L	H	L	L	H	Transparent
L	H	H	H	L	
L	↓	l	L	H	Latched
L	↓	h	H	L	
H	X	X	Z	Z	Hi-Z
L	L	X	NC	NC	Hold

H= High voltage level
L= Low voltage level
h= High state one setup time before the High-to-Low LE transition
l = Low state one setup time before the High-to-Low LE transition
↓= High-to-Low transition
X=Don't care
NC=No change
Z =High impedance

LOGIC DIAGRAM for 'F843


D0 (2)
D1 (3)
D2 (4)
D3 (5)
D4 (6)
D5 (7)
D6 (8)
D7 (9)
D8 (10)
$\overline{PRE}$ (14)
$\overline{MR}$ (11)
LE (13)
$\overline{OE}$ (1)
D P
L C Q
(23) Q0
(22) Q1
(21) Q2
(20) Q3
(19) Q4
(18) Q5
(17) Q6
(16) Q7
(15) Q8
V_{CC} =Pin 24
GND =Pin 12

LOGIC DIAGRAM for 'F844

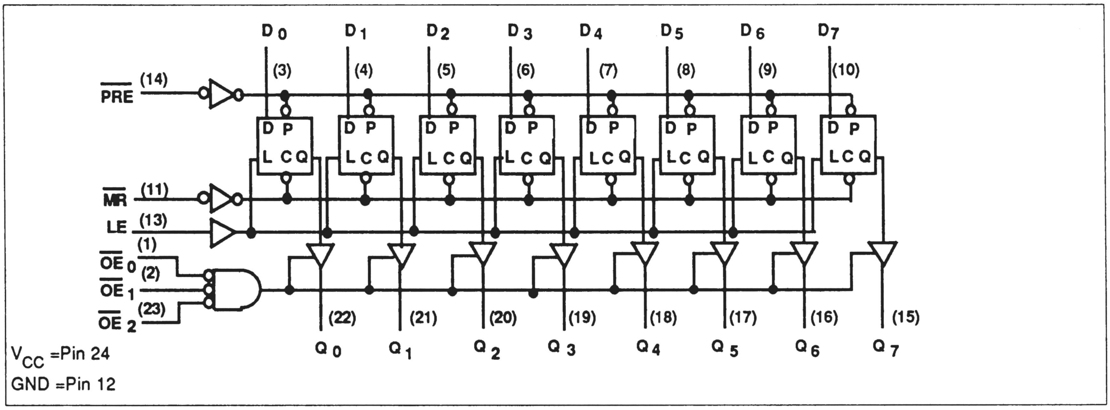

D0 (2)
D1 (3)
D2 (4)
D3 (5)
D4 (6)
D5 (7)
D6 (8)
D7 (9)
D8 (10)
$\overline{PRE}$ (14)
$\overline{MR}$ (11)
LE (13)
$\overline{OE}$ (1)
D P
L C Q
(23) $\overline{Q}_0$
(22) $\overline{Q}_1$
(21) $\overline{Q}_2$
(20) $\overline{Q}_3$
(19) $\overline{Q}_4$
(18) $\overline{Q}_5$
(17) $\overline{Q}_6$
(16) $\overline{Q}_7$
(15) $\overline{Q}_8$
V_{CC} =Pin 24
GND =Pin 12

FUNCTION TABLE for 'F843 and 'F844

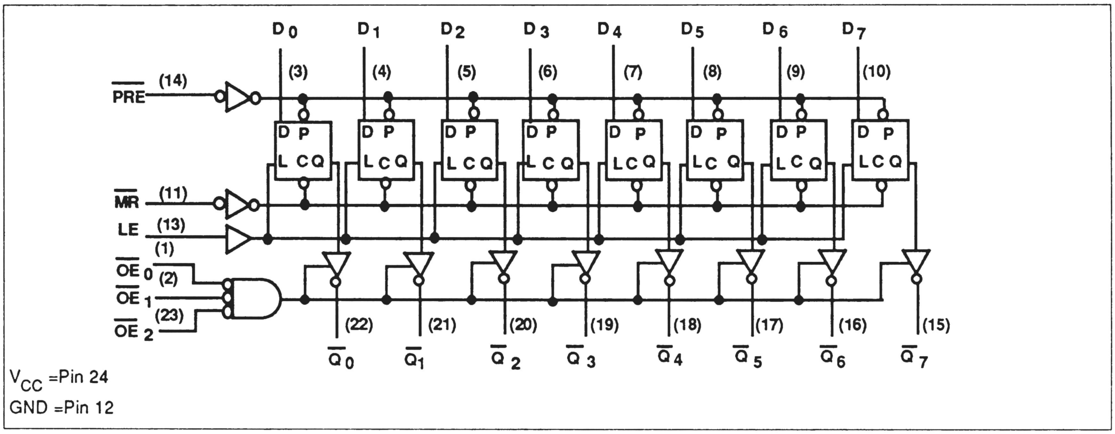
INPUTS					OUTPUTS		OPERATING MODE
					'F843	'F844	
$\overline{OE}$	$\overline{PRE}$	$\overline{MR}$	LE	D_n	Q	$\overline{Q}$	
L	L	X	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	H	H	H	L	L	H	Transparent
L	H	H	H	H	H	L	
L	H	H	↓	l	L	H	Latched
L	H	H	↓	h	H	L	
H	X	X	X	X	Z	Z	Hi-Z
L	H	H	L	X	NC	NC	Hold

H= High voltage level
L= Low voltage level
h= High state one setup time before the High-to-Low LE transition
l =Low state one setup time before the High-to-Low LE transition
↓=High-to-Low transition
X=Don't care
NC=No change
Z =High impedance

LOGIC DIAGRAM for 'F845


D0 D1 D2 D3 D4 D5 D6 D7
(3) (4) (5) (6) (7) (8) (9) (10)
$\overline{PRE}$ (14)
D P
L C Q
$\overline{MR}$ (11)
LE (13)
$\overline{OE}_0$ (1)
$\overline{OE}_1$ (2)
$\overline{OE}_2$ (23)
(22) (21) (20) (19) (18) (17) (16) (15)
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
V_{CC} =Pin 24
GND =Pin 12

LOGIC DIAGRAM for 'F846


D0 D1 D2 D3 D4 D5 D6 D7
(3) (4) (5) (6) (7) (8) (9) (10)
$\overline{PRE}$ (14)
D P
L C Q
$\overline{MR}$ (11)
LE (13)
$\overline{OE}_0$ (1)
$\overline{OE}_1$ (2)
$\overline{OE}_2$ (23)
(22) (21) (20) (19) (18) (17) (16) (15)
$\overline{Q}_0$ $\overline{Q}_1$ $\overline{Q}_2$ $\overline{Q}_3$ $\overline{Q}_4$ $\overline{Q}_5$ $\overline{Q}_6$ $\overline{Q}_7$
V_{CC} =Pin 24
GND =Pin 12

FUNCTION TABLE for 'F845 and 'F846

INPUTS					OUTPUTS		OPERATING MODE
					'F845	'F846	
$\overline{OE}_n$	$\overline{PRE}$	$\overline{MR}$	LE	D_n	Q	$\overline{Q}$	
L	L	X	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	H	H	H	L	L	H	Transparent
L	H	H	H	H	H	L	
L	H	H	↓	l	L	H	Latched
L	H	H	↓	h	H	L	
H	X	X	X	X	Z	Z	Hi-Z
L	H	H	L	X	NC	NC	Hold

H= High voltage level
L= Low voltage level
h= High state one setup time before the High-to-Low LE transition
l =Low state one setup time before the High-to-Low LE transition
↓=High-to-Low transition
X=Don't care
NC=No change
Z =High impedance

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	84	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			74F841, 74F842, 74F843, 74F844, 74F845, 74F846			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OH} = -15mA	±10% V_{CC}	2.0			V
						±5% V_{CC}	2.0			V
					I_{OH} = -3mA	±10% V_{CC}	2.4			V
						±5% V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage			V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OL} = MAX	±10% V_{CC}		0.38	0.55	V
						±5% V_{CC}		0.35	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7 V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5 V					-20	mA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F841	I_{CCH}	V_{CC} = MAX				50	65	mA
			I_{CCL}					60	80	mA
			I_{CCZ}					70	92	mA
I_{CC}	Supply current (total)	'F842	I_{CCH}	V_{CC} = MAX				40	60	mA
			I_{CCL}					65	90	mA
			I_{CCZ}					60	90	mA
I_{CC}	Supply current (total)	'F843 'F845	I_{CCH}	V_{CC} = MAX				65	90	mA
			I_{CCL}					75	100	mA
			I_{CCZ}					85	115	mA
I_{CC}	Supply current (total)	'F844 'F846	I_{CCH}	V_{CC} = MAX				50	70	mA
			I_{CCL}					70	95	mA
			I_{CCZ}					70	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	74F841, 74F842					UNIT
				T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	'F841	Waveform 1, 2	2.0 2.5	4.0 4.5	7.5 7.5	2.0 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay LE to Q_n or $\overline{Q}_n$		Waveform 1, 2	4.5 4.0	6.5 6.0	9.5 9.0	4.0 3.5	10.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	'F842	Waveform 1, 2	3.5 3.0	5.5 5.0	8.5 8.0	4.5 4.0	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to Q_n or $\overline{Q}_n$		Waveform 1, 2	5.0 4.5	7.0 6.5	10.0 9.0	3.0 3.0	10.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, $\overline{OE}_n$ to Q_n or $\overline{Q}_n$		Waveform 5 Waveform 6	2.5 6.5	4.5 8.5	8.0 12.0	2.0 5.5	8.5 13.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level, $\overline{OE}_n$ to Q_n or $\overline{Q}_n$		Waveform 5 Waveform 6	1.0 1.0	4.5 5.0	8.0 8.0	1.0 1.0	8.5 8.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	74F841, 74F842					UNIT
				T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, High or Low D_n to LE		Waveform 4	0.0 0.0			1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to LE	'F841	Waveform 4	2.5 3.0			3.0 4.0		ns
$t_w(H)$	LE Pulse width, High		Waveform 4	3.5			4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to LE	'F842	Waveform 4	3.0 3.5			3.5 4.5		ns
$t_w(H)$	LE Pulse width, High		Waveform 4	3.0			3.0		ns

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F843, 74F845					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	Waveform 1, 2	2.0 2.5	4.5 4.5	7.5 8.0	2.0 2.5	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to Q_n or $\overline{Q}_n$	Waveform 1, 2	4.5 4.0	6.5 6.0	9.5 8.5	4.0 4.0	10.0 8.5	ns
t_{PLH}	Propagation delay $\overline{PRE}$ to Q_n or $\overline{Q}_n$	Waveform 3	3.5	5.5	8.5	3.0	9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n or $\overline{Q}_n$	Waveform 3	2.0	4.5	7.5	2.0	8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, $\overline{OE}_n$ to Q_n or $\overline{Q}_n$	Waveform 5 Waveform 6	2.5 5.5	4.5 7.5	7.5 10.5	2.0 5.0	8.0 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level, $\overline{OE}_n$ to Q_n or $\overline{Q}_n$	Waveform 5 Waveform 6	1.0 1.0	4.5 5.0	8.0 8.0	1.0 1.0	8.5 8.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	74F843, 74F845					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, High or Low D_n to LE	Waveform 4	1.0 1.0			1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to LE	Waveform 4	3.0 2.5			3.0 3.0		ns
$t_w(H)$	LE Pulse width, High	Waveform 4	3.5			3.5		ns
$t_w(L)$	$\overline{PRE}$ Pulse width, Low	Waveform 3	7.0			7.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 3	4.5			4.5		ns
t_{rec}	$\overline{PRE}$ Recovery time	Waveform 3	0.0			0.0		ns
t_{rec}	$\overline{MR}$ Recovery time	Waveform 3	2.0			2.0		ns

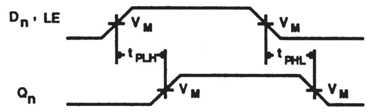
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F844, 74F846					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	Waveform 1, 2	3.5 3.0	5.5 5.0	8.5 8.0	3.0 3.0	9.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to Q_n or $\overline{Q}_n$	Waveform 1, 2	5.0 4.5	7.0 6.5	10.0 9.0	5.0 4.5	10.5 9.5	ns
t_{PLH}	Propagation delay $\overline{PRE}$ to Q_n or $\overline{Q}_n$	Waveform 3	3.5	5.5	8.5	3.0	9.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n or $\overline{Q}_n$	Waveform 3	5.0	7.0	10.0	4.5	10.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, $\overline{OE}_n$ to Q_n or $\overline{Q}_n$	Waveform 5 Waveform 6	2.5 6.5	5.0 8.5	7.5 11.5	2.0 5.5	8.0 12.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level, $\overline{OE}_n$ to Q_n or $\overline{Q}_n$	Waveform 5 Waveform 6	1.0 1.0	4.5 5.0	8.0 8.0	1.0 1.0	8.5 8.5	ns

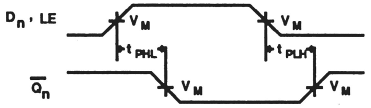
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	74F844, 74F846					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, High or Low D_n to LE	Waveform 4	0.0 0.0			0.0 0.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to LE	Waveform 4	3.0 4.0			3.0 4.0		ns
$t_w(H)$	LE Pulse width, High	Waveform 4	3.0			3.0		ns
$t_w(L)$	$\overline{PRE}$ Pulse width, Low	Waveform 3	4.0			5.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 3	4.0			5.0		ns
t_{rec}	$\overline{PRE}$ Recovery time	Waveform 3	0.0			0.0		ns
t_{rec}	$\overline{MR}$ Recovery time	Waveform 3	3.5			4.5		ns

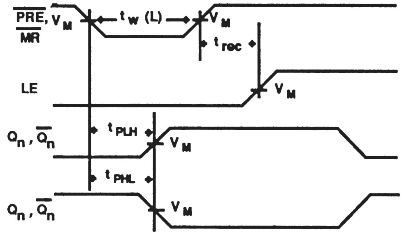
AC WAVEFORMS


D_n, LE
Q_n
V_M
t_{PLH}
t_{PHL}

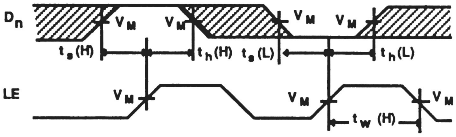
Waveform 1. Propagation Delay, Non-Inverting Path


D_n, LE
Q̅_n
V_M
t_{PHL}
t_{PLH}

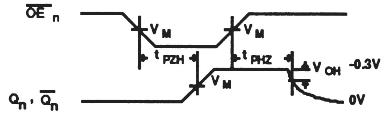
Waveform 2. Propagation Delay, Inverting Path


PRE, MR
LE
Q_n, Q̅_n
Q_n, Q̅_n
V_M
t_w (L)
t_{rec}
t_{PLH}
t_{PHL}

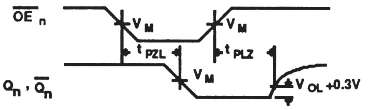
Waveform 3.
Master Reset and Preset Pulse Width, Master Reset and Preset to Output Delay and Master Reset and Preset to Latch Enable Recovery Time


D_n
LE
V_M
t_s(H)
t_h(H)
t_s(L)
t_h(L)
t_w (H)

Waveform 4. Data Setup And Hold Times


OE_n
Q_n, Q̅_n
V_M
t_{PZH}
t_{PHZ}
V_{OH} -0.3V
0V

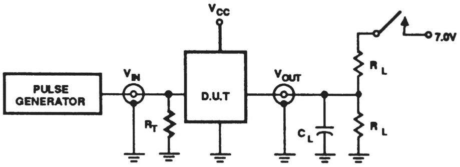
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level


OE_n
Q_n, Q̅_n
V_M
t_{PZL}
t_{PLZ}
V_{OL} +0.3V

Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
7.0V
PULSE GENERATOR
V_{IN}
R_T
D.U.T
V_{OUT}
C_L
R_L
R_L

Test Circuit For 3-State Outputs

SWITCH POSITION

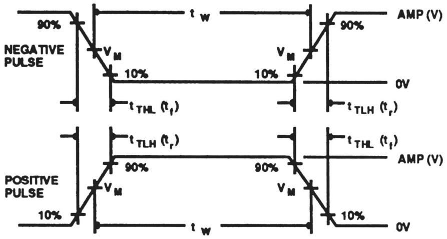
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
V_M
t_w
AMP (V)
0V
t_{THL} (t_f)
t_{TLH} (t_r)

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F847

Shift Register

10/9-Bit Serial/Parallel-In Serial Out Shift Register

Preliminary Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F847	150MHz	55mA

- **Both true and complementary outputs for 10 bit applications**
- **Single true output for 9 bit applications**
- **Suited for high resolution bit map graphics**

DESCRIPTION

The 74F847 is a high speed 10/9-bit Serial/Parallel-In Serial Out Shift Register. Data is shifted right on every Low to High transition of the CP input when the $\overline{CE}$ input is Low and the $\overline{PE}$ input is High. While the $\overline{PE}$ input is High, the shift is inhibited, and a word present on the inputs (D_0-D_7) will be loaded into the shift register on every Low to High transition of the CP input with no regard to the state of of the $\overline{CE}$ input. Three outputs are provided: Q_8 for 9 bit applications and Q_9 and $\overline{Q}_9$ for 10 bit applications. Q_9 and $\overline{Q}_9$ can be used independently or together to drive a twisted pair.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F847N
20-Pin Plastic SOL	N74F847D

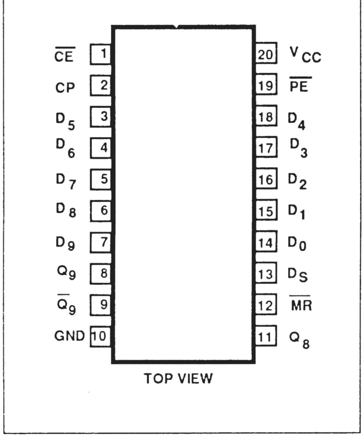
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0-D_9	Parallel data inputs	1.0/1.0	20μA/0.6mA
D_S	Serial data input (Shift right)	1.0/1.0	20μA/0.6mA
CP	Clock input (Active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{CE}$	Clock Enable input (Active Low)	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel Enable input (Active Low)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset input (Active Low)	1.0/1.0	20μA/0.6mA
Q_8,Q_9	True data outputs	50/33	1.0mA/20mA
$\overline{Q}_9$	Complementary data output	50/33	1.0mA/20mA

NOTE:

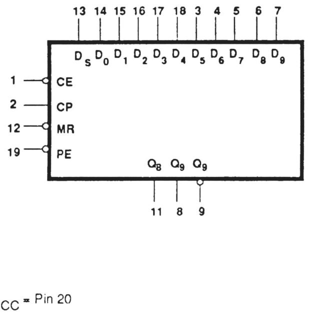
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



$\overline{CE}$ 1
CP 2
D_5 3
D_6 4
D_7 5
D_8 6
D_9 7
Q_9 8
$\overline{Q}_9$ 9
GND 10
20 V_{CC}
19 $\overline{PE}$
18 D_4
17 D_3
16 D_2
15 D_1
14 D_0
13 D_S
12 $\overline{MR}$
11 Q_8
TOP VIEW

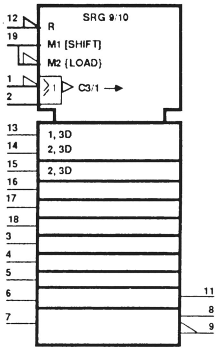
LOGIC SYMBOL



13 14 15 16 17 18 3 4 5 6 7
D_S D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8 D_9
1 CE
2 CP
12 MR
19 PE
Q_8 Q_9 Q_9
11 8 9

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)



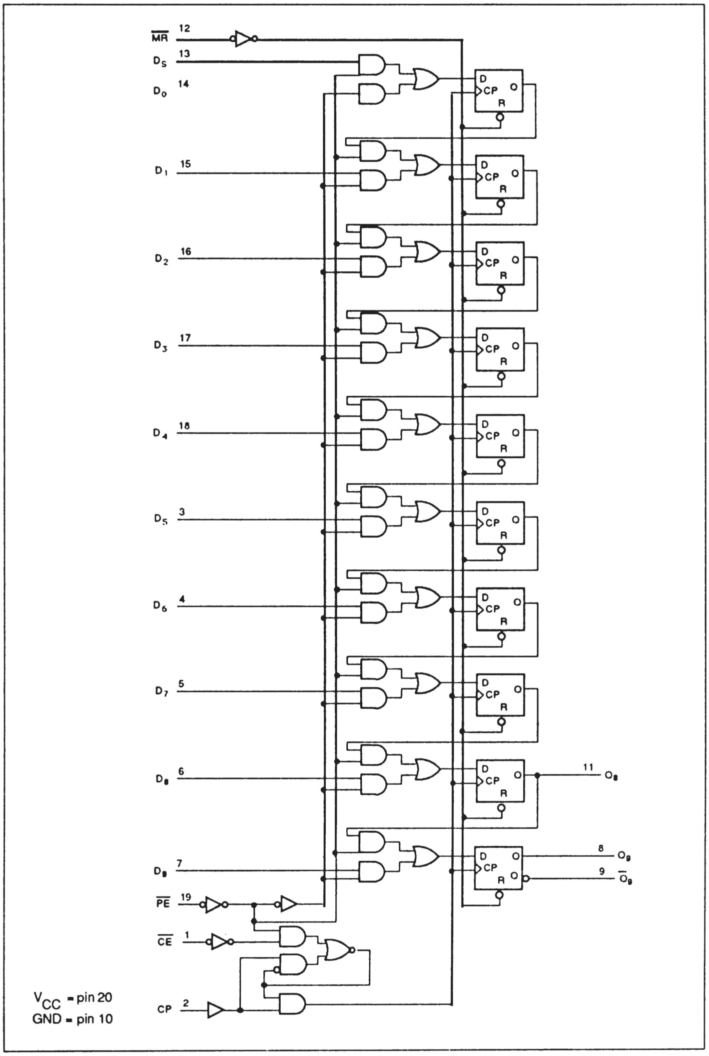
SRG 9/10
12 R
19 M1 [SHIFT]
M2 [LOAD]
1
2
C3/1 →
13 1, 3D
14 2, 3D
15 2, 3D
16
17
18
3
4
5
6
7
11
8
9

FUNCTION TABLE

INPUTS				OUTPUTS			OPERATING MODE
CP	$\overline{PE}$	$\overline{CE}$	$\overline{MR}$	Q_8	Q_9	$\overline{Q}_9$	
↑	h	l	H	q_7	q_8	$\overline{q}_8$	Serial shift, serial load
↑	l	X	H	q_8	q_9	$\overline{q}_9$	Parallel load
X	h	h	H	q_8	q_9	$\overline{q}_9$	Disabled
X	X	X	L	L	L	H	Master reset

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
q_n = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM


$\overline{MR}$ 12
D_S 13
D_0 14
D_1 15
D_2 16
D_3 17
D_4 18
D_5 3
D_6 4
D_7 5
D_8 6
D_9 7
$\overline{PE}$ 19
$\overline{CE}$ 1
CP 2
D
CP
Q
R
11 Q_8
8 Q_9
9 $\overline{Q}_9$
V_{CC} = pin 20
GND = pin 10

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			55		mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

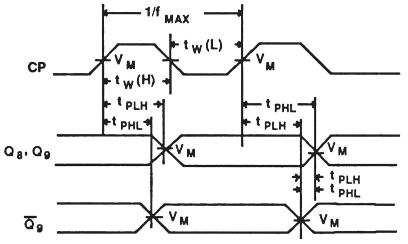
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	160	170		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_8, Q_9, $\overline{Q}_9$	Waveform 1	2.0 2.0	7.0 7.0	10.0 10.0	2.0 2.0	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay (skew) Q_9 to $\overline{Q}_9$	Waveform 1	1.0 1.0	3.0 3.0	5.0 5.0	1.0 1.0	6.0 6.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_8, Q_9	Waveform 2	2.0	5.0	8.0	2.0	9.0	ns
t_{PLH}	Propagation delay $\overline{MR}$ to $\overline{Q}_9$	Waveform 2	2.0	5.0	8.0	2.0	9.0	ns

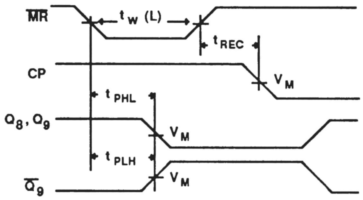
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 4	3.5 3.5			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_s to CP	Waveform 4	3.0 2.5			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_s to CP	Waveform 4	0 0			1.0 0		ns
$t_s(L)$	Setup time, Low $\overline{CE}$ to CP	Waveform 3	5.0			6.0		ns
$t_h(H)$	Hold time, High $\overline{CE}$ to CP	Waveform 3	0			0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 4	4.5 4.5			5.5 5.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 4	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	6.0 5.0			6.5 5.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	4.0			5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	4.0			4.5		ns

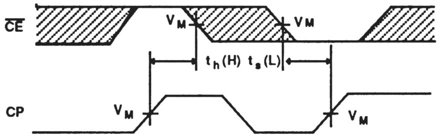
AC WAVEFORMS


1/f MAX
CP
V_M
$t_W(L)$
$t_W(H)$
t_{PLH}
t_{PHL}
t_{PHL}
t_{PLH}
Q_8, Q_9
t_{PLH}
t_{PHL}
$\overline{Q}_9$

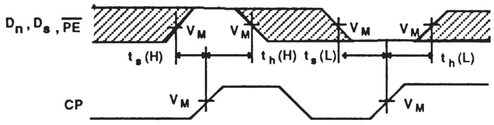
Waveform 1. Propagation Delay, Clock Input to Outputs, True Output To Complementary Output, Clock Widths, and Maximum Clock Frequency


$\overline{MR}$
$t_W(L)$
t_{REC}
CP
V_M
t_{PHL}
Q_8, Q_9
t_{PLH}
$\overline{Q}_9$

Waveform 2. Master Reset Pulse Width,Master Reset to Output Delay and Master Reset to Clock Recovery Time


$\overline{CE}$
V_M
$t_h(H)$
$t_s(L)$
CP
V_M

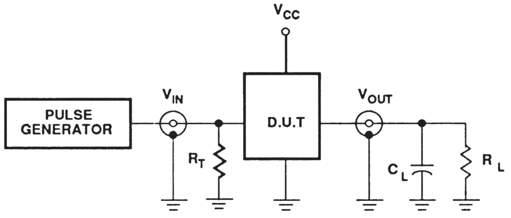
Waveform 3. Setup And Hold Times


$D_n, D_s, \overline{PE}$
V_M
$t_s(H)$
$t_h(H)$
$t_s(L)$
$t_h(L)$
CP
V_M

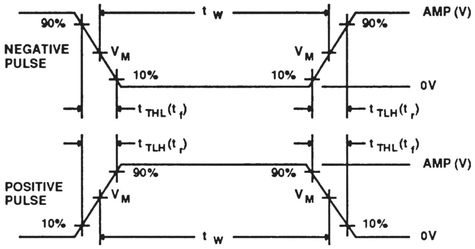
Waveform 4. Setup And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
R_T
D.U.T
V_{OUT}
C_L
R_L

Test Circuit For Totem-Pole Outputs


NEGATIVE PULSE
90%
V_M
10%
t_w
AMP (V)
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
POSITIVE PULSE
AMP (V)
0V

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F899

Dual Latch Transceiver with Parity

9-Bit Dual Latch Transceiver With 8-bit Parity Generator/Checker (3-State Outputs)
Preliminary Specification

FEATURES

- **Combines 'F543 and 'F280 functions into one package**
- **Combines 'F657 and 'F373 functions into one package (No need to change $T/\overline{R}$ to check parity)**
- **Output sink of 24 mA for the A-Bus and 64 mA for the B-bus**
- **Symmetrical (A and B bus functions are identical)**
- **Selectable generate parity or "feed-through" parity for A-to-B and B-to-A directions**
- **Independant transparent latches for A-to-B and B-to-A directions**
- **Selectable ODD/$\overline{\text{EVEN}}$ parity**
- **Continously checks parity of both A bus and B bus latches as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$**
- **Ability to simultaneously generate and check parity**
- **Can simultaneously read/latch A and B bus data**

DESCRIPTION

The 'F899 is a 9-bit to 9-bit parity transceiver with separate transparent latches for the A bus and B bus. Either bus can generate or check parity. The parity bit can be fed-through with no change or the generated parity can be substituted with in 3-State.

TYPE	TYPICAL PROPAGATION DELAY	MAX SUPPLY CURRENT (TOTAL)
74F899	8.0ns	150mA

ORDERING INFORMATION

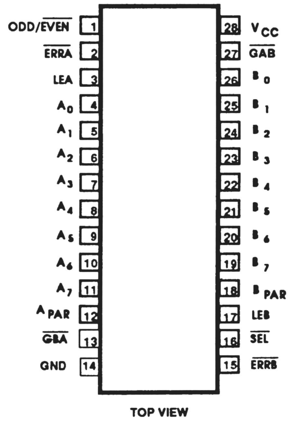
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP (600mil)	N74F889N
28-Pin PLCC	N74F889A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

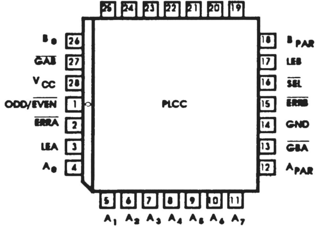
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	Latched A bus 3-State inputs	3.5/0.117	70µA/70µA
B_0 - B_7	Latched B bus 3-State inputs	3.5/0.117	70µA/70µA
A_{PAR}	A bus parity 3-State input	1.0/0.033	20µA/20µA
B_{PAR}	B bus parity 3-State input	1.0/0.033	20µA/20µA
ODD/$\overline{\text{EVEN}}$	Parity Select Input (Low for EVEN parity)	1.0/0.033	20µA/20µA
$\overline{\text{GBA}}$,$\overline{\text{GAB}}$	Output Enable Inputs (Gate A to B, B to A)	2.0/0.066	40µA/40µA
$\overline{\text{SEL}}$	Mode Select Input (Low for generate)	1.0/0.033	20µA/20µA
LEA,LEB	Latch Enable Inputs (Low for latch)	1.0/0.033	20µA/20µA
$\overline{\text{ERRA}}$, $\overline{\text{ERRB}}$	Error Signal Outputs (active Low)	150/40	3mA/24mA
A_0 - A_7	A bus 3-State outputs	150/40	3mA/24mA
B_0 - B_7	B bus 3-State outputs	750/106.7	15mA/64mA
A_{PAR}	A bus parity 3-State output	150/40	3mA/24mA
B_{PAR}	B bus parity 3-State output	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

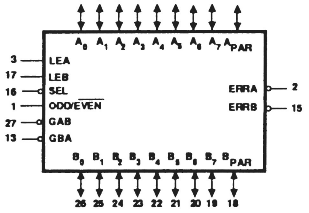
DIP PIN CONFIGURATION


ODD/EVEN 1
ERRA 2
LEA 3
A0 4
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
APAR 12
GBA 13
GND 14
28 VCC
27 GAB
26 B0
25 B1
24 B2
23 B3
22 B4
21 B5
20 B6
19 B7
18 BPAR
17 LEB
16 SEL
15 ERRB
TOP VIEW

PLCC PIN CONFIGURATION


B1 B2 B3 B4 B5 B6 B7
25 24 23 22 21 20 19
B0 26
GAB 27
VCC 28
ODD/EVEN 1
ERRA 2
LEA 3
A0 4
PLCC
18 BPAR
17 LEB
16 SEL
15 ERRB
14 GND
13 GBA
12 APAR
5 6 7 8 9 10 11
A1 A2 A3 A4 A5 A6 A7

LOGIC SYMBOL


4 5 6 7 8 9 10 11 12
A0 A1 A2 A3 A4 A5 A6 A7 APAR
3 LEA
17 LEB
16 SEL
1 ODD/EVEN
27 GAB
13 GBA
ERRA 2
ERRB 15
B0 B1 B2 B3 B4 B5 B6 B7 BPAR
26 25 24 23 22 21 20 19 18

V_{CC} = Pin 28
GND = Pin 14

September 22, 1988

The device has a guaranteed current sinking capability of 24 mA for the A-bus and 64 mA for the B-bus. Otherwise, the part is symmetrical (A and B bus functions are identical).

The 'F899 features independent latch enables for the A and B bus latches, a select pin for ODD/$\overline{\text{EVEN}}$ parity, and separate error signal output pins for checking parity.

FUNCTIONAL DESCRIPTION:

The 'F899 has three principal modes of operation which are outlined below. All modes apply to both the A-to-B and B-to-A directions.

Transparent latch, Generate parity, Check A and B bus parity:
Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as B_{PAR} (A_{PAR}). If LEA and LEB are High and the Mode Select ($\overline{\text{SEL}}$) is Low, the parity generated from A_0-A_7 and B_0-B_7 can be checked and monitored by $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$. (Fault detection on both input and output buses.)

Transparent latch, Feed-through parity, Check A and B bus parity:
Bus A (B) communicates to Bus B (A) in a feed-through mode if $\overline{\text{SEL}}$ is High. Parity is still generated and checked as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ and can be used as an interrupt to signal a data/parity bit error to the CPU.

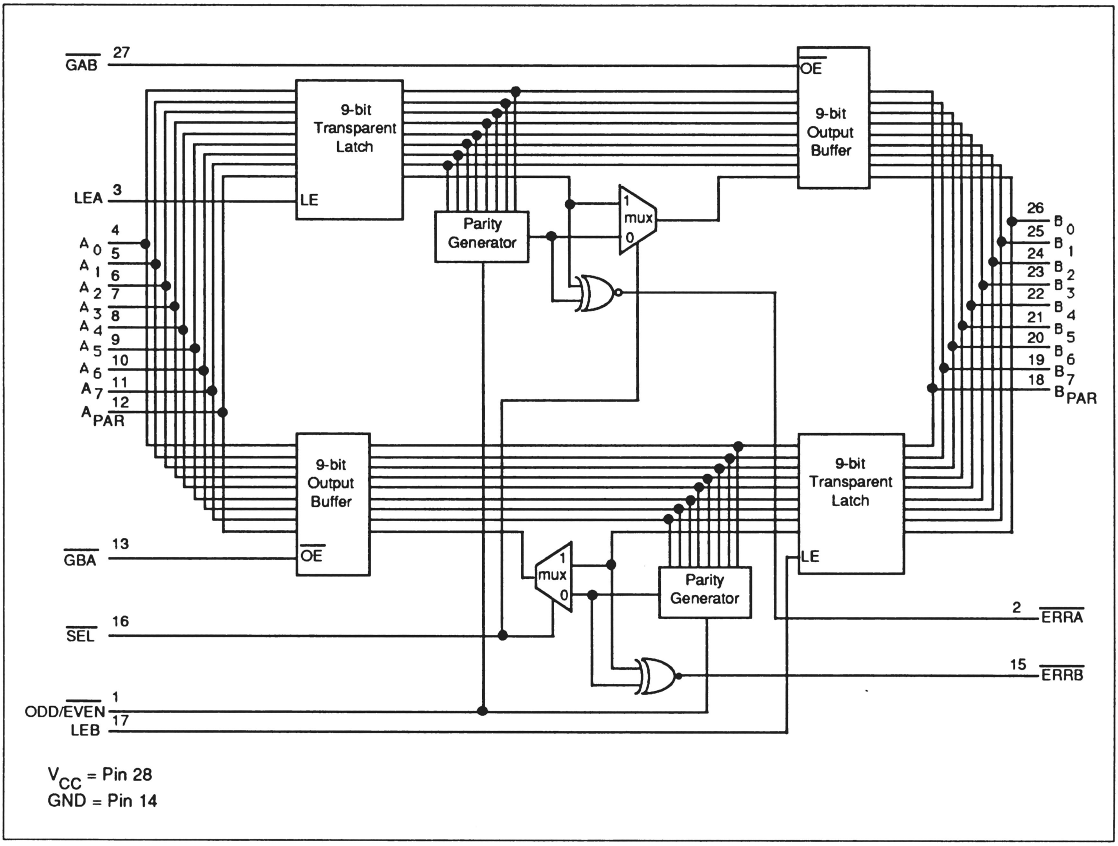
Latched input, Generate/Feed-through parity, Check A (and B) bus parity:
Independent latch enables (LEA and LEB) allow other permutations of:
Transparent latch / 1bus latched / both busses latched
Feed-through parity / generate parity
Check in bus parity / check out bus parity / check in and out bus parity
See function table below.

FUNCTION TABLE

INPUTS					OPERATING MODE
GAB	GBA	$\overline{\text{SEL}}$	LEA	LEB	
H	H	X	X	X	3-state A bus and B bus (Input A & B simultaneously)
H	L	L	L	H	B → A, Transparent B latch, Generate parity from B_0-B_7, Check B bus parity
H	L	L	H	H	B → A, Transparent A & B latch, Generate parity from B_0-B_7, Check A & B bus parity
H	L	L	X	L	B → A, B bus latched, Generate parity from latched B_0-B_7 data, Check B bus parity
H	L	H	X	H	B → A, Transparent B latch, Parity feed-through, Check B bus parity
H	L	H	H	H	B → A, Transparent A & B latch, Parity feed-through, Check A & B bus parity
L	H	L	H	X	A → B, Transparent A latch, Generate parity from A_0-A_7, Check A bus parity
L	H	L	H	H	A → B, Transparent A & B latch, Generate parity from A_0-A_7, Check A & B bus parity
L	H	L	L	X	A → B, A bus latched, Generate parity from latched A_0-A_7 data, Check A bus parity
L	H	H	H	L	A → B, Transparent A latch, Parity feed-through, Check A bus parity
L	H	H	H	H	A → B, Transparent A & B latch, Parity feed-through, Check A & B bus parity
L	L	X	X	X	Output to A bus and B bus (NOT ALLOWED)

H = High voltage level
L = Low voltage level
X = Don't care

BLOCK DIAGRAM


GAB 27
LEA 3
A0 4
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
APAR 12
GBA 13
SEL 16
ODD/EVEN 1
LEB 17
9-bit Transparent Latch
LE
Parity Generator
1 mux 0
OE
9-bit Output Buffer
26 B0
25 B1
24 B2
23 B3
22 B4
21 B5
20 B6
19 B7
18 BPAR
9-bit Output Buffer
OE
9-bit Transparent Latch
LE
1 mux 0
Parity Generator
2 ERRA
15 ERRB

V_{CC} = Pin 28
GND = Pin 14

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	A_0 - A_7, A_{PAR}, $\overline{ERRA}$, $\overline{ERRB}$	48	mA
		B_0 - B_7, B_{PAR}	128	
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0 - A_7			-3	mA
		B_0 - B_7			-15	
I_{OL}	Low-level output current	A_0 - A_7			24	mA
		B_0 - B_7			64	
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	All outputs	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		B_0-B_7, B_{PAR}		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7, A_{PAR}, $\overline{\text{ERRA}}$, $\overline{\text{ERRB}}$	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7, B_{PAR}		I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	Other Inputs	V_{CC} = 0.0V, V_I = 7.0V					100	μA
		A_0-A_7, A_{PAR}	V_{CC} = MAX, V_I = 5.5V					2.0	mA
		B_0-B_7, B_{PAR}						1.0	mA
I_{IH}	High-level input current	ODD/$\overline{\text{EVEN}}$, $\overline{\text{SEL}}$,LEA,LEB	V_{CC} = MAX, V_I = 2.7V					20	μA
		$\overline{\text{GAB}}$, $\overline{\text{GBA}}$						40	μA
I_{IL}	Low-level input current	ODD/$\overline{\text{EVEN}}$, $\overline{\text{SEL}}$,LEA,LEB	V_{CC} = MAX, V_I = 0.5V					-20	μA
		$\overline{\text{GAB}}$, $\overline{\text{GBA}}$						-40	μA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied	A_0-A_7, A_{PAR} B_0-B_7, B_{PAR}	V_{CC} = MAX, V_O = 2.7V					70	μA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-70	μA
I_{OZH}	Off-state output current High-level voltage applied	ODD/$\overline{\text{EVEN}}$, $\overline{\text{SEL}}$,LEA,LEB, $\overline{\text{GAB}}$, $\overline{\text{GBA}}$	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V					50	μA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX ,V_{IH} = MIN, V_O = 0.5V					-50	μA
I_{OS}	Short-circuit output current[3]	A_0-A_7, A_{PAR}	V_{CC} = MAX			-60		-150	mA
		B_0-B_7, B_{PAR}				-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				90	125	mA
		I_{CCL}					106	150	mA
		I_{CCZ}					98	145	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

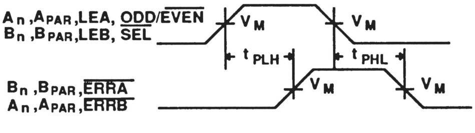
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay (Transparent latch) A_n to B_n or B_n to A_n	Waveform 1		8.0 8.0		5.0 5.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay (Feed-through Parity) A_{PAR} to B_{PAR} or B_{PAR} to A_{PAR}	Waveform 1		8.0 8.0		5.0 5.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay (Generate Parity) A_n, A_{PAR} to B_{PAR} or B_n, B_{PAR} to A_{PAR}	Waveform 1		10.0 10.0		8.0 8.0	15.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay (Check Parity) A_n, A_{PAR} to $\overline{ERRA}$ or B_n, B_{PAR} to $\overline{ERRB}$	Waveform 1		10.0 10.0		8.0 8.0	15.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{EVEN}$ to $\overline{ERRA}$, $\overline{ERRB}$, A_{PAR}, or B_{PAR}	Waveform 1		10.0 10.0		8.0 8.0	15.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SEL}$ to A_{PAR}, B_{PAR}	Waveform 1		8.0 8.0		5.0 5.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay LEA to B_n, B_{PAR} or LEB to A_n, A_{PAR}	Waveform 1		8.0 8.0		5.0 5.0	12.0 12.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{GBA}$ to A_n, A_{PAR} or $\overline{GAB}$ to B_n, B_{PAR}	Waveform 3, 4		10.0 10.0		8.0 8.0	15.0 15.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{GBA}$ to A_n, A_{PAR} or $\overline{GAB}$ to B_n, B_{PAR}	Waveform 3, 4		10.0 10.0		8.0 8.0	15.0 15.0	ns

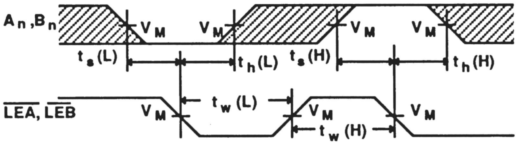
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time A_n to LEA or B_n to LEB	Waveform 2	3.0 3.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time A_n to LEA or B_n to LEB	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	Pulse width LEA or LEB	Waveform 2	5.0 5.0			5.0 5.0		ns

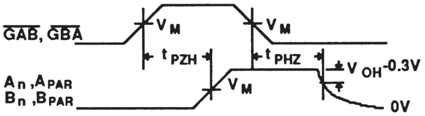
AC WAVEFORMS


An ,APAR,LEA, ODD/EVEN
Bn ,BPAR,LEB, SEL
VM
VM
tPLH
tPHL
Bn ,BPAR,ERRA
An ,APAR,ERRB
VM
VM

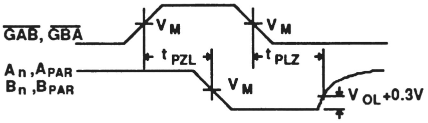
Waveform 1. Propagation Delay For Input To Output


An ,Bn
VM
VM
VM
VM
ts(L)
th(L)
ts(H)
th(H)
LEA, LEB
VM
tw (L)
VM
tw (H)
VM

Waveform 2. Data Setup And Hold Times And LEA, LEB Pulse Widths


GAB, GBA
VM
VM
tPZH
tPHZ
VOH-0.3V
An ,APAR
Bn ,BPAR
VM
0V

Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level

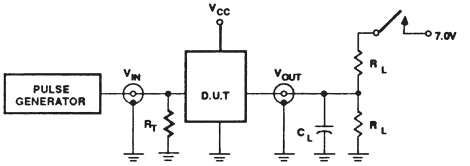

GAB, GBA
VM
VM
tPZL
tPLZ
An ,APAR
Bn ,BPAR
VM
VOL+0.3V

Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T
VOUT
RT
CL
RL

Test Circuit For 3-State Outputs

SWITCH POSITION

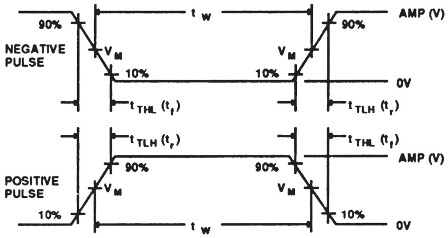
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


90%
NEGATIVE PULSE
VM
10%
tw
VM
10%
90%
AMP (V)
0V
tTHL (tf)
tTLH (tr)
tTLH (tr)
tTHL (tf)
AMP (V)
POSITIVE PULSE
90%
VM
10%
90%
VM
10%
tw
0V

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F1604
LATCH

Dual Octal Latch

Preliminary Specification

FEATURES

- **High impedance NPN base inputs for reduced loadling (20μA in High and Low state)**
- **Stores 16-Bit-Wide data inputs, multiplexed 8-Bit outputs**
- **Propagation delay 7.5ns typical**
- **Power supply current 75mA typical**

DESCRIPTION

The 74F1604 is a Dual Octal Transparent Latch. Organized as 8-bit A and B latches, the latch outputs are connected by pairs to eight 2-input multiplexers. A Select (SELECT $A/\overline{B}$) input determines whether the A or B latch contents are multiplexed to the eight outputs. Data entered from the B inputs are selected when SELECT $A/\overline{B}$ is Low: data from the A inputs are selected when SELECT $A/\overline{B}$ is High. Data enters the latch on the falling edge of the Latch Enable ($\overline{LE}$) input. The Latch remains transparent to the data inputs while $\overline{LE}$ is Low, and stores the data that is present one setup time before the Low-to-High Latch Enable transition.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N74F1604	7.5 ns	75mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP	N74F1604N
28-Pin Plastic SOL	N74F1604D

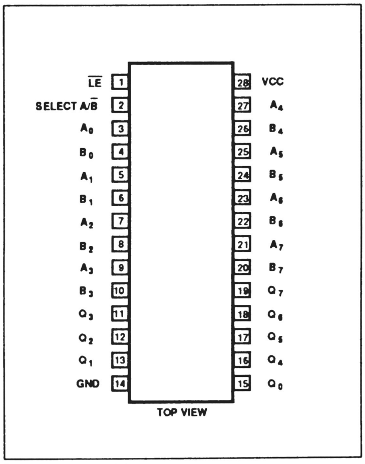
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_n, B_n	Data inputs	1.0/.033	20μA/20μA
SELECT $A/\overline{B}$	Select input	1.0/.033	20μA/20μA
$\overline{LE}$	Latch Enable input (Active Low)	1.0/.033	20μA/20μA
Q_0 - Q_7	Data outputs	50/33	1.0mA/20mA

NOTE:

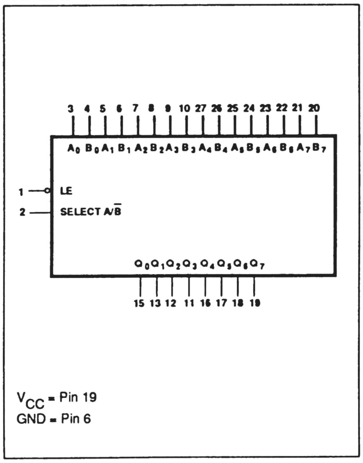
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



LE 1
SELECT A/B 2
A0 3
B0 4
A1 5
B1 6
A2 7
B2 8
A3 9
B3 10
Q3 11
Q2 12
Q1 13
GND 14
28 VCC
27 A4
26 B4
25 A5
24 B5
23 A6
22 B6
21 A7
20 B7
19 Q7
18 Q6
17 Q5
16 Q4
15 Q0
TOP VIEW

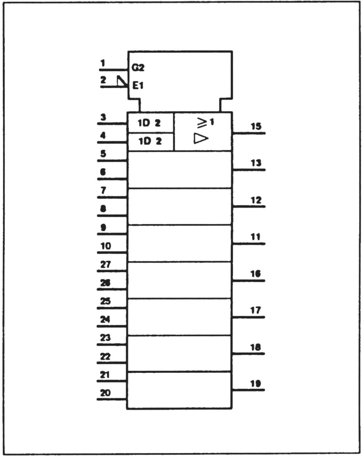
LOGIC SYMBOL



3 4 5 6 7 8 9 10 27 26 25 24 23 22 21 20
A0 B0 A1 B1 A2 B2 A3 B3 A4 B4 A5 B5 A6 B6 A7 B7
1 LE
2 SELECT A/B
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
15 13 12 11 16 17 18 19

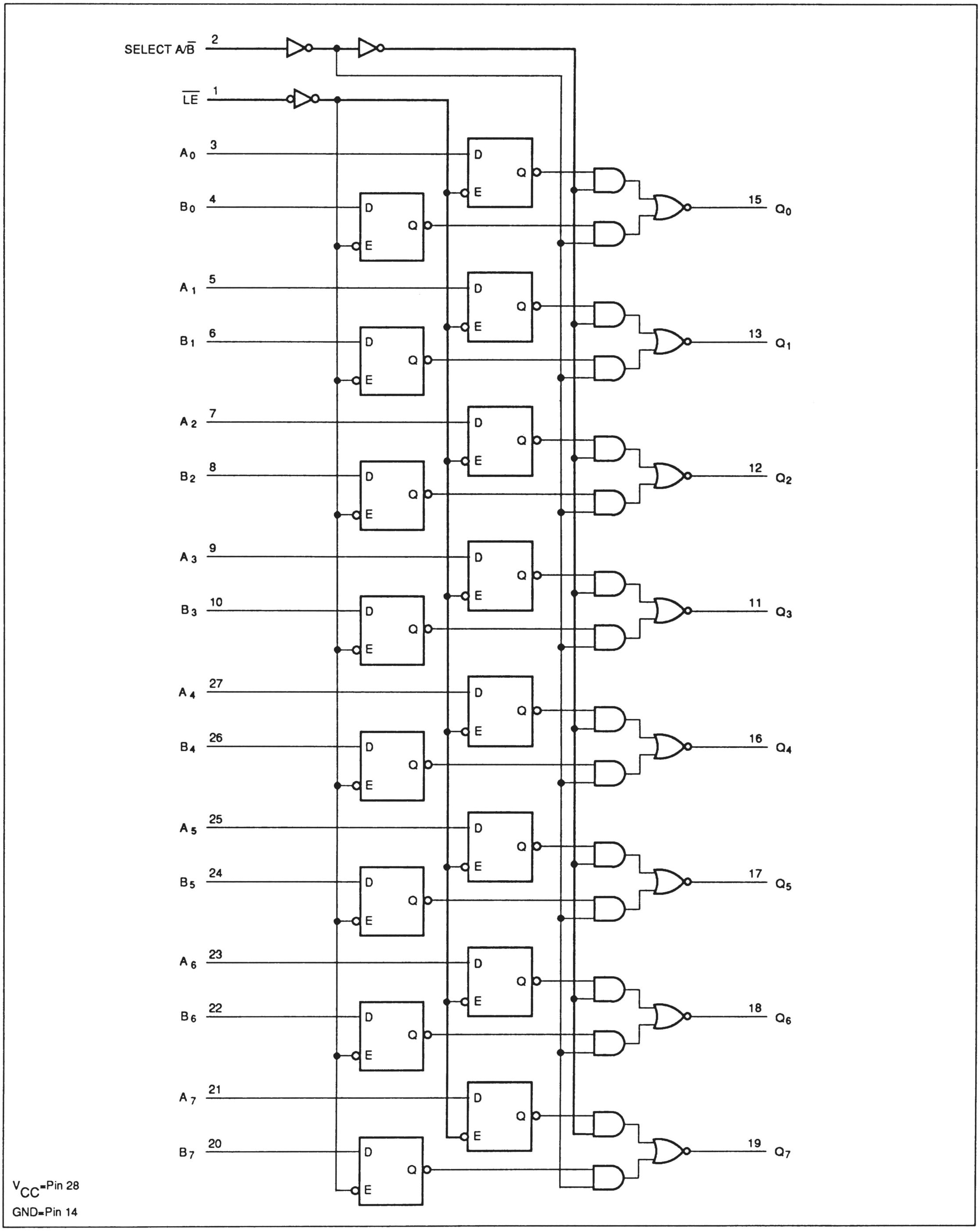
V_{CC} = Pin 19
GND = Pin 6

LOGIC SYMBOL(IEEE/IEC)



1 G2
2 E1
3
4
1D 2
1D 2
≥1
▷
15
5
6
13
7
8
12
9
10
11
27
26
16
25
24
17
23
22
18
21
20
19

LOGIC DIAGRAM


SELECT A/$\overline{B}$
2
$\overline{LE}$
1
A0
3
B0
4
A1
5
B1
6
A2
7
B2
8
A3
9
B3
10
A4
27
B4
26
A5
25
B5
24
A6
23
B6
22
A7
21
B7
20
D
Q
E
15
Q0
13
Q1
12
Q2
11
Q3
16
Q4
17
Q5
18
Q6
19
Q7
VCC=Pin 28
GND=Pin 14

FUNCTION TABLE

INPUTS				OUTPUTS	OPERATING MODE
A_0 - A_7	B_0 - B_7	SELECT $A/\overline{B}$	$\overline{LE}$	Q_0 - Q_7	
A data	B data	L	L	B data	Enable and Read Register
A data	B data	H	L	A data	
X	X	X	H	NC	Hold
A data	B data	l	↑	B data	Latch and Read Register
A data	B data	h	↑	A data	

H = High voltage level
h = High voltage level one setup time to the Low-to-High $\overline{LE}$ transition
L = Low voltage level
l = Low voltage level one setup time to the Low-to-High $\overline{LE}$ transition
NC = No change
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-1mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH}=-3mA	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
				±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 5.5V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX				60	82	mA
	I_{CCL}					75	100	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

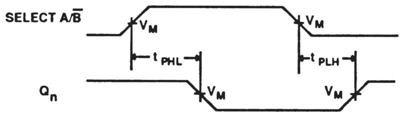
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay SELECT $A/\overline{B}$ to Q_n (B register)	Waveform 2	5.0 6.0	7.0 8.5	9.0 10.5	4.5 5.5	10.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay SELECT $A/\overline{B}$ to Q_n (A register)	Waveform 1	6.0 4.0	8.0 6.5	10.0 8.5	5.5 3.5	11.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to Q_n	Waveform 3	5.0 6.5	7.5 9.0	9.5 11.0	4.5 6.0	10.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to Q_n	Waveform 2	5.0 5.0	7.0 7.0	9.5 9.5	4.5 4.5	11.0 11.0	ns

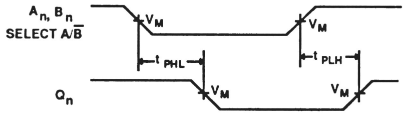
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n , B_n ,SELECT $A/\overline{B}$ to $\overline{LE}$	Waveform 4	1.0 2.0			2.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n , B_n ,SELECT $A/\overline{B}$ to $\overline{LE}$	Waveform 4	0 1.0			0 1.5		ns
$t_w(L)$	Pulse width, Low $\overline{LE}$	Waveform 4	5.0			6.0		ns

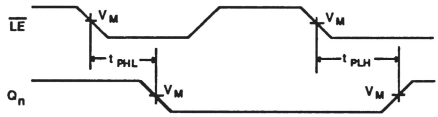
AC WAVEFORMS


SELECT A/B̄
VM
VM
tPHL
tPLH
Qn
VM
VM

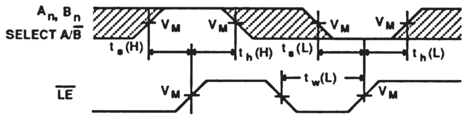
Waveform 1. Propagation delay, SELECT A/B̄ to Output (A register stored data = Low)


An, Bn
SELECT A/B̄
VM
VM
tPHL
tPLH
Qn
VM
VM

Waveform 2. Propagation delay, SELECT A/B̄ to Output (B register stored data = Low)


L̄Ē
VM
VM
tPHL
tPLH
Qn
VM
VM

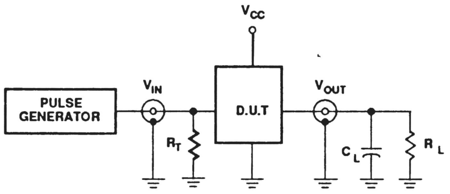
Waveform 3. Propagation delay, Latch Enable to Outputs


An, Bn
SELECT A/B̄
VM
VM
VM
VM
ts(H)
th(H)
ts(L)
th(L)
tw(L)
L̄Ē
VM
VM

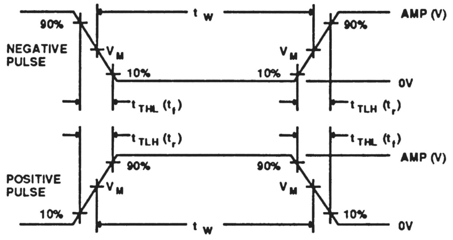
Waveform 4. Setup and Hold Times and L̄Ē pulse width

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
RT
D.U.T
VOUT
CL
RL

Test Circuit For Totem-Pole Outputs


tw
AMP (V)
90%
NEGATIVE PULSE
VM
10%
0V
tTHL (tf)
tTLH (tr)
tTLH (tr)
tTHL (tf)
AMP (V)
90%
POSITIVE PULSE
VM
10%
0V
tw

$V_M = 1.5V$
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F1761

DRAM and Interrupt Vector Controller

Preliminary Specification

November 1986

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1761	100 MHz	200 mA

FEATURES

- **Programmable DRAM signal timing generator**
- **Automatic refresh circuitry**
- **Provides byte selection for 16 and 32 bit buses**
- **Interrupt Priority Encoder included**
- **Interrupt Acknowledge vector generator on-chip**

DESCRIPTION

The Signetics DRAM and Interrupt Vector Controller (DIVC) is a high performance bipolar device designed to reduce board space and improve performance in micro-processor-based systems. The DIVC's functions include a DRAM signal interface with user programmable timing to match the performance of specific DRAMs used in a system. With a maximum clock frequency of 100 Mhz., this means a timing resolution of 10 nsec. The DRAM Controller section also includes automatic refresh arbitration, with the duration and frequency of refresh totally programmable by the user. When used with the 74F1762 Memory Address Controller, the DIVC provides a complete system solution for DRAM and Interrupt Control. For Interrupt Control, the DIVC contains an Interrupt Priority Decoder with latched inputs controlled by the Interrupt Latch Enable (ILE) input. In addition, the DIVC contains an Interrupt Acknowledge Controller which passes a program-mable 8-bit vector on the system data bus upon receipt of an interrupt acknowledge. There are 7 interrupt acknowledge vectors, each accessable by placing the priority number of the interrupt acknowledge on the A1-A3 signal inputs while acknowledging an interrupt.

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; T_A=0°C to 70°C
Plastic DIP	N74F1761N
PLCC 44	N74F1761A

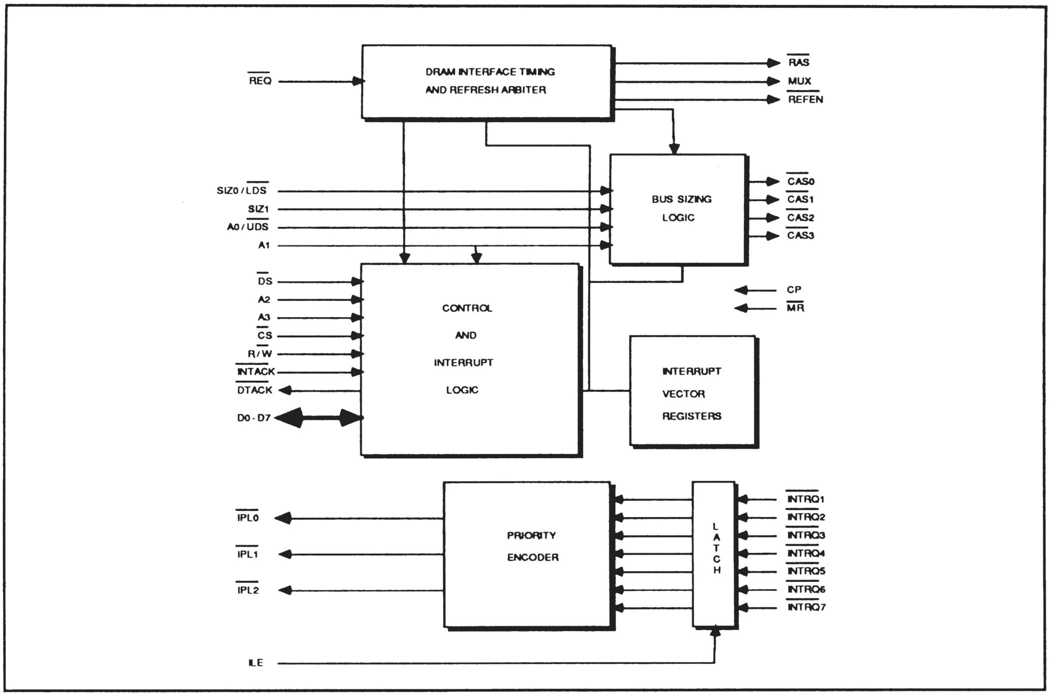
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

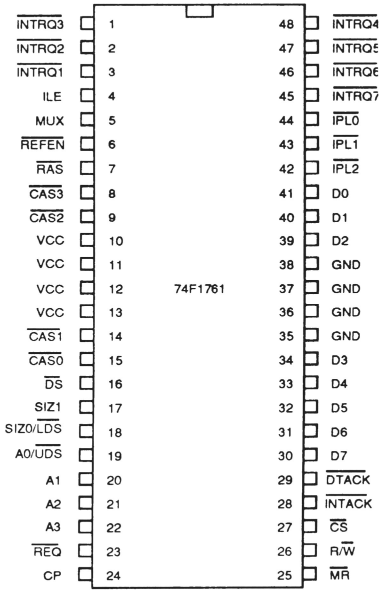
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{\text{REQ}}$	DRAM Request Input	1.0/1.0	20 uA/0.6 mA
SIZ0/$\overline{\text{LDS}}$,SIZ1, A0/$\overline{\text{UDS}}$,A1	Byte Select Inputs	1.0/1.0	20 uA/0.6 mA
A2,A3	Register Select Inputs	1.0/1.0	20 uA/0.6 mA
$\overline{\text{CS}}$,$\overline{\text{DS}}$	Chip Select, Data Strobe	1.0/1.0	20 uA/0.6 mA
R/$\overline{\text{W}}$	Read/Write Input	1.0/1.0	20 uA/0.6 mA
$\overline{\text{INTACK}}$	Interrupt Acknowledge Input	1.0/1.0	20 uA/0.6 mA
ILE	Interrupt Latch Enable Input	1.0/1.0	20 uA/0.6 mA
CP	Clock Input	1.0/1.0	20 uA/0.6 mA
$\overline{\text{MR}}$	Master Reset Input	1.0/1.0	20 uA/0.6 mA
$\overline{\text{INTRQ1-7}}$	Interrupt Request Inputs	1.0/1.0	20 uA/0.6 mA
$\overline{\text{DTACK}}$	Data Transfer Ack. Output	(O.C.) 80	24 mA
D0-D7	Data Bus	50/80 (1.0/1.0)	1.0 mA/24 mA
$\overline{\text{IPL0-2}}$	Interrupt Priority Outputs	50/80	1.0 mA/24 mA
$\overline{\text{RAS}}$,MUX, $\overline{\text{REFEN}}$,$\overline{\text{CAS0-3}}$	DRAM Control Outputs	1750/100	35 mA/60 mA

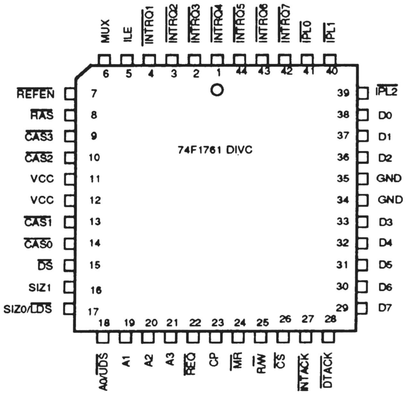
NOTE:
One (1.0) FAST Unit Load is defined as 20 uA in the HIGH state and 0.6 mA in the LOW state.

BLOCK DIAGRAM


REQ
DRAM INTERFACE TIMING AND REFRESH ARBITER
RAS
MUX
REFEN
SIZ0/LDS
SIZ1
A0/UDS
A1
BUS SIZING LOGIC
CAS0
CAS1
CAS2
CAS3
CP
MR
DS
A2
A3
CS
R/W
INTACK
DTACK
D0 - D7
CONTROL AND INTERRUPT LOGIC
INTERRUPT VECTOR REGISTERS
IPL0
IPL1
IPL2
PRIORITY ENCODER
LATCH
INTRQ1
INTRQ2
INTRQ3
INTRQ4
INTRQ5
INTRQ6
INTRQ7
ILE

PIN CONFIGURATION


74F1761
1 INTRQ3
2 INTRQ2
3 INTRQ1
4 ILE
5 MUX
6 REFEN
7 RAS
8 CAS3
9 CAS2
10 VCC
11 VCC
12 VCC
13 VCC
14 CAS1
15 CAS0
16 DS
17 SIZ1
18 SIZ0/LDS
19 A0/UDS
20 A1
21 A2
22 A3
23 REQ
24 CP
48 INTRQ4
47 INTRQ5
46 INTRQ6
45 INTRQ7
44 IPL0
43 IPL1
42 IPL2
41 D0
40 D1
39 D2
38 GND
37 GND
36 GND
35 GND
34 D3
33 D4
32 D5
31 D6
30 D7
29 DTACK
28 INTACK
27 CS
26 R/W
25 MR


74F1761 DIVC
6 MUX
5 ILE
4 INTRQ1
3 INTRQ2
2 INTRQ3
1 INTRQ4
44 INTRQ5
43 INTRQ6
42 INTRQ7
41 IPL0
40 IPL1
7 REFEN
8 RAS
9 CAS3
10 CAS2
11 VCC
12 VCC
13 CAS1
14 CAS0
15 DS
16 SIZ1
17 SIZ0/LDS
39 IPL2
38 D0
37 D1
36 D2
35 GND
34 GND
33 D3
32 D4
31 D5
30 D6
29 D7
18 A0/UDS
19 A1
20 A2
21 A3
22 REQ
23 CP
24 MR
25 R/W
26 CS
27 INTACK
28 DTACK

NOTE: Pinout assignments are strictly preliminary and are subject to change.

PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
$\overline{\text{DS}}$	2	2	I	Active LOW Data Strobe used to enable the Data Bus during register access cycles and the CAS outputs during DRAM access cycles.
SIZ0/$\overline{\text{LDS}}$	3	3	I	In 16-bit Mode, an active LOW Lower Data Strobe signal used to enable the $\overline{\text{CAS1}}$ output during a DRAM access cycle. In 32-bit Mode, an active HIGH SIZE 0 signal used with SIZ1 to indicate to the DIVC the size of the DRAM access transaction.
SIZ1	4	4	I	In 32-bit Mode, an active HIGH SIZE 1 signal used with SIZ0 to indicate to the DIVC the size of the DRAM access transaction.
A0/$\overline{\text{UDS}}$	5	5	I	In 16-bit Mode, an active LOW Upper Data Strobe used to enable the $\overline{\text{CAS0}}$ output during a DRAM access cycle. In 32-bit Mode, used with A1 to indicate to the DIVC the byte boundary of the DRAM access transaction.
A1	6	6	I	During DIVC register access, forms the least significant address bit of the register address. During DRAM access and in 32-bit Mode, used with A0 to indicate to the DIVC the byte boundary of the DRAM access transaction.
A2,A3	7,8	7,8	I	During DIVC register access, forms the most significant two address bits of the register address.
$\overline{\text{REQ}}$	1	1	I	Active LOW DRAM Access Request indicating to the DIVC that the processor wishes to access the DRAM controlled by the DIVC.
$\overline{\text{CS}}$	9	9	I	Active LOW Chip Select used for Register Access with the DIVC.
R/$\overline{\text{W}}$	10	10	I	Read/Write signal used to indicate the direction of register access with the DIVC.
V_{CC}	11,12 13,14	11,12		Power Supply +5V ± 10%
$\overline{\text{INTACK}}$	15	13	I	Active LOW Interrupt Acknowledge signal used with the A1,A2, and A3 inputs to assert the contents of one of seven internal Interrupt Vector Registers on the data bus (D0-D7).
$\overline{\text{DTACK}}$	16	14	O	Active LOW Data Transfer Acknowledge. Indicates to the processor the completion of a DIVC register or DRAM access cycle. For DRAM access, this signal's timing is programmable internally. Open Collector Output.
D0-D7	17-24	15-22	I/O	Active HIGH Tri-StateData Bus over which data is transferred between the processor and internal registers of the DIVC.
$\overline{\text{IPL0}}$ $\overline{\text{IPL1}}$ $\overline{\text{IPL2}}$	34 33 32	32 31 30	O O O	Active LOW Interrupt Priority Level signals indicating to the processor the priority level of the highest latched interrupt request on the INTRQ1-7 inputs. A level of all ONES indicates no interrupt rrequest pending.
ILE	39	35	I	Active HIGH Interrupt Latch Enable which causes the internal latches connected to the INTRQ1-7 inputs to become transparent. A HIGH-to-LOW transition causes the INTRQ1-7 signals to be internally latched.

PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
$\overline{\text{INTRQ1-7}}$	31-25	29-23	I	Active LOW Interrupt Request inputs.
CP	40	36	I	DIVC Clock Input
$\overline{\text{MR}}$	41	37	I	Active LOW Master Reset input.
$\overline{\text{CAS0-3}}$	45-42	41-38	O	Active LOW Column Address Strobe outputs.
$\overline{\text{REFEN}}$	46	42	O	Active LOW Refresh Enable Output. Indicates that the refresh address should be asserted.
MUX	47	43	O	Active HIGH Multiplexer output. Indicates that the Column address should be asserted to the DRAMs.
$\overline{\text{RAS}}$	48	44	O	Active LOW Row Address Strobe output.
GND	35-38	33-34		Ground Reference.

FUNCTIONAL DESCRIPTION

Figure 1 shows the overall architecture of the 74F1761. The DRAM Interface Timing section produces the RAS, MUX, CAS, DTACK and Refresh Enable (REFEN) signals in response to the Request (REQ) input. The timing of these signals is configurable by programming a register set within the F1761 (see **REGISTER DESCRIPTION**). The timing section also includes a refresh arbiter that allows for refreshing the DRAM at a frequency programmable by the user. While a refresh cycle is being executed, the REFEN output is asserted, allowing a companion memory address generator (such as the 74F1762 Memory Address Controller) to assert a refresh row address on the DRAM address inputs.

The Bus Sizing Logic section is a configurable decoder that allows for multiple CAS outputs depending on the state of the DS, SIZ0/LDS, SIZ1, A0/UDS, and A1 signal inputs, and the selected bus size scheme (See **Table 4. CAS DECODING SUMMARY**). By programming the Configuration Register, the F1761 can respond to a variety of 8, 16, and 32 Bit Processor signal outputs. In the 8-bit mode, the F1761 will assert one of four CAS outputs depending on the state of the A0 and A1 inputs during the CAS signal assertio time determined by the timing logic. In the 16-bit mode, the F1761 will assert CAS0 and/or CAS1 depending on the state of the UDS and LDS inputs, respectively. In the 32 Bit mode, the A1, A0, SIZ1 and SIZ0 determine the CAS outputs to be asserted according to the 68020 byte-selection scheme.

The Control and Interrupt Logic section determines the response of the F1761 in one of two modes. The internal registers of the device can be accessed by asserting the CS and DS inputs while placing the address of the register to be accessed on the A1,A2, and A3 inputs. The R/W input indicates to the F1761 the direction of data transfer when accessing a particular register. In addition, the configuration register contains one bit of register addressing that is initialized to 0. The lower order registers contain the timing information for the DRAM interface, while the upper order registers contain the Interrupt Vectors to be passed during an interrupt acknowledge. All internal registers are read/write, with unused bits being read as zeros and ignored during write cycles. In the Interrupt Acknowledge mode, the INTACK input signals the F1761 that an interrupt acknowledge is occuring. The F1761 responds by placing the contents of one of seven vector registers on the data outputs, according to the value of the A1,A2, and A3 signal inputs. For both Register Access and Interrupt Acknowledge modes, the device will assert DTACK to indicate the completion of the cycle. This DTACK signal is also asserted by the DRAM timing logic in response to a Request from the processor, with its timing programmed by the user.

The F1761 also includes an 8 to 3 bit Interrupt Priority Encoder which can be used to interface with the 68000 family of processors, with the Interrupt inputs (INTRQ1 - INTRQ7) latched on the falling edge of the Interrupt Latch Enable (ILE) input. The ILE input can be connected to the processor clock for glitch-free interrupting.

All of the DRAM interface timing is based upon the Master Clock (CP) input. Numerical values programmed into the Timing Registers indicate the number of clock cycles between events. When a 0 value is programmed into a timing skew, the two events indicated will happen simultaneously. The AC specifications indicate the amount of timing variation due to propogation delays within the device. The Master Reset input (MR) initializes all timing registers to their maximum delay (All ones) and clears the Configuration Register.

TABLE 2. DIVC Register Selection Map

RSS[1]	A3	A2	A1	ACRONYM	REGISTER NAME	MODE	AFFECTED BY RESET
X	0	0	0	CR	Configuration Register	R/W	Yes
0	0	0	1	RTR	Refresh Timing Register	R/W	Yes
0	0	1	0	TR2	Timing Register 2	R/W	Yes
0	0	1	1	TR3	Timing Register 3	R/W	Yes
0	1	0	0	TR4	Timing Register 4	R/W	Yes
0	1	0	1	TR5	Timing Register 5	R/W	Yes
0	1	1	0	-----	Reserved	-----	-----
0	1	1	1	-----	Reserved	-----	-----
1	0	0	1	VR1	Vector Register 1	R/W	No
1	0	1	0	VR2	Vector Register 2	R/W	No
1	0	1	1	VR3	Vector Register 3	R/W	No
1	1	0	0	VR4	Vector Register 4	R/W	No
1	1	0	1	VR5	Vector Register 5	R/W	No
1	1	1	0	VR6	Vector Register 6	R/W	No
1	1	1	1	VR7	Vector Register 7	R/W	No

Note 1: RSS = Register Set Select Bit in the Configuration Register

REGISTER DESCRIPTION

Register Map

The DIVC contains a set of registers which can be programmed by a controlling processor to configure the DIVC for different bus sizes, DRAM timing, and Interrupt Vectors. Table 2 shows the Register Map of the DIVC. Note that the higher-order bit of the register address (RSS) is contained in the Configuration Register. Access to the Configuration Register is independent of the value of the RSS bit. By toggling the RSS bit, two sets of registers can be accessed. Those registers accessed with RSS = 0 are the DRAM timing registers for programming events during DRAM access. With RSS = 1, the seven Interrupt Vector registers can be accessed.

Configuration Register (CR)

This register configures the mode of access and register set select for the DIVC. **Bits 7 and 6** are used to specify the size of the bus to be used with the DRAM controlled by the DIVC. In the 8-bit mode, the Column Address Strobe outputs will respond to CAS signal assertion from the Timing Block by asserting one of the CAS outputs depending on the state of the A0 and A1 inputs, in binary fashion (i.e. If A0=A1=0 then CAS0=0; if A0=0 and A1=1 then CAS2=0). In 16-bit mode, the DIVC responds to a CAS assertion from the Timing Block by asserting CAS0 and CAS1 depending on the state of the UDS and LDS inputs, respectively. In 32-bit mode, the SIZ0, SIZ1, A0, and A1 inputs determine the state of the CAS outputs according to the decoding used with the 68020 Microprocessor, with CAS0 corresponding to the most significant byte and CAS3 corresponding to the least significant byte of the 32-bit bus. **Bit 5** is used as a register set select (RSS) for accessing the other registers in the DIVC. When RSS is low, registers 1 through 5 correspond to the Refresh Timing Register and Timing Registers 2 through 5. With RSS high, registers 1 through 7 correspond to Vector Registers 1 through 7. **Bit 4** is used to disable the refreshing operation of the DRAM Controller section of the DIVC. When set, no refreshes will be performed and internally generated Refresh Requests will be ignored, regardless of the state of the refresh timing parameters. Other bits in the Configuration Register are ignored on write cycles and are read as zeros on read cycles. All implemented bits of this register are reset to zeros when the DIVC is reset.

Refresh Timing Register (RTR)

The value in this register is used with a reloadable counter within the DIVC to generate refresh requests. Each time the counter counts down (using the CP clock divided by sixteen), a refresh request will be generated inside the DIVC. If no DRAM access is taking place, the DIVC immediately performs a refresh cycle, using the REFRESH RASON to RASOFF delay programmed into Timing Register 2, and the RASOFF to REFRESHOFF delay programmed into Timing Register 3. If a DRAM access cycle has already begun, the DIVC will wait until the completion of the DRAM access cycle, after which it will perform the refresh cycle as explained. A value of all zeros will program the DIVC with the shortest possible delay between refresh requests: 16 CP clock cycles. At 100 Mhz., this register gives a refresh period resolution of 160 nsec. Resetting the DIVC changes all bits to ones.

Timing Register 2 (TR2)

Bits 0 to 4 of this register program the RAS pulse width of a refresh cycle in CP clock cycles. Although a value of zero would normally result in no RAS pulse during a refresh cycle, internal propagation delays cause a small RAS pulse to be output. Resetting the DIVC will result in all these bits being set to ones. **Bits 5 to 7** are ignored during write cycles and read as zeros during read cycles.

Timing Register 3 (TR3)

Bits 0 to 3 of this register program the delay between RAS negated and the end of a refresh cycle. Because an access cycle could begin immediately after the

Table 3. REGISTER BIT FORMATS

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	BUS SIZING		**RSS**	**RD**	**UNIMPLEMENTED**			
CR	00 = 8 Bit Mode 01 = 16 Bit Mode 10 = 32 Bit Mode 11 = Invalid		See Text	Refresh Disable				

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	REFRESH TIMING COUNTER VALUE							
RTR	Refresh Period in CP/16 Cycles							

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	UNIMPLEMENTED			**REFRESH RAS PULSE WIDTH**				
TR2				CP Cycles				

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	UNIMPLEMENTED			**REFRESH RAS OFF TO REFRESH OFF**				
TR3				CP Cycles - 1				

refresh, some delay may be desired between RASOFF and the end of the refresh cycle to accomodate RAS precharge requirements of the DRAMs. The value programmed into these bits should be one less than the number of clock cycle delays desired. Resetting the DIVC will result in these bits being set to ones. **Bits 4 to 7** are ignored during write cycles and read as zeros during read cycles.

Timing Register 4 (TR4)

Bits 5-7 of this register program the DIVC with the ACCESS GRANT TO RAS delay of a DRAM access cycle in CP clock cycles. Since the REFEN output is asserted during a refresh cycle, it is commonly used as a select signal for address multiplexers that select between a processor address and the refresh row address. If, on the completion of a refresh cycle, the DIVC immediately performs an access cycle, there may be a need to wait until the processor's row address has become stable at the DRAMs, before asserting RAS. (Since the REFEN output is negated at the same time as the refresh RAS output, and there is a programmable delay between RASOFF and REFRESHOFF, the problem is associated with the application. See explanation of bits 3-7 in Timing Register 3) These bits can be programmed with the number of clock cycles to wait from the time that an access is granted until RAS is asserted. A value of zero will result in no delay between events. **Bits 3 and 4** configure the timing between RAS and the MUX output asserted in CP clock cycles. A value of zero in these bits will cause no delay between RAS and MUX. **Bits 0 to 2** configure the timing between MUX asserted and CAS asserted in CP clock cycles. A value of zero in these bits will cause no delay between MUX and CAS. Resetting the DIVC sets all bits of this register to ones.

Timing Register 5 (TR5)

Bits 5 to 7 of this register program the delay between the assertion of CAS and the negation of RAS, in CP clock cycles. A value of zero in these bits results in no delay between these events. **Bits 0 to 4** program the delay beween the assertion of RAS and the assertion of DTACK back to the processor over the chip's DTACK signal pin. A value of zero in these bits results in no delay between these events. Resetting the DIVC will result in all bits of this register being set to ones.

Interrupt Vector Registers 1 to 7 (VR1-7)

Each of these registers can be programmed to contain the 8-bit vector to be placed on the DIVC's data bus during an Interrupt Acknowledge cycle. When the processor asserts the INTACK and DS inputs and places the Interrupt Priority on the A1, A2, and A3 inputs, the DIVC will respond by placing the contents of the Interrupt Vector Register addressed by these address inputs on the data bus and asserting DTACK. In this way, peripheral devices which do not contain the interrupt acknowledging circuitry can be used with a processor which expects these kinds of acknowledge cycles to occur. Resetting the DIVC does not affect the contents of these registers.

TABLE 3. REGISTER BIT FORMATS (Continued)

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	GRANT TO RAS DELAY			RAS TO MUX DELAY		MUX TO CAS DELAY		
TR4	CP Cycles			CP Cycles		CP Cycles		

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	CAS TO RAS OFF DELAY			RAS TO DTACK DELAY				
TR5	CP Cycles			CP Cycles				

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	INTERRUPT VECTOR VALUE							
VR1-VR7								

TABLE 4. CAS DECODING SUMMARY

MODE	SIZ0/$\overline{\text{LDS}}$	SIZ1	A0/$\overline{\text{UDS}}$	A1	$\overline{\text{CAS0}}$	$\overline{\text{CAS1}}$	$\overline{\text{CAS2}}$	$\overline{\text{CAS3}}$
8	X	X	0	0	0	1	1	1
8	X	X	1	0	1	0	1	1
8	X	X	0	1	1	1	0	1
8	X	X	1	1	1	1	1	0
16	1	X	1	X	1	1	1	1
16	1	X	0	X	0	1	1	1
16	0	X	1	X	1	0	1	1
16	0	X	0	X	0	0	1	1
32	1	0	0	0	0	1	1	1
32	1	0	1	0	1	0	1	1
32	1	0	0	1	1	1	0	1
32	1	0	1	1	1	1	1	0
32	0	1	0	0	0	0	1	1
32	0	1	1	0	1	0	0	1
32	0	1	0	1	1	1	0	0
32	0	1	1	1	1	1	1	0
32	1	1	0	0	0	0	0	1
32	1	1	1	0	1	0	0	0
32	1	1	0	1	1	1	0	0
32	1	1	1	1	1	1	1	0
32	0	0	0	0	0	0	0	0
32	0	0	1	0	1	0	0	0
32	0	0	0	1	1	1	0	0
32	0	0	1	1	1	1	1	0

NOTE: This table gives the functional decoding of the CAS output signals of the DIVC when DS is valid and the DRAM timing circuitry asserts CAS.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
VCC	Supply Voltage	-0.5 to +7.0	V
V_{IN}	Input Voltage	-0.5 to +7.0	V
I_{IN}	Input Current	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in LOW output state	120	mA
T_A	Operating free-air temperature range	0 to 70	° C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				+0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	HIGH-level output current				-35	mA
I_{OL}	LOW-level output current	Buffer			60	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			74F1761			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -15mA	±10% V_{CC}	2.5	3.2		V
				±5% V_{CC}	2.7	3.4		V
			I_{OH2} = -35 mA	±10% V_{CC}	2.4			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24 mA	±10% V_{CC}		0.35	0.50	V
				±5% V_{CC}		0.35	0.50	V
			I_{OL2} = 60 mA	±10% V_{CC}		0.45	0.80	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Short circuit output current	V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	V_{CC} = MAX				200	220	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at Vcc = 5V, T_A = 25°C.
3. I_{OH2} is the current necessary to guarantee a LOW to HIGH transition in a 70Ω transmission line and is specified for the RAS, CAS0-3, MUX, and REFEN signals.
4. I_{OL2} is the current necessary to guarantee a HIGH to LOW transition in a 70Ω transmission line and is specified for the RAS, CAS0-3, MUX, and REFEN signals.

AC ELECTRICAL CHARACTERISTICS

(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

	PARAMETER	74F1761					UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 300pF$, $R_L = 70\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 300pF$, $R_L = 70\Omega$		
		Min	Typ	Max	Min	Max	
1	CP Period	10	9		10		ns
2	CP LOW time	5	4		5		ns
3	CP HIGH time	5	4		5		ns
4	MR Pulse Width	20	15		20		ns
5	CS Pulse Width	50	40		50		ns
6	A1-A3 setup to CS asserted	5	3		5		ns
7	CS negated to A1-A3 negated	3	2		3		ns
8	R/W setup to CS asserted	5	3		5		ns
9	CS negated to R/W invalid	3	2		3		ns
10[1]	CS or DS to Data Out (Read)		5	8		10	ns
11[1]	CS or DS negated to Data Out invalid (Read)		8	10		12	ns
12[4]	CS to DTACK asserted		4	5		6	ns
13[4]	CS negated to DTACK negated		4	5		6	ns
14	DS Pulse Width	30	25		30		ns
15	Data In valid to DS negated (Write)	0	0		0		ns
16	DS negated to Data In invalid (Write)	5	3		5		ns
17	INTACK Pulse Width	30	25		30		ns
18	A1-A3 setup to INTACK asserted	5	3		5		ns
19	INTACK negated to A1-A3 invalid	3	2		3		ns
20[1]	INTACK or DS to Data Out		5	8		10	ns
21[1]	INTACK or DS negated to Data Out invalid		8	10		10	ns
22[4]	INTACK asserted to DTACK asserted		4	6		7	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	74F1761					UNIT
	T_A = +25°C V_{CC} = +5.0V C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ±10% C_L = 300pF, R_L = 70Ω		
	Min	Typ	Max	Min	Max	
23[4] INTACK negated to DTACK negated	4	5		6	ns	
24 REQ setup to CP	2	1.2		2		ns
25[2] Worst case REQ to RAS with 000 in TR4			8+T_{cp}		11+T_{cp}	ns
26 CP to RAS asserted		6	9 (7)[3]		11 (9)	ns
27 CP to RAS negated		10	14 (12)		16 (14)	ns
28[1] CP to MUX asserted		7	8 (10)		10 (12)	ns
29[1] REQ negated to MUX negated		5	6		8	ns
30 CP to CAS asserted		9	12 (14)		14 (16)	ns
31 REQ negated to CAS negated		8	10		12	ns
32 SIZ0, SIZ1, A0, A1 setup to CAS asserted	8	6		10		ns
33 SIZ0, SIZ1, A0, A1 invalid to CAS negated		6	8		10	ns
34[4] CP to DTACK asserted		7	9 (11)		11 (13)	ns
35[4] REQ negated to DTACK negated		5	7		9	ns
36[1] CP to REFEN asserted		4	5		6	ns
37 CP to Refresh RAS asserted		5	6		7	ns
38 CP to Refresh RAS negated		5	11		13	ns
39[1] CP to REFEN negated		5	10		12	ns
40 INTRQ setup to ILE negated	4	3		4		ns
41 INTRQ hold from ILE negated	0	0		0		ns
42 ILE Pulse Width	17	15		20		ns
43[1] INTRQ asserted to IPL asserted		7	10		12	ns

NOTES

1: For these signals, refer to Test Circuit #2

2: Worst case REQ to RAS assumes that REQ did not meet setup time requirements on the last rising edge of CP, that 000 was programmed into the GRANT to RAS delay in TR4, and that no refresh request is pending or being executed. T_{cp} is AC parameter number 1.

3: Numbers in parentheses indicate propogation delay with 0 programmed into the appropriate delay field.

4: For DTACK test load, refer to Test Circuit #3.

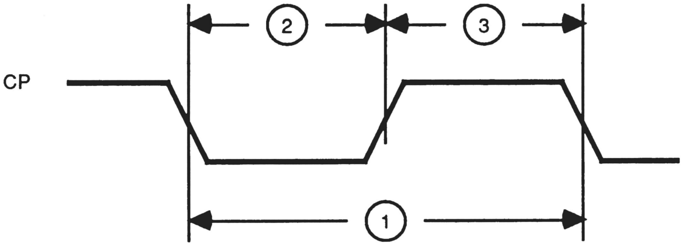


Figure 1. CP Timing

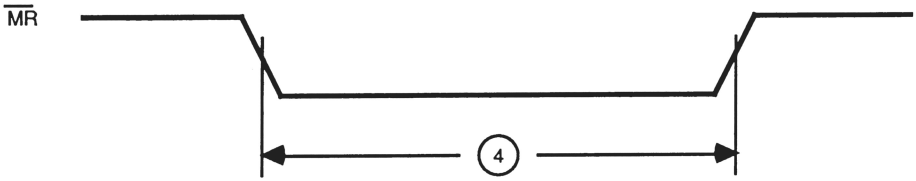
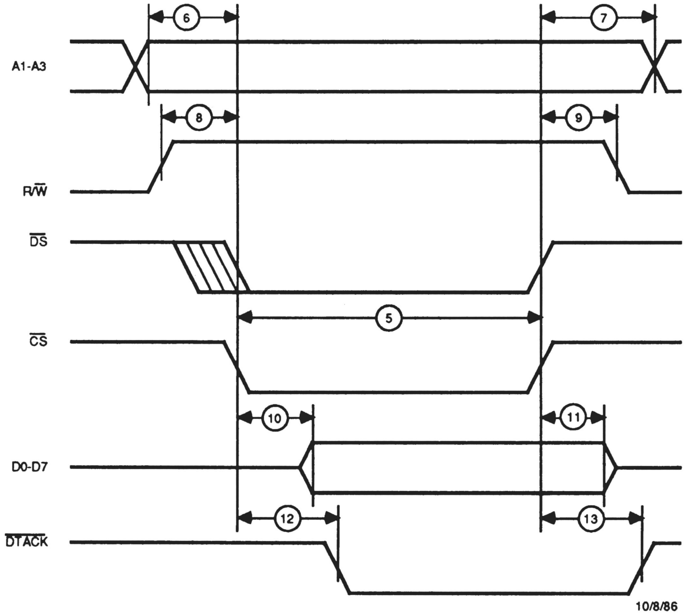
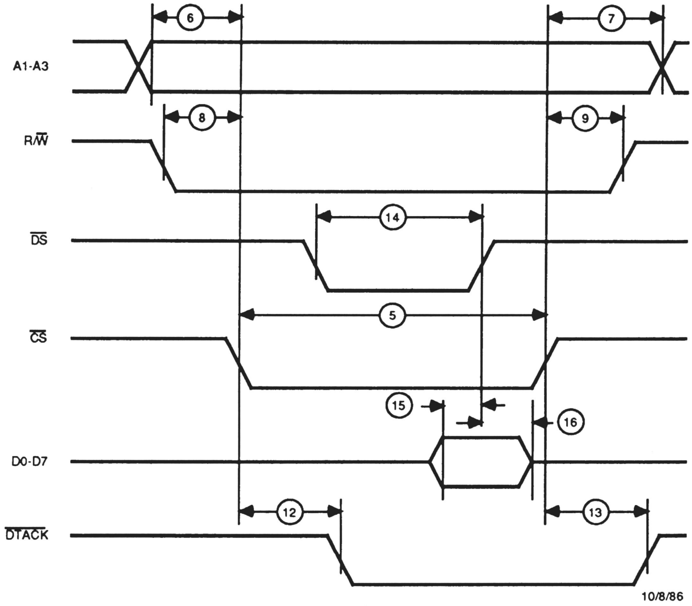

$\overline{MR}$
④

Figure 2. MR Timing



6
7
A1-A3
8
9
R/W̄
D̄S̄
5
C̄S̄
10
11
D0-D7
12
13
D̄T̄ĀC̄K̄
10/8/86

Figure 3. Bus Timing (Read Cycle)



6
7
A1-A3
8
9
R/W̄
14
D̄S̄
5
C̄S̄
15
16
D0-D7
12
13
D̄T̄ĀC̄K̄
10/8/86

Figure 4. Bus Timing (Write Cycle)

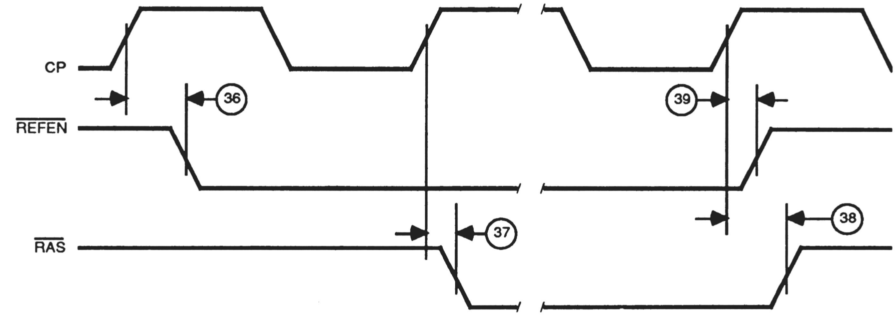

CP
REFEN
RAS
36
37
38
39

Figure 5. Refresh Timing

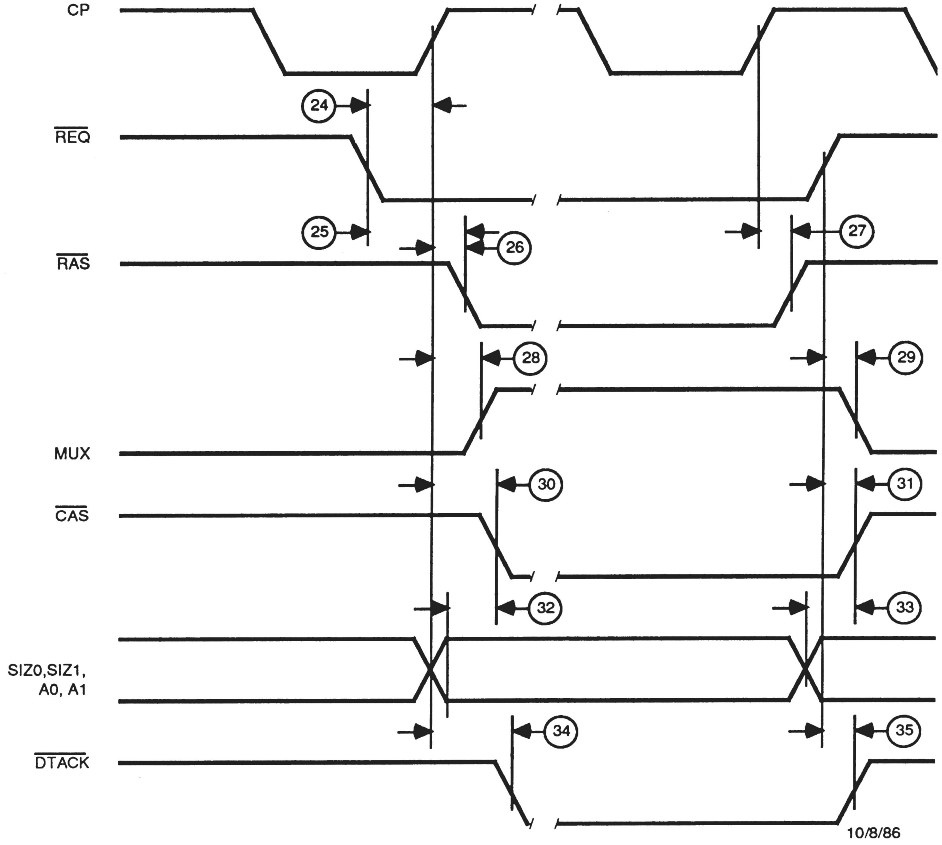

CP
REQ
RAS
MUX
CAS
SIZ0,SIZ1,
A0, A1
DTACK
24
25
26
27
28
29
30
31
32
33
34
35
10/8/86

Figure 6. DRAM Access Timing

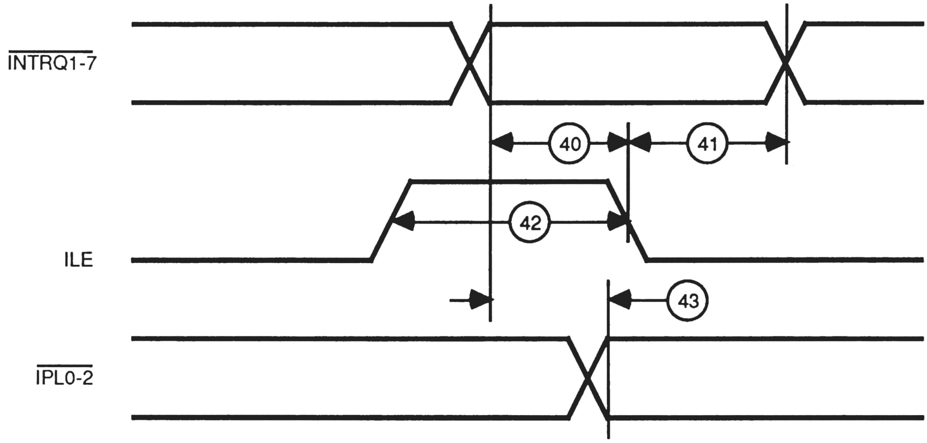

INTRQ1-7
40
41
42
ILE
43
IPL0-2

Figure 7. Interrupt Request Timing

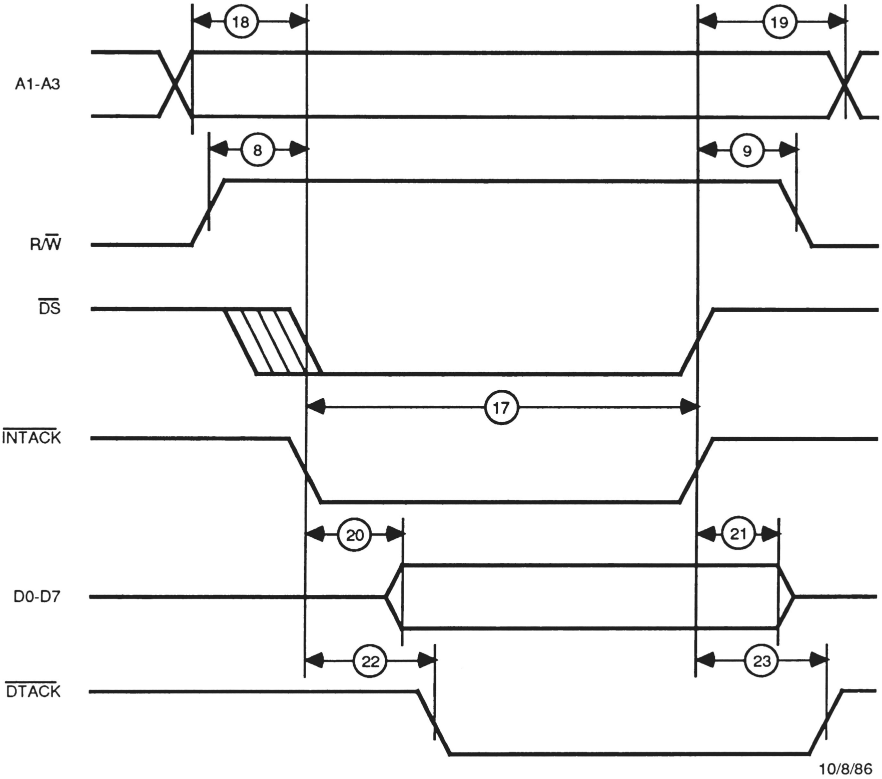
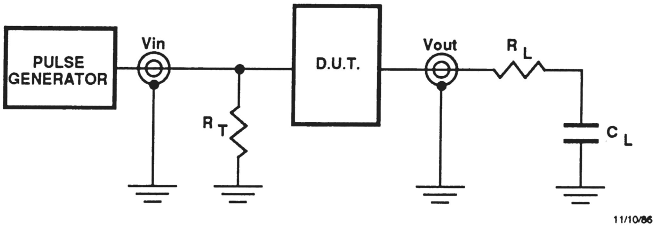

18
19
A1-A3
8
9
R/W
DS
17
INTACK
20
21
D0-D7
22
23
DTACK
10/8/86

Figure 8. Interrupt Acknowledge Timing

TEST CIRCUITS AND WAVEFORMS

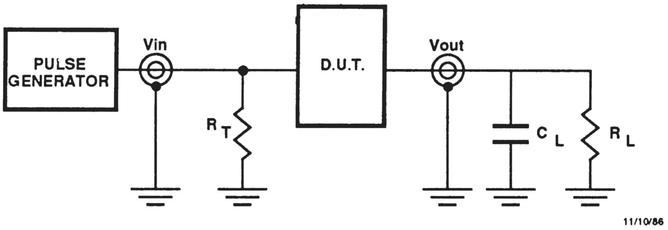
Test Circuit #1:

Used for RAS, CAS signals
$R_L = 70\ \Omega$
$C_L = 300$ pF
$R_T = Z_{OUT}$ of pulse generator


PULSE GENERATOR
Vin
R T
D.U.T.
Vout
R L
C L
11/10/86

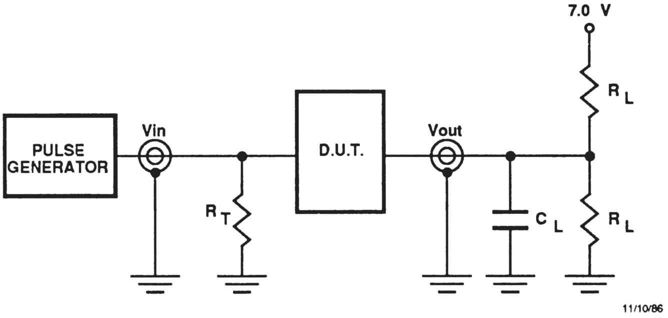
Test Circuit #2:

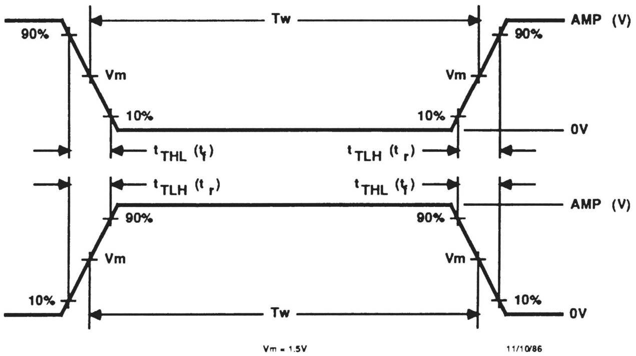
Used for microprocessor interface signals
$R_L = 500\ \Omega$
$C_L = 50$ pF
$R_T = Z_{OUT}$ of pulse generator


PULSE GENERATOR
Vin
R T
D.U.T.
Vout
C L
R L
11/10/86

Test Circuit #3:

Used for DTACK signal
$R_L = 500\ \Omega$
$C_L = 50$ pF
$R_T = Z_{OUT}$ of pulse generator


7.0 V
R L
PULSE GENERATOR
Vin
R T
D.U.T.
Vout
C L
R L
11/10/86


Tw
AMP (V)
90%
90%
Vm
Vm
10%
10%
0V
tTHL (tf)
tTLH (tr)
tTLH (tr)
tTHL (tf)
AMP (V)
90%
90%
Vm
Vm
10%
10%
Tw
0V
Vm = 1.5V
11/10/86

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F1762

Memory Address Multiplexer

Product Specification

FEATURES

- **Provides refresh and multiplexed row and column addresses for DRAMs**
- **Addressing up to 4MBit DRAMs**
- **Compatible with 74F1761 DIVC and other DRAM controllers**
- **High-performance outputs**
- **High-speed address multiplexing**
- **On-chip 11-bit refresh counter**

PRODUCT DESCRIPTION:

The Signetics Memory Address Multiplexer is designed for use in very high performance dynamic RAM applications. In addition to multiplexing row and column addresses, the device also generates and multiplexes refresh addresses. Though specifically designed to be used with the 74F1761, DRAM and Interrupt Vector Controller, it may be used with any other custom or standard DRAM timing controller chip.

The 'F1762 contains 22 address inputs (RA_0 - RA_{10}) and (CA_0 - CA_{10}), an 11-bit refresh counter, and eleven 3-to-1 multiplexers. The multiplexed row, column or refresh address is output on the eleven high-performance outputs ($\overline{MA}_0$ - $\overline{MA}_{10}$). This enables direct addressing of up to 4MBit dynamic RAMs. Combined with the 'F1761, the 'F1762 provides a complete 4MBit DRAM and interrupt control solution. This solution can control dynamic RAMs with access times down to 40ns.

TYPE	TYPICAL DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N74F1762	5.3ns	90mA

ORDERING INFORMATION

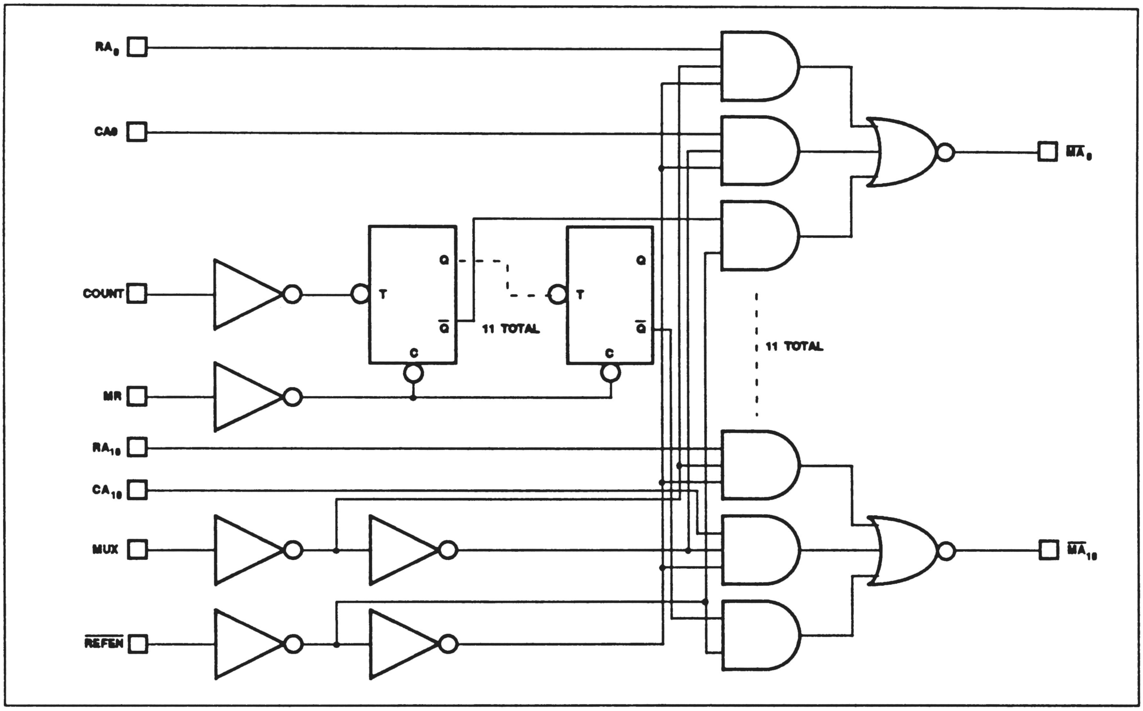
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
Plastic DIP	N74F1762N
PLCC 44	N74F1762A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
RA_0 - RA_{10}	Row address inputs	1.0/1.0	20µA/0.6mA
CA_0 - CA_{10}	Column address inputs	1.0/1.0	20µA/0.6mA
$\overline{MA}_0$ - $\overline{MA}_{10}$	DRAM address outputs	N/A	15mA/20mA
$\overline{REFEN}$	Refresh enable input	1.0/1.0	20µA/0.6mA
MUX	Row/column select input	1.0/1.0	20µA/0.6mA
COUNT	Refresh address count input	1.0/1.0	20µA/0.6mA
MR	Refresh counter reset input	1.0/1.0	20µA/0.6mA

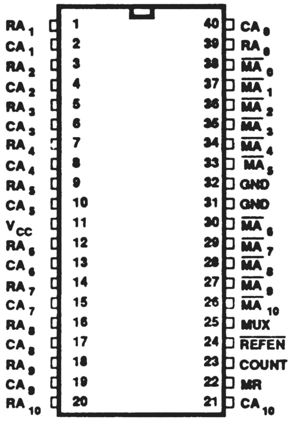
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state. FAST Unit Loads do not correspond to DRAM Input Loads. See Functional Description for details.

LOGIC DIAGRAM

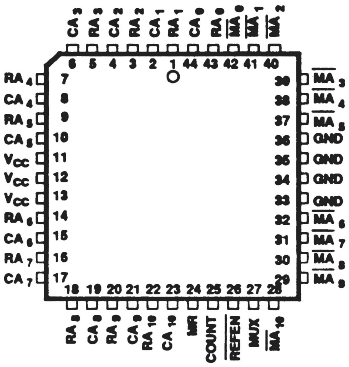

RA9
CA9
COUNT
MR
RA10
CA10
MUX
REFEN
T
Q
Q̄
C
11 TOTAL
11 TOTAL
MA9
MA10

PIN CONFIGURATION

N Package


RA1 1
CA1 2
RA2 3
CA2 4
RA3 5
CA3 6
RA4 7
CA4 8
RA5 9
CA5 10
VCC 11
RA6 12
CA6 13
RA7 14
CA7 15
RA8 16
CA8 17
RA9 18
CA9 19
RA10 20
40 CA0
39 RA0
38 MA0
37 MA1
36 MA2
35 MA3
34 MA4
33 MA5
32 GND
31 GND
30 MA6
29 MA7
28 MA8
27 MA9
26 MA10
25 MUX
24 REFEN
23 COUNT
22 MR
21 CA10

A Package


6 CA3
5 RA3
4 CA2
3 RA2
2 CA1
1 RA1
44 CA0
43 RA0
42 MA0
41 MA1
40 MA2
RA4 7
CA4 8
RA5 9
CA5 10
VCC 11
VCC 12
VCC 13
RA6 14
CA6 15
RA7 16
CA7 17
39 MA3
38 MA4
37 MA5
36 GND
35 GND
34 GND
33 GND
32 MA6
31 MA7
30 MA8
29 MA9
18 RA8
19 CA8
20 RA9
21 CA9
22 RA10
23 CA10
24 MR
25 COUNT
26 REFEN
27 MUX
28 MA10

PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
RA_0 - RA_{10}	39, 1, 3, 5, 7, 9, 12, 14, 16, 18, 20	43, 1, 3, 5, 7, 9, 14, 16, 18, 20, 22	I	Row Address Inputs. When $\overline{REFEN}$ is negated and MUX is Low, these inputs are inverted and propogated to the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs.
CA_0 - CA_{10}	40, 2, 4, 6, 8, 10, 13, 15, 17, 19, 21	44, 2, 4, 6, 8, 10, 15, 17, 19, 21, 23	I	Column Address Inputs. When $\overline{REFEN}$ is negated and MUX is High, these inputs are inverted and propogated to the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs.
$\overline{MA}_0$ - $\overline{MA}_{10}$	38, 37, 36, 35, 34, 33, 30, 29, 28, 27, 26	42, 41, 40, 39, 38, 37, 32, 31, 30, 29, 28	O	Active Low Memory Address Outputs. These outputs contain the address from either the internal refresh counter, the Row Address inputs, or the Column Address inputs depending on the state of the $\overline{REFEN}$ and MUX signal inputs.
$\overline{REFEN}$	24	26	I	Active Low Refresh Enable Input. When asserted, the address contained in the internal refresh counter is asserted on the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs.
MUX	25	27	I	Row / Column Address Multiplex Input. If $\overline{REFEN}$ is High, this signal will multiplex the inverted Row or Column address inputs on the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs when it is asserted Low or High respectively.
COUNT	23	25	I	Refresh Counter Count Clock Input. A Low to High transition on this input will increment the internal refresh counter by one, regardless of the state of REFEN.
MR	22	24	I	Active High Refresh Counter Master Reset Input. A High level on this input will reset the internal refresh counter to all zeros.
V_{CC}	11	11, 12, 13		+5V ± 10% Supply input.
GND	31, 32	33, 34, 35, 36		Ground.

FUNCTIONAL DESCRIPTION:

Functionally, the 'F1762 Memory Address Multiplexer is quite simple. Referring to the logic diagram, the 11-bit Refresh Counter is controlled by the COUNT input, which increments the value stored in the refresh counter on every Low to High transition. When the 'F1762 is used with the 'F1761, this pin is usually connected to the $\overline{REFEN}$ input, so that at the end of every refresh cycle, the refresh counter will be incremented. The Master Reset (MR) input clears the contents of the refresh counter, and may be used for diagnostic testing or initializing after power-up. The eleven 3-to-1 multiplexers are controlled by the MUX and $\overline{REFEN}$ inputs. When $\overline{REFEN}$ is asserted, regardless of the state of the MUX signal, the contents of the internal refresh counter are inverted and asserted at the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs. When $\overline{REFEN}$ is negated, the MUX signal controls which set of address inputs will be propagated to the outputs. With MUX Low, the Row Address inputs (RA_0 - RA_{10}) will be inverted and asserted at the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs. When MUX is High, the Column Addresses (CA_0 - CA_{10}) will be correspondingly asserted.

The $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs have specialized drivers to switch 70 ohm transmission lines (typical of DRAM arrays) on the incident edge, thus improving overall system performance. For more information on the driving characteristics, please refer to the DC electrical characteristics and also Signetics application note number AN218.

FUNCTION TABLE

INPUTS						OUTPUTS	COUNTER
MR	COUNT	MUX	$\overline{\mathrm{REFEN}}$	RA_n	CA_n	$\overline{\mathrm{MA}}_n$	COUNTER CONTENTS
H	X	X	X	X	X	UN*	Reset to 0
L	↑	X	X	X	X	UN*	Increment by 1
H	X	X	L	X	X	L	Reset to 0
L	X	X	L	X	X	COUNTER CONTENTS	Unchanged
L	X	L	H	L	X	H	Unchanged
L	X	L	H	H	X	L	Unchanged
L	X	H	H	X	L	H	Unchanged
L	X	H	H	X	H	L	Unchanged

* The state of the outputs is dependant on the state of the MUX and $\overline{\mathrm{REFEN}}$ inputs. The Counter is reset any time MR is High, and if MR is Low, it is incremented on every low to high transistion of COUNT.

UN = Unspecified
H = High level voltage
L = Low level voltage
X = Don't care
↑ = Low-to-High transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	120	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage[3]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -15mA	±10%V_{CC}	2.5	3.2		V
				±5%V_{CC}	2.7	3.4		V
			I_{OH2} = -35mA	±5%V_{CC}	2.4			V
V_{OL}	Low-level output voltage[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.5	V
				±5%V_{CC}		0.35	0.5	V
			I_{OL2} = 60mA	±5%V_{CC}		0.45	0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Low-level output voltage	V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{IO}[5]	Output current	V_{CC} = MAX, V_{OUT} = 2.25V			-30		-120	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX				55	80	mA
	I_{CCL}					90	120	mA

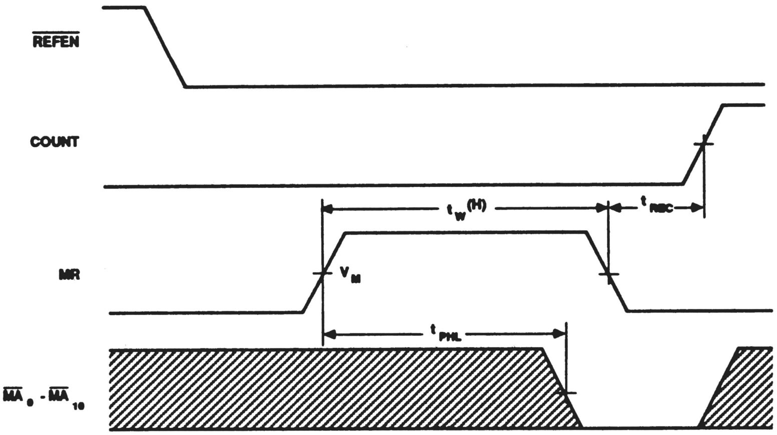
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH2} is the current necessary to guarantee a Low-to-High transition in a 70Ω transmission line.
4. I_{OL2} is the current necessary to guarntee a High-to-Low transition in a 70Ω transmission line.
5. The output conditions have been chosen to produce a current that closely approximates one-half of the short circuit current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 300pF R_L = 70Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 300pF R_L = 70Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay, MUX(↑) to $\overline{MA}_0$ - $\overline{MA}_{10}$, (column address) valid		2.0 2.5	4.5 5.0	7.5 8.0	2.0 2.5	8.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay, MUX(↓) to $\overline{MA}_0$ - $\overline{MA}_{10}$, (row address) valid		4.0 2.0	6.5 4.5	9.5 7.5	3.0 2.0	10.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{REFEN}$ (↑) to $\overline{MA}_0$ - $\overline{MA}_{10}$		2.0 2.0	4.3 4.5	7.5 8.0	2.0 2.0	8.5 11.0	ns
t_{PLH} t_{PHL}	$\overline{REFEN}$ (↓) to $\overline{MA}_0$ - $\overline{MA}_{10}$ (refresh address) valid		4.0 2.0	6.9 4.7	10.5 7.5	3.5 2.0	11.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay, RA_0 - RA_{10} to $\overline{MA}_0$ - $\overline{MA}_{10}$		1.0 0.5	3.0 2.2	6.0 5.0	1.0 0.5	6.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay, CA_0 - CA_{10} to $\overline{MA}_0$ - $\overline{MA}_{10}$		1.0 0.5	3.0 2.2	6.0 5.0	1.0 0.5	6.5 5.5	ns
t_{PLH} t_{PHL}	COUNT (↑) to $\overline{MA}_0$ - $\overline{MA}_{10}$ (refresh address) valid		2.0	15.0	35.0	2.0	40.0	ns
t_{PHL}	Propagation delay, MR(↑) to $\overline{MA}_0$ - $\overline{MA}_{10}$		3.0	5.8	10.5	2.5	11.0	ns
$t_w(H)$	COUNT pulse width, High		5.0			5.0		ns
$t_w(L)$	COUNT pulse width, Low		5.0			5.0		ns
$t_w(H)$	MR Pulse width		5.0			5.0		ns
t_{rec}	Recovery time, MR (↓) to COUNT (↑)		5.0			5.0		ns

AC WAVEFORMS

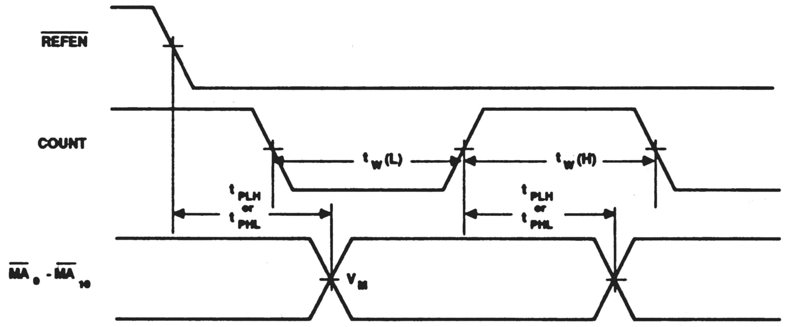


Waveform 1. Waveforms Showing Master Reset Timing

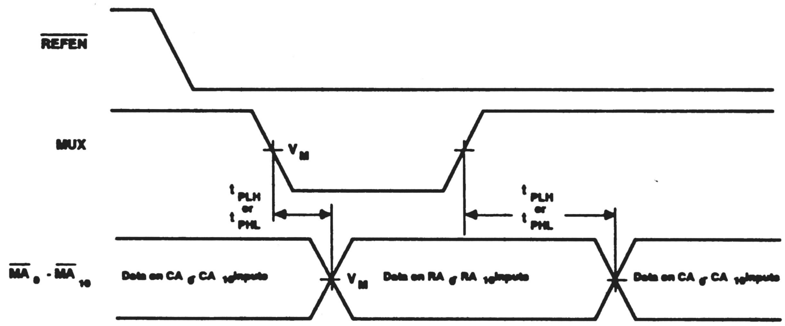
NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

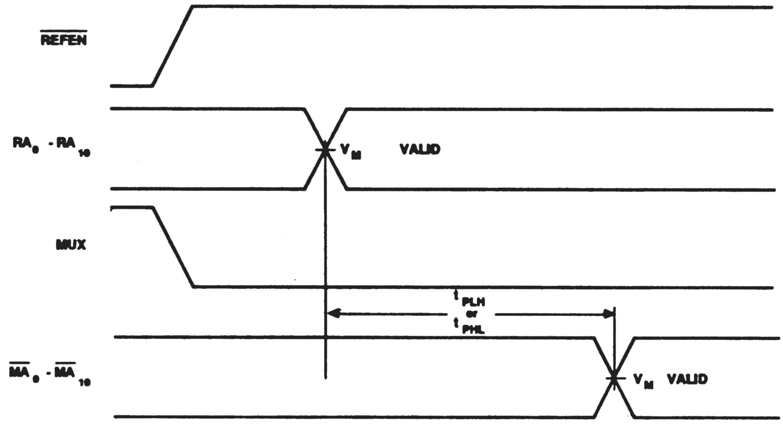
AC WAVEFORMS


REFEN
COUNT
t_W(L)
t_W(H)
t_PLH or t_PHL
t_PLH or t_PHL
MA_0 - MA_10
V_M

Waveform 2. Waveforms Showing Refresh Timing


REFEN
MUX
V_M
t_PLH or t_PHL
t_PLH or t_PHL
MA_0 - MA_10
Data on CA_0 - CA_10 inputs
V_M
Data on RA_0 - RA_10 inputs
Data on CA_0 - CA_10 inputs

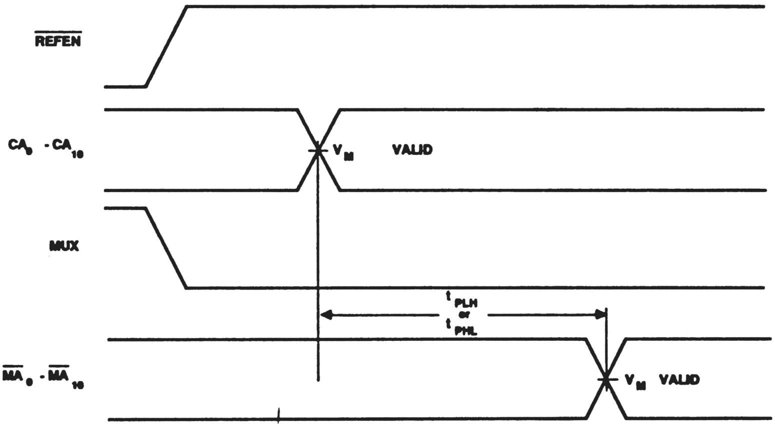
Waveform 3. Waveforms Showing Address Multiplexing Timing


REFEN
RA_0 - RA_10
V_M
VALID
MUX
t_PLH or t_PHL
MA_0 - MA_10
V_M
VALID

Waveform 4. Waveforms Showing RA_0 - RA_{10} to $\overline{MA}_0$ - to $\overline{MA}_{10}$ Propagation Delay

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

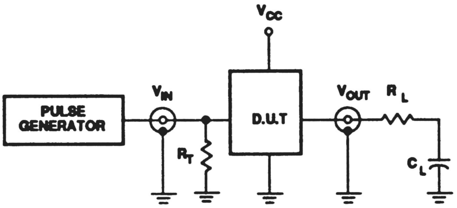
AC WAVEFORMS


$\overline{REFEN}$
CA_0 - CA_{10}
V_M
VALID
MUX
t_{PLH} or t_{PHL}
$\overline{MA}_0$ - $\overline{MA}_{10}$
V_M
VALID

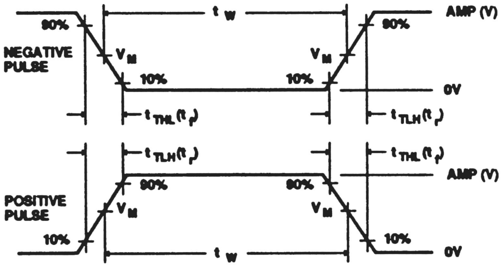
Waveform 4. Waveforms Showing CA_0 - CA_{10} to $\overline{MA}_0$ - to $\overline{MA}_{10}$ Propagation Delay

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
R_T
D.U.T
V_{OUT}
R_L
C_L

Test Circuit For Totem-Pole Outputs


t_W
90%
AMP (V)
NEGATIVE PULSE
V_M
10%
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
POSITIVE PULSE

V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F1763

Intelligent DRAM Controller (IDC)

Preliminary Specification

September 1988

FEATURES

- **DRAM signal timing generator**
- **Automatic refresh circuitry**
- **Selectable row address hold and $\overline{\text{RAS}}$ precharge times**
- **Supports page mode accesses**
- **Controls 1 MBit DRAMs**
- **Intelligent burst-mode refresh after page-mode access cycles**

PRODUCT DESCRIPTION:

The Signetics Intelligent Dynamic RAM Controller is a 1 MBit, single-port version of the popular 74F764 Dual Port Dynamic RAM Controller . It contains automatic signal timing, address multiplexing and refresh control required for interfacing with dynamic RAMs. Additional features have been added to this device to take advantage of technological advances in Dynamic RAMs. A Page-Mode access pin allows the user to assert $\overline{\text{RAS}}$ for the entire access cycle rather than the pre-defined four-clock-cycle pulse width used for normal random access cycles. In addition, the user has the ability to select the $\overline{\text{RAS}}$ precharge time and Row-Address Hold time to fit the particular DRAMs being used. $\overline{\text{DTACK}}$ has been modified from previous family parts to become a negative true, tri-stated output. The options for latched or unlatched address are contained on a single device by the addition of an Address Latch Enable ($\overline{\text{ALE}}$) input. Finally, a burst refresh monitor has been added to ensure complete refreshing after lengthy page-mode access cycles. With a maximum clock frequency of 100 Mhz, the F1763 is capable of driving DRAM arrays with access times down to 40 nsec.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1763	100 MHz	150 mA

ORDERING CODE

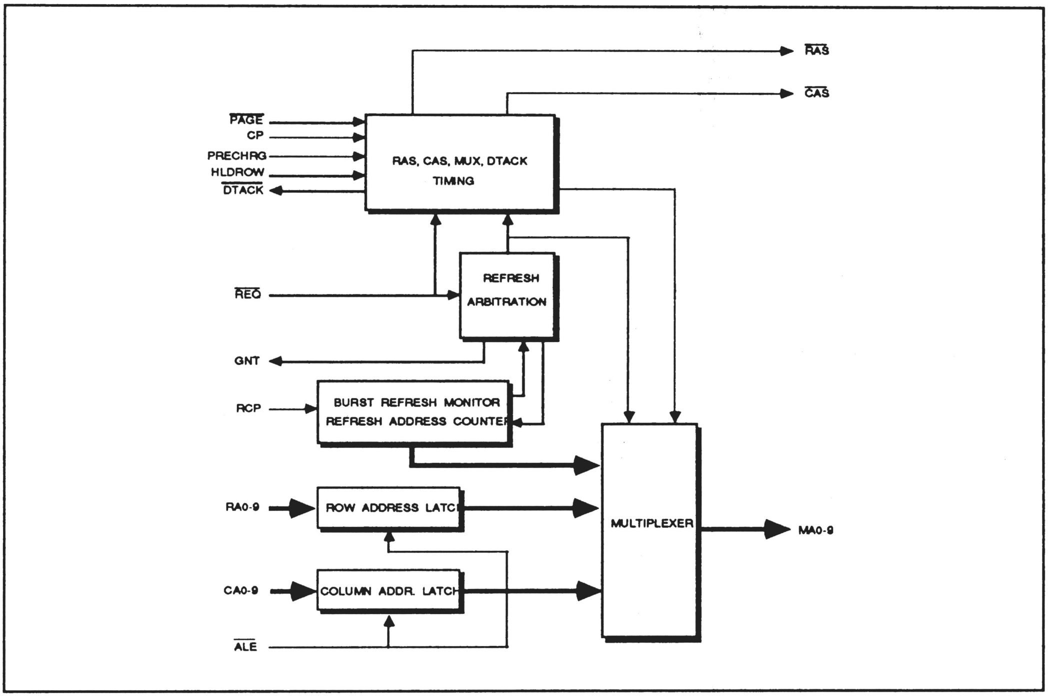
PACKAGES	COMMERCIAL RANGE V_{cc} = 5V ± 10%; T_A=0°C to 70°C
Plastic DIP	74F1763N
PLCC 44	74F1763A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

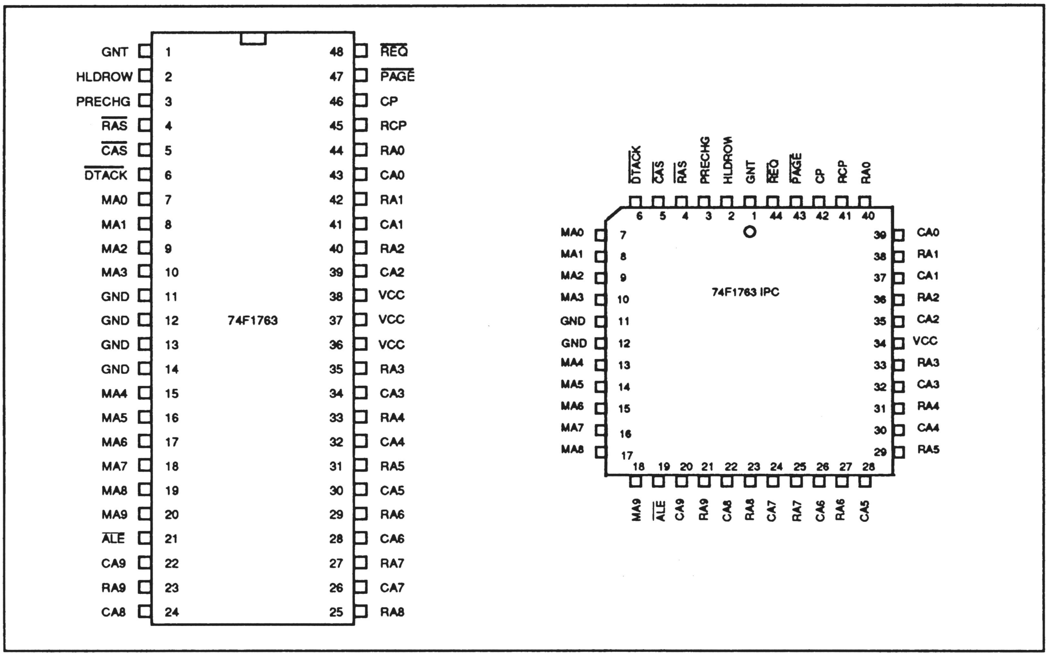
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{\text{REQ}}$	DRAM Request Input	1.0/1.0	20 µA/0.6 mA
CP	Clock Input	1.0/1.0	20 A/0.6 mA
$\overline{\text{PAGE}}$	Page Mode Select Input	1.0/1.0	20 A/0.6 mA
PRECHRG	$\overline{\text{RAS}}$ Precharge Select Input	1.0/1.0	20 A/0.6 mA
HLDROW	Row Hold Select Input	1.0/1.0	20 A/0.6 mA
$\overline{\text{DTACK}}$	Data Transfer Ack. Output	50/80	35 mA/60 mA
GNT	Access Grant Output	50/80	35 mA/60 mA
RCP	Refresh Clock Input	1.0/1.0	20 A/0.6 mA
RA0-RA9	Row Address Inputs	1.0/1.0	20 A/0.6 mA
CA0-CA9	Column Address Inputs	1.0/1.0	20 A/0.6 mA
$\overline{\text{ALE}}$	Address Latch Enable Input	1.0/1.0	20 A/0.6 mA
$\overline{\text{RAS}}$	Row Address Strobe Output	N/A	35 mA/60 mA
$\overline{\text{CAS}}$	Column Address Strobe Output	N/A	35 mA/60 mA
MA0-MA9	DRAM Address Outputs	N/A	35 mA/60 mA

NOTE:
One (1.0) FAST Unit Load is defined as 20 uA in the HIGH state and 0.6 mA in the LOW state.
FAST Unit Loads do not correspond to DRAM Input Loads. See Functional Description for details.

BLOCK DIAGRAM


RAS
CAS
PAGE
CP
PRECHRG
HLDROW
DTACK
RAS, CAS, MUX, DTACK TIMING
REQ
REFRESH ARBITRATION
GNT
RCP
BURST REFRESH MONITOR
REFRESH ADDRESS COUNTER
RA0-9
ROW ADDRESS LATCH
CA0-9
COLUMN ADDR. LATCH
ALE
MULTIPLEXER
MA0-9

PIN CONFIGURATION


GNT 1
HLDROW 2
PRECHG 3
RAS 4
CAS 5
DTACK 6
MA0 7
MA1 8
MA2 9
MA3 10
GND 11
GND 12
GND 13
GND 14
MA4 15
MA5 16
MA6 17
MA7 18
MA8 19
MA9 20
ALE 21
CA9 22
RA9 23
CA8 24
48 REQ
47 PAGE
46 CP
45 RCP
44 RA0
43 CA0
42 RA1
41 CA1
40 RA2
39 CA2
38 VCC
37 VCC
36 VCC
35 RA3
34 CA3
33 RA4
32 CA4
31 RA5
30 CA5
29 RA6
28 CA6
27 RA7
26 CA7
25 RA8
74F1763
DTACK 6
CAS 5
RAS 4
PRECHG 3
HLDROW 2
GNT 1
REQ 44
PAGE 43
CP 42
RCP 41
RA0 40
MA0 7
MA1 8
MA2 9
MA3 10
GND 11
GND 12
MA4 13
MA5 14
MA6 15
MA7 16
MA8 17
39 CA0
38 RA1
37 CA1
36 RA2
35 CA2
34 VCC
33 RA3
32 CA3
31 RA4
30 CA4
29 RA5
74F1763 IPC
MA9 18
ALE 19
CA9 20
RA9 21
CA8 22
RA8 23
CA7 24
RA7 25
CA6 26
RA6 27
CA5 28

PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
$\overline{\text{REQ}}$	48	44	I	Active Low Memory Access Request input, ust be asserted for the entire DRAM access cycle. REQ is sampled on the rising edge of the CP clock.
GNT	1	1	I	Active High Grant output. When High ndicates that a DRAM access cycle has begun. Asserted from the rising edge of the CP clock.
$\overline{\text{PAGE}}$	47	43	I	Active Low Page-Mode Access input. Forces the IDC to keep $\overline{\text{RAS}}$ asserted for as long as the $\overline{\text{PAGE}}$ input is Low.
HLDROW	2	2	I	Row Address Hold input. If Low will configure the IDC to maintain the row addresses for a full CP clock cycle after $\overline{\text{RAS}}$ is asserted. If High will program the IDC to maintain row addresses for a 1/2 CP clock cycle.
PRECHRG	3	3	I	$\overline{\text{RAS}}$ Precharge input. A Low will program the IDC to guarantee a minimum of 4 CP clock cycles of precharge. A High will guarantee 3 clock cycles of precharge.
CP	46	42	I	Clock input. Used by the Controller for all timing and arbitration functions.
RCP	45	41	I	Refresh Clock input. Divided internally by 64 to produce an internal Refresh Request.
$\overline{\text{DTACK}}$	6	6	O	Active Low, 3-state Data Transfer Acknowledge output. Enabled by the $\overline{\text{REQ}}$ input and asserted four clock cycles after the assertion of $\overline{\text{RAS}}$.
RA0-RA9			I	Row Address inputs. Propogated to the MA0-9 outputs when GNT is asserted.
CA0-CA9			I	Column Address inputs. Propogated to the MA0-9 outputs 1 CP clock cycle after $\overline{\text{RAS}}$ is asserted, if HLDROW=0 or 1/2 clock cycle later if HLDROW is 1.
$\overline{\text{RAS}}$	4	4	O	Active Low Row Address Strobe. Asserted for four clock cycles during each refresh cycle. Also asserted for four clock cycles during processor access if the $\overline{\text{PAGE}}$ input is false. If PAGE is true, $\overline{\text{RAS}}$ is negated upon negation of $\overline{\text{PAGE}}$ or $\overline{\text{REQ}}$, whichever occurs first.
$\overline{\text{CAS}}$	5	5	O	Active Low Column Address Strobe. Asserted 1 CP clock cycle after $\overline{\text{RAS}}$ if HLDROW=1, or 1 1/2 clock cycle later if HLDROW=0. Negated upon negation of $\overline{\text{REQ}}$.
MA0-MA9			O	DRAM multiplexed address outputs. Row and column addresses asserted on these pins during an access cycle. Refresh counter addresses presented on these outputs during refresh cycles.
$\overline{\text{ALE}}$	21	19	I	Active Low Address Latch Enable input. A Low on this pin will cause the address latches to be transparent. A Low to High transition will latch the RA0-9 & CA0-9 inputs.
V_{CC}	36-38	34		+5 V ± 10% Supply Input.
GND	11-14	11,12		Ground

FUNCTIONAL DESCRIPTION

The 74F1763 1 Megabit Intelligent DRAM Controller (IDC) is a synchronous device with all signal timing being a function of the CP input clock.

Arbitration:

When a memory access request ($\overline{\text{REQ}}$) is asserted and sampled by the IDC, internal arbitration takes place between this request and any pending refresh requests. Refresh always has priority over a memory access cycle and is serviced either immediately or following the current memory access cycle (if any). The IDC will perform a refresh cycle immediately when it becomes due if it is not performing a memory access cycle. If a memory refresh becomes due during a memory access cycle the controller will wait until after its completion before starting a refresh cycle. Similarly, if a memory access request is made when a refresh cycle is in process, the DRAM controller will wait until the cycle is completed before granting access to the requesting processor. If no refresh cycle is in process, and the $\overline{\text{RAS}}$ precharge requirement of the DRAM has been satisfied, the access will be granted within one clock cycle of the CP clock . The Grant (GNT) output goes high at this time to indicate the start of a memory access cycle.

Address multiplexing:

The row (RA0-9) and column (CA0-9) address inputs may be latched at any time using the $\overline{\text{ALE}}$ input pin. Otherwise the $\overline{\text{ALE}}$ input should remain Low to allow the addresses to propagate to the MA0-9 address outputs. When GNT becomes valid, the RA0-9 address inputs will have already propagated to the MA0-9 outputs for the row address. At this time, the $\overline{\text{RAS}}$ output becomes valid. One or one-half CP clock cycles later (depending on the state of the HLDROW input) the CA0-9 address inputs are propagated to the MA0-9 outputs for a column address. $\overline{\text{CAS}}$ is always asserted one and one-half CP clock cycles after $\overline{\text{RAS}}$ is asserted. If the $\overline{\text{PAGE}}$ input is High, $\overline{\text{RAS}}$ will be negated approximately four CP clock cycles after its initial assertion. At this time the $\overline{\text{DTACK}}$ output becomes valid indicating the completion of a memory access cycle. The IDC will maintain the state of all its outputs untill the $\overline{\text{REQ}}$ input is negated (see AC electrical characteristics).

Row address hold times:

If the HLDROW input of the IDC is High the row address outputs will remain valid 1/2 CP clock cycle after $\overline{\text{RAS}}$ is asserted. If the HLDROW input is Low the row address outputs will remain valid one CP clock cycle after $\overline{\text{RAS}}$ is asserted.

$\overline{\text{RAS}}$ precharge timing:

In order to meet the $\overline{\text{RAS}}$ precharge requirement of dynamic RAMs, the controller will hold-off a subsequent $\overline{\text{RAS}}$ signal assertion due to a processor access request or a refresh cycle for four or three full CP clock cycles from the previous negation of $\overline{\text{RAS}}$, depending on the state of the PRECHG input. If the PRECHG input is Low, $\overline{\text{RAS}}$ remains High for at least 4 CP clock cycles. If the PRECHG input is High $\overline{\text{RAS}}$ remains High for at least 3 CP clock cycles.

Refresh timing:

The refreshing block of the controller functions by accepting a refresh clock (RCP) and dividing it down internally by 64 to produce an internal refresh request. This refresh request is recognized either immediately or at the end of a running memory access cycle. Due to the possibility that page mode access cycles may be lengthy, the controller keeps track of how many refresh requests have been missed by logging them internally (up to 128) and services any pending refresh requests at the end of the memory access cycle. The controller performs $\overline{\text{RAS}}$-only refresh cycles until all pending refresh requests are depleted.

Page-mode access:

Fast accesses to consecutive locations of DRAM can be realized by asserting the $\overline{\text{PAGE}}$ input while requesting access to the memory. In this mode, the controller does not automatically negate $\overline{\text{RAS}}$ after four CP clock cycles, but keeps it asserted throughout the access cycle. By using external gates, the $\overline{\text{CAS}}$ output can be gated on and off while changing the column address inputs to the controller, which will propogate to the MA0-9 address outputs and provide a new column address. This is only useful if the $\overline{\text{ALE}}$ input is Low, enabling the user to change addresses. This mode can be used with DRAMs that support page or nibble mode addressing.

Output driving characteristics:

Considering the transmission line characteristic of the DRAM arrays, the outputs of the IDC have been designed to provide incident-edge switching, needed in high performance systems. For more information on the driving characteristics, please refer to Signetics application note number AN218.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		LIMITS	UNIT
VCC	Supply Voltage	-0.5 to +7.0	V
V_{IN}	Input Voltage	-0.5 to +7.0	V
I_{IN}	Input Current	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	120	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				+0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	HIGH-level output current				-35	mA
I_{OL}	LOW-level output current	Buffer			60	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -15mA	±10% V_{CC}	2.5	3.2		V
				±5% V_{CC}	2.7	3.4		V
			I_{OH2}[3] = -35 mA	±10% V_{CC}	2.4			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10% V_{CC}		0.35	0.50	V
				±5% V_{CC}		0.35	0.50	V
			I_{OL2}[4] = 60mA	±10% V_{CC}		0.45	0.80	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Short circuit output current	V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	V_{CC} = MAX					200	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at Vcc = 5V, T_A = 25°C.
3. I_{OH2} is the current necessary to guarantee a LOW to HIGH transition in a 70Ω transmission line.
4. I_{OL2} is the current necessary to guarantee a HIGH to LOW transition in a 70Ω transmission line.

AC ELECTRICAL CHARACTERISTICS

NO	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A=0°C to +70°C V_{cc}=+5.0V ±10% C_L=300pF RL=70Ω			T_A=0°C to +70°C V_{cc}=+5.0V ±10% C_L=300pF RL=70Ω		
			Min	Typ	Max	Min	Max	
1	CP clock period (tcp)		10			10		ns
2	CP clock low time		5			5		ns
3	CP clock high time		5			5		ns
4	RCP clock period		100			100		ns
5	RCP clock low time		10			10		ns
6	RCP clock high time		10			10		ns
7	Setup time $\overline{\text{REQ}}$ to CP(↑)		2			2		ns
8	Propagation delay CP(↑) to GNT High		5	10	14	5	16	ns
9	Propagation delay $\overline{\text{REQ}}$(↑) to GNT Low		7	12	16	7	18	ns
10	RA0-9, CA0-9 High or Low set-up to $\overline{\text{ALE}}$(↑)		2			2		ns
11	$\overline{\text{ALE}}$(↑) to RA0-9,CA0-9 High or Low hold		2			2		ns
12	Propagation delay RA0-9,CA0-9 High or Low to MA0-9		4	7	12	4	13	ns
13	Propagation delay $\overline{\text{REQ}}$(↑) to MA0-9		7	12	25	7	25	ns
14	Propagation delay CP(↑) to valid MA0-9 (column address)		5	12	17	5	18	ns
15	MA0-9 (row address) hold after $\overline{\text{RAS}}$(↓)	HLDROW = 1	1/2tcp			1/2tcp		ns
16	Propagation delay CP(↑) to $\overline{\text{RAS}}$(↓)		5	10	14	5	16	ns
17	MA0-9 (row address) hold after $\overline{\text{RAS}}$(↓)	HLDROW = 0	1tcp			1tcp		ns
18	$\overline{\text{RAS}}$ Low pulse width	PAGE = 1	4tcp			4tcp		ns
19	Propagation delay CP(↑) to $\overline{\text{RAS}}$(↑)		6	11	15	6	17	ns
20	Propagation delay $\overline{\text{REQ}}$(↑) to $\overline{\text{RAS}}$(↑)		8	13	17	8	19	ns
21	Propagation delay CP(↓) to $\overline{\text{CAS}}$(↓)		5	10	14	5	16	ns
22	Propagation delay $\overline{\text{PAGE}}$(↑) to $\overline{\text{RAS}}$(↑)		4	7	12	4	13	ns
23	Propagation delay $\overline{\text{RAS}}$(↓) to $\overline{\text{CAS}}$(↓)		1.5tcp -5	1.5tcp -2	1.5tcp	1.5tcp -5	1.5tcp	ns
24	Propagation delay $\overline{\text{REQ}}$(↑) to $\overline{\text{CAS}}$(↑)		6	11	15	6	17	ns

AC ELECTRICAL CHARACTERISTICS

NO	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A=0°C to +70°C V_{cc}=+5.0V ±10% C_L=300pF RL=70Ω			T_A=0°C to +70°C V_{cc}=+5.0V ±10% C_L=300pF RL=70Ω		
			Min	Typ	Max	Min	Max	
25	Set-up time $\overline{\text{PAGE}}$(↓) to CP(↑)		2			2		ns
26	Propagation delay CP(↑) to $\overline{\text{DTACK}}$(↓)		5	10	14	5	16	ns
27	Propagation delay $\overline{\text{REQ}}$(↓) to $\overline{\text{DTACK}}$(↑)				12		14	ns
28	Propagation delay $\overline{\text{RAS}}$(↓) to $\overline{\text{DTACK}}$(↓)			4tcp				ns
29	Propagation delay $\overline{\text{REQ}}$(↑) to $\overline{\text{DTACK}}$(3-state)				12		14	ns
30	MA0-9 (refresh address) set-up to $\overline{\text{RAS}}$(↓)	PRECHRG =1		1/2tcp				ns
31	MA0-9 (refresh address) set-up to $\overline{\text{RAS}}$(↓)	PRECHRG = 0		1/2tcp				ns
32	MA0-9 (refresh address) hold after $\overline{\text{RAS}}$(↓)	PRECHRG = 1	1tcp	1tcp +20	1tcp +30	1tcp	1tcp +35	ns
33	MA0-9 (refresh address) hold after $\overline{\text{RAS}}$(↓)	PRECHRG = 0	1tcp	1tcp +20	1tcp +30	1tcp	1tcp +35	ns
34	$\overline{\text{RAS}}$ high (precharge) time	PRECHRG = 0	4tcp			4tcp		ns
35	$\overline{\text{RAS}}$ low time	PRECHRG = 0	4tcp			4tcp		ns
36	$\overline{\text{RAS}}$ high (precharge) time	PRECHRG = 1	3tcp			3tcp		ns
37	$\overline{\text{RAS}}$ low time	PRECHRG = 1	4tcp			4tcp		ns

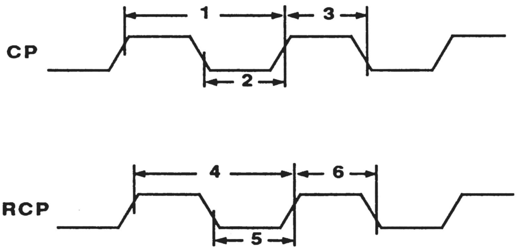

CP
1
2
3
RCP
4
5
6

Figure 1: Clock cycle Timing

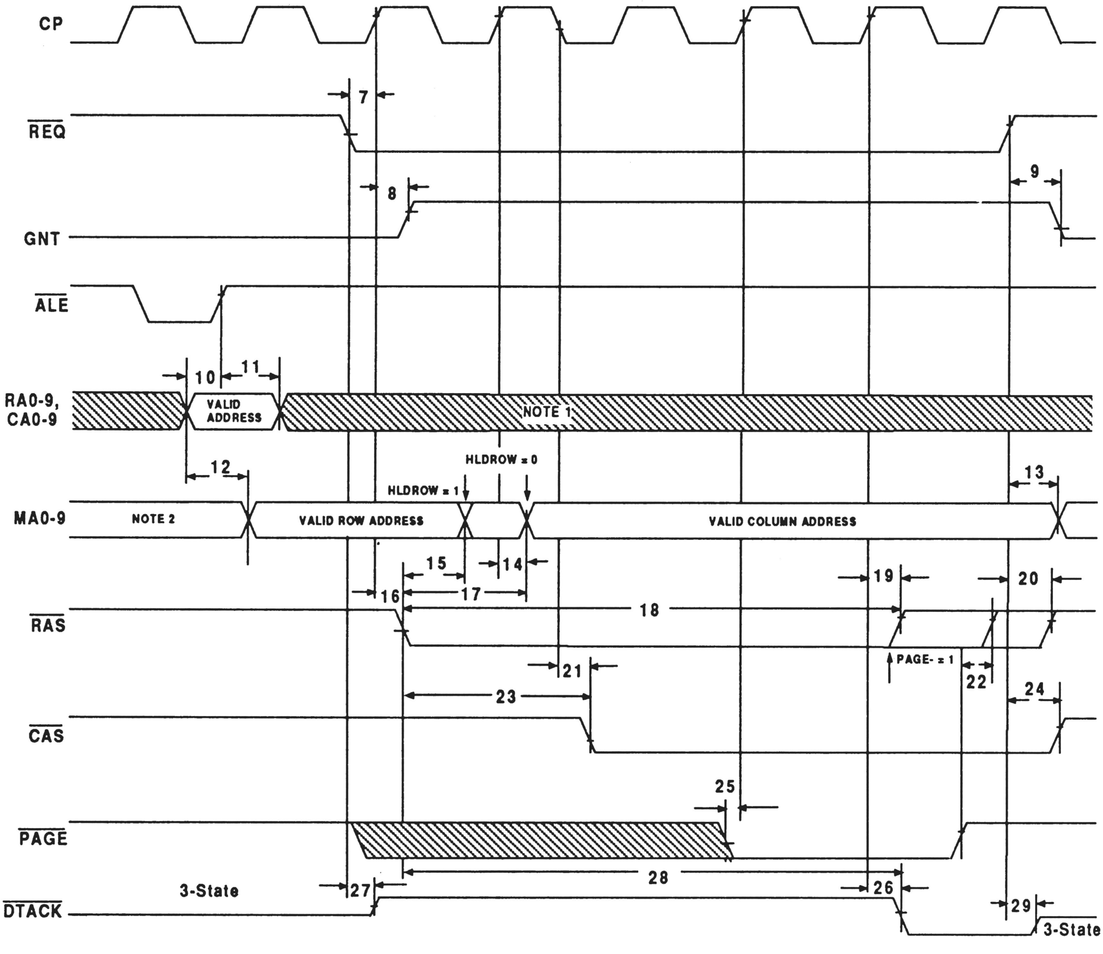

CP
REQ
GNT
ALE
RA0-9, CA0-9
MA0-9
RAS
CAS
PAGE
DTACK
VALID ADDRESS
NOTE 1
NOTE 2
VALID ROW ADDRESS
VALID COLUMN ADDRESS
HLDROW = 1
HLDROW = 0
PAGE- = 1
3-State
3-State
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29

Figure 2: Memory access cycle timing

Note 1: If the RA0-9 & CA0-9 address inputs are not latched, they should remain valid until the corresponding $\overline{\text{REQ}}$ is negated.
Note 2: MA0-9 outputs will contain the present row address on the RA0-9 inputs or the last row address latched into the device.

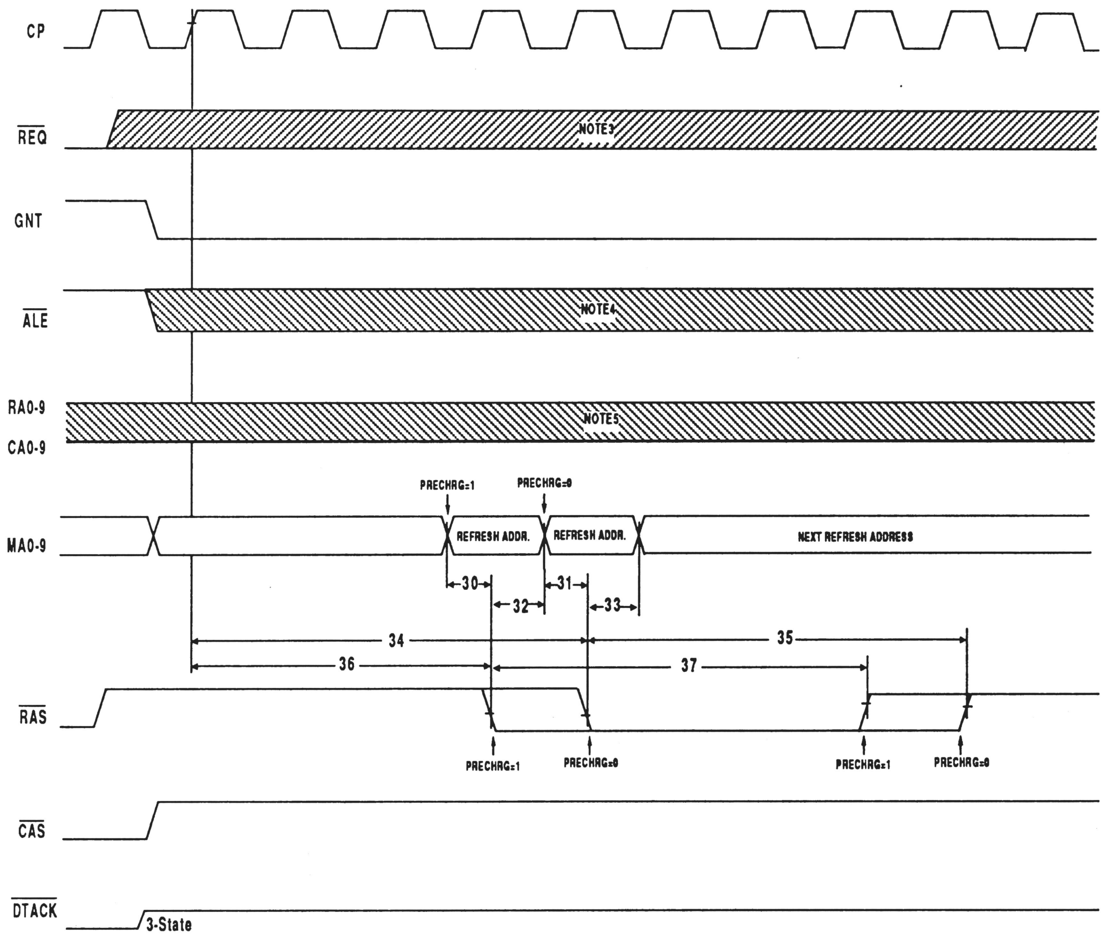

CP
REQ
NOTE3
GNT
ALE
NOTE4
RA0-9
CA0-9
NOTE5
PRECHRG=1
PRECHRG=0
MA0-9
REFRESH ADDR.
REFRESH ADDR.
NEXT REFRESH ADDRESS
30
31
32
33
34
35
36
37
RAS
PRECHRG=1
PRECHRG=0
PRECHRG=1
PRECHRG=0
CAS
DTACK
3-State

Figure 3: Refresh cycle timing following a memory access cycle

Note 3: $\overline{REQ}$ input is a don't care during a memory refresh cycle. If $\overline{REQ}$ is asserted during a refresh cycle, it will be recognized at the first rising CP clock edge, but GNT will not be asserted until after the completion of the refresh cycle (see Figure 4).

Note 4: RA0-9 & CA0-9 address inputs may be latched at anytime during a memory refresh cycle. However, a memory access cycle will not begin until after the completion of the refresh cycle.

Note 5: RA0-9 & CA0-9 are don't care during a memory refresh cycle.

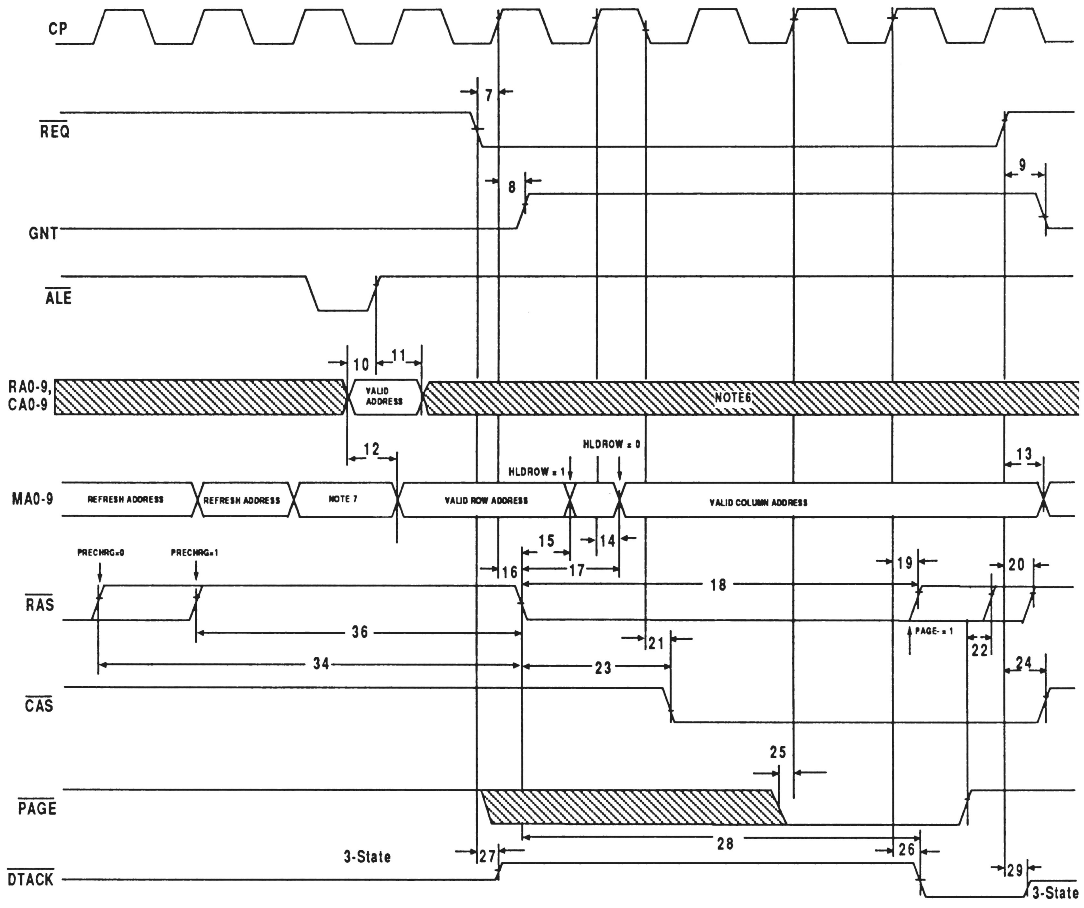

CP
REQ
GNT
ALE
RA0-9,
CA0-9
VALID ADDRESS
NOTE6
MA0-9
REFRESH ADDRESS
REFRESH ADDRESS
NOTE 7
VALID ROW ADDRESS
VALID COLUMN ADDRESS
HLDROW = 1
HLDROW = 0
RAS
PRECHRG=0
PRECHRG=1
PAGE- = 1
CAS
PAGE
DTACK
3-State
3-State
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
34
36

Figure 4: Memory access cycle timing following a refresh cycle

Note 6: If RA0-9 & CA0-9 address inputs are not latched, they should remain valid until the corresponding $\overline{\text{REQ}}$ is negated.
Note 7: MA0-9 outputs will contain the present row address on the RA0-9 inputs or the last row address latched into the device.

FAST 74F2952, 74F2953 Transceivers

'F2952 Registered Transceiver, Non-Inverting (3-State)
'F2953 Registered Transceiver, Inverting (3-State)
Product Specification

FEATURES

- **8-bit Registered Transceivers**
- **Two 8-bit , back-to-back registers store data moving in both directions between two bidirectional busses**
- **Separate Clock, Clock Enable and 3-state Enable provided for each register**
- **'F2952 Non-inverting 'F2953 Inverting**
- **AM2952/2953 functional equivalent**
- **A outputs sink 24mA and source 3mA**
- **B outputs sink 64mA and source 15mA**
- **300 mil wide 24-pin Slim DIP package**

DESCRIPTION

The 74F2952 and 74F2953 are 8-bit Registered Transceivers. Two 8-bit back to back registers store data flowing in both directions between two bi-directional busses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{\text{CEXX}}$) is Low. The data is then present at the 3-state output buffers, but is only accessible when the Output Enable ($\overline{\text{OEXX}}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F2952	160MHz	105mA
74F2953	160MHz	105mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F2952N, N74F2953N
24-Pin Plastic SOL[1]	N74F2952D, N74F2953D

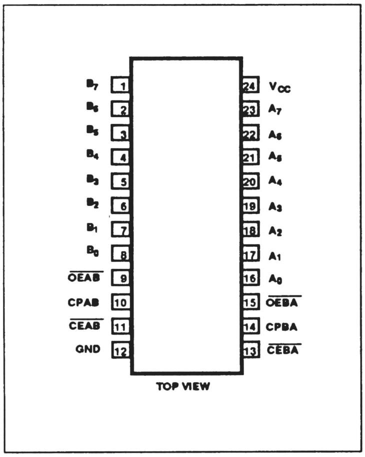
NOTE:
1.Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

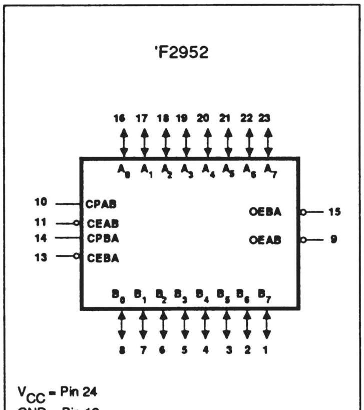
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	Port A, 3-state inputs	3.5/1.0	70μA/0.6mA
B_0 - B_7	Port B, 3-state inputs	3.5/1.0	70μA/0.6mA
CPAB,CPBA	Clock inputs	1.0/1.0	20μA/0.6mA
$\overline{\text{CEAB}}$,$\overline{\text{CEBA}}$	Clock Enable inputs	1.0/1.0	20μA/0.6mA
$\overline{\text{OEAB}}$,$\overline{\text{OEBA}}$	Output Enable inputs	1.0/1.0	20μA/0.6mA
A_0 - A_7	Port A, 3-state outputs	150/40	3.0mA/24mA
B_0 - B_7	Port B, 3-state outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

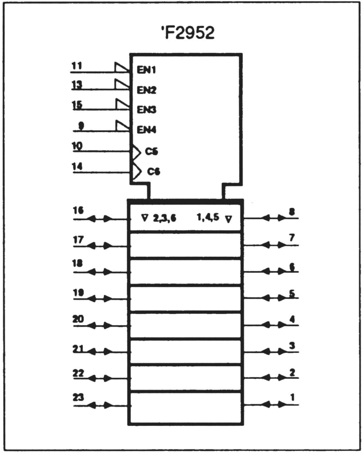

B7 1
B6 2
B5 3
B4 4
B3 5
B2 6
B1 7
B0 8
OEAB 9
CPAB 10
CEAB 11
GND 12
24 VCC
23 A7
22 A6
21 A5
20 A4
19 A3
18 A2
17 A1
16 A0
15 OEBA
14 CPBA
13 CEBA
TOP VIEW

LOGIC SYMBOL

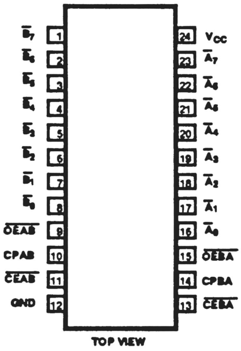

'F2952
16 17 18 19 20 21 22 23
A0 A1 A2 A3 A4 A5 A6 A7
10 CPAB
11 CEAB
14 CPBA
13 CEBA
OEBA 15
OEAB 9
B0 B1 B2 B3 B4 B5 B6 B7
8 7 6 5 4 3 2 1

V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

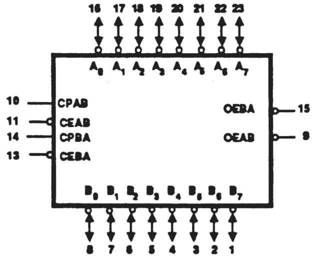

'F2952
11 EN1
13 EN2
15 EN3
9 EN4
10 C5
14 C6
∇ 2,3,6
1,4,5 ∇
16
17
18
19
20
21
22
23
8
7
6
5
4
3
2
1

PIN CONFIGURATION


$\overline{B}_7$ 1
$\overline{B}_6$ 2
$\overline{B}_5$ 3
$\overline{B}_4$ 4
$\overline{B}_3$ 5
$\overline{B}_2$ 6
$\overline{B}_1$ 7
$\overline{B}_0$ 8
$\overline{OEAB}$ 9
CPAB 10
$\overline{CEAB}$ 11
GND 12
24 V_{CC}
23 $\overline{A}_7$
22 $\overline{A}_6$
21 $\overline{A}_5$
20 $\overline{A}_4$
19 $\overline{A}_3$
18 $\overline{A}_2$
17 $\overline{A}_1$
16 $\overline{A}_0$
15 $\overline{OEBA}$
14 CPBA
13 $\overline{CEBA}$
TOP VIEW

LOGIC SYMBOL

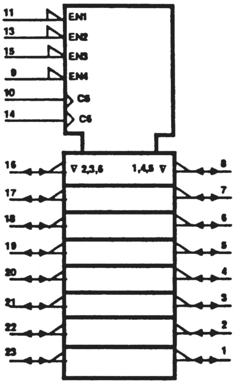
'F2953


16 17 18 19 20 21 22 23
A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7
10 CPAB
11 CEAB
14 CPBA
13 CEBA
OEBA 15
OEAB 9
B_0 B_1 B_2 B_3 B_4 B_5 B_6 B_7
8 7 6 5 4 3 2 1

V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

'F2953


11 EN1
13 EN2
15 EN3
9 EN4
10 C5
14 C6
∇ 2,3,6
1,4,5 ∇
16
17
18
19
20
21
22
23
8
7
6
5
4
3
2
1

FUNCTION TABLE for Register A_n or B_n

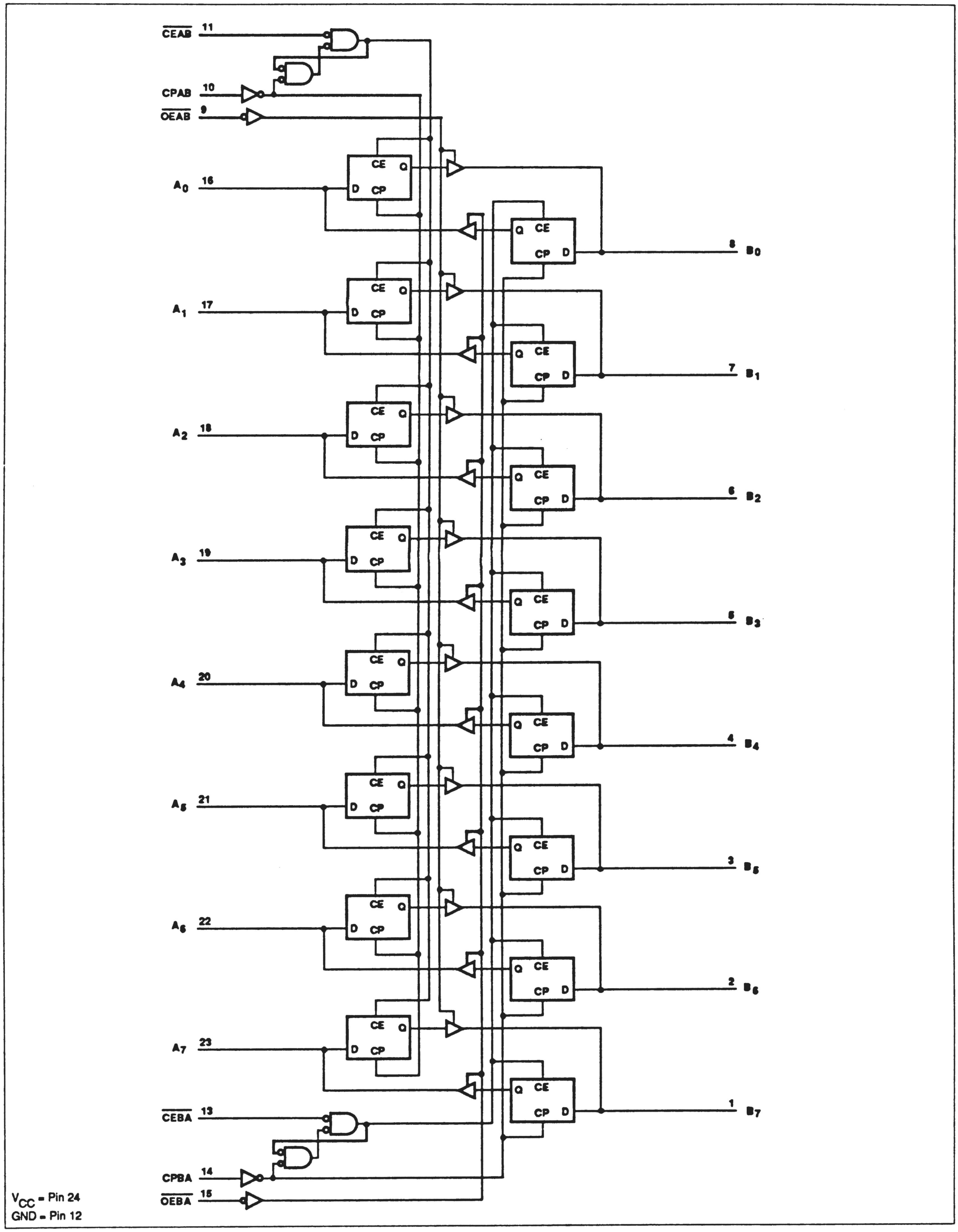
INPUTS			INTERNAL Q	OPERATING MODE
A_n or B_n	CPXX	$\overline{CEXX}$		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	

FUNCTION TABLE for Output Enable

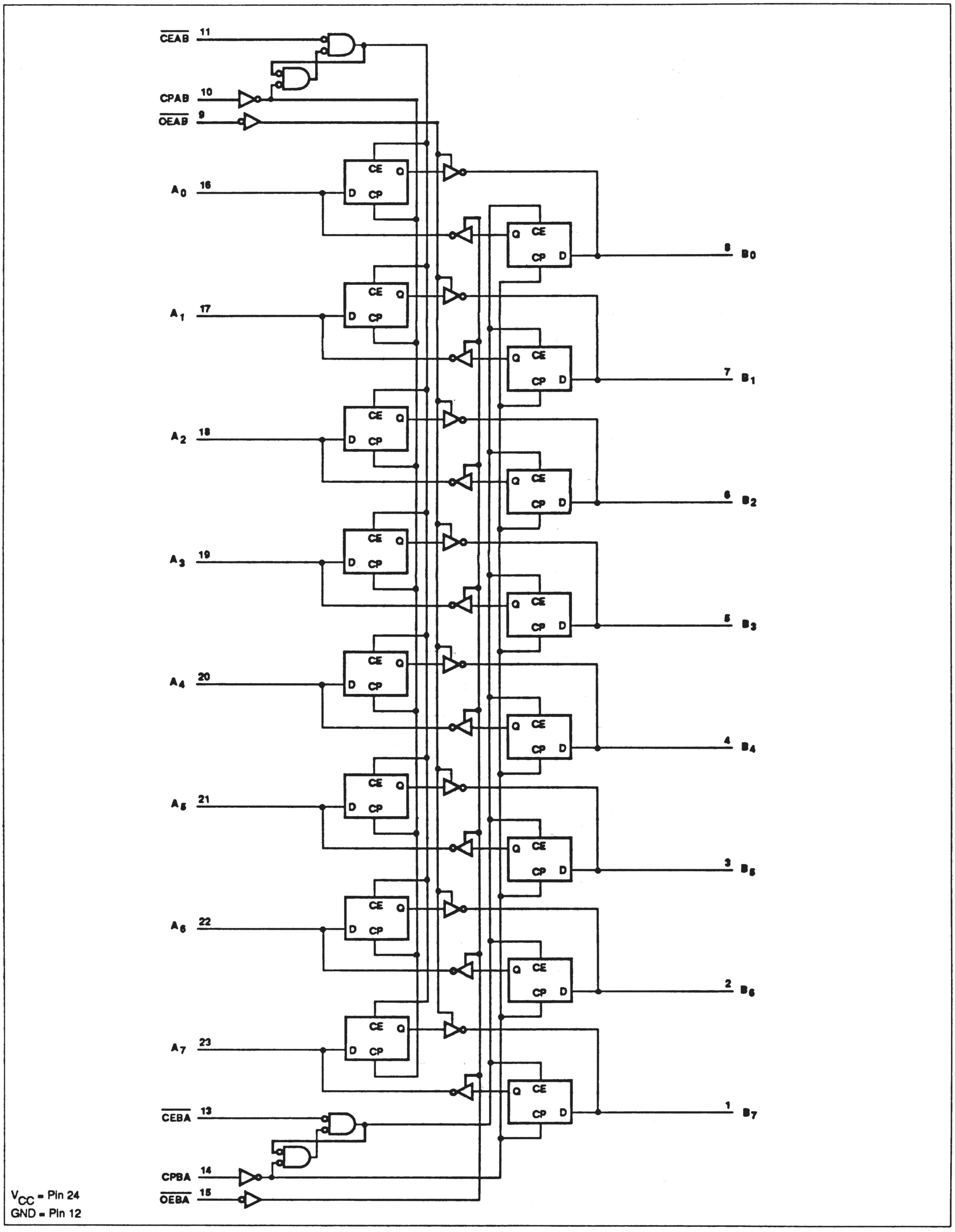
INPUTS	INTERNAL Q	A_n or B_n OUTPUTS		OPERATING MODE
$\overline{OEXX}$		'F2952	'F2953	
H	X	Z	Z	Disable outputs
L	L	L	H	Enable outputs
L	H	H	L	

H= High voltage level
L= Low voltage level
↑ =Low-to-High transition
X=Don't care
XX=AB or BA
NC=No change
Z =High impedance "off" state

LOGIC DIAGRAM for 'F2952


$\overline{\text{CEAB}}$ 11
CPAB 10
$\overline{\text{OEAB}}$ 9
A_0 16
A_1 17
A_2 18
A_3 19
A_4 20
A_5 21
A_6 22
A_7 23
$\overline{\text{CEBA}}$ 13
CPBA 14
$\overline{\text{OEBA}}$ 15
CE Q
D CP
Q CE
CP D
8 B_0
7 B_1
6 B_2
5 B_3
4 B_4
3 B_5
2 B_6
1 B_7
V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM for 'F2953


CEAB 11
CPAB 10
OEAB 9
A0 16
A1 17
A2 18
A3 19
A4 20
A5 21
A6 22
A7 23
CE Q
D CP
Q CE
CP D
8 B0
7 B1
6 B2
5 B3
4 B4
3 B5
2 B6
1 B7
CEBA 13
CPBA 14
OEBA 15
V_{CC} = Pin 24
GND = Pin 12

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0-B_7			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=-3mA	±10%VCC	2.4			V
					±5%VCC	2.7	3.3		V
		B_0-B_7		I_{OH}=-15mA	±10%VCC	2.0			V
					±5%VCC	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL}=24mA	±10%VCC		0.35	0.50	V
					±5%VCC		0.35	0.50	V
		B_0-B_7		I_{OL}=48mA	±10%VCC		0.38	0.55	V
				I_{OL}=64mA	±5%VCC		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	CPAB, CPBA, $\overline{OEAB}$ $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$	V_{CC} = 5.5V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	CPAB, CPBA, $\overline{OEAB}$ $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	CPAB, CPBA, $\overline{OEAB}$ $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
$I_{IH}+I_{OZH}$	Off-state output current High-level voltage applied	A_0-A_7, B_0-B_7	V_{CC} = MAX, V_O= 2.7V					70	µA
$I_{IL}+I_{OZL}$	Off-state output current Low-level voltage applied	A_0-A_7, B_0-B_7	V_{CC} = MAX, V_O = 0.5V					-600	µA
I_O	Output current[3]	A_0-A_7	V_{CC} = MAX, V_O=2.25V			-20		-80	mA
		B_0-B_7				-50		-160	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				90	140	mA
		I_{CCL}					120	175	mA
		I_{CCZ}					105	155	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit ouptput current, I_{OS}.

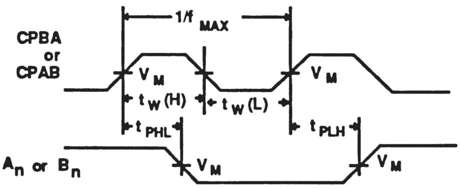
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F2952, 74F2953					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	145	160		135		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA or CPAB to A_n or B_n	Waveform 1	3.0 3.5	5.0 6.0	7.5 8.5	2.5 3.5	8.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	Waveform 3 Waveform 4	2.0 3.5	4.5 6.0	7.0 9.5	2.0 3.0	8.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	Waveform 3 Waveform 4	2.0 1.5	4.0 3.5	8.0 6.5	1.5 1.0	9.0 7.0	ns

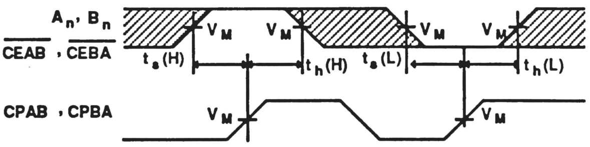
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	74F2952, 74F2953					UNIT
				T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	'F2952	Waveform 2	4.5 3.5			5.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	'F2953	Waveform 2	4.0 3.5			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA		Waveform 2	0.0 0.0			0.0 0.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEAB}$,$\overline{CEBA}$ to CPAB , CPBA		Waveform 2	0.0 4.0			0.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEAB}$,$\overline{CEBA}$ to CPAB , CPBA		Waveform 2	2.5 2.5			2.5 3.0		ns
$t_w(H)$ $t_w(L)$	CPAB or CPBA Pulse width, High or Low		Waveform 1	3.0 3.5			3.0 3.5		ns

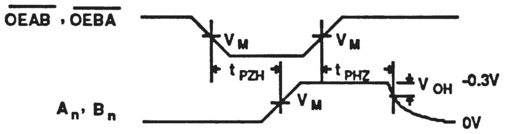
AC WAVEFORMS


CPBA
or
CPAB
1/f MAX
V M
t W (H)
t W (L)
t PHL
t PLH
A n or B n

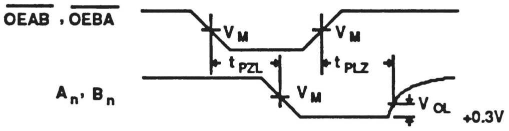
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency


A n, B n
CEAB, CEBA
t s (H)
t h (H)
t s (L)
t h (L)
V M
CPAB, CPBA

Waveform 2. Data Setup And Hold Times


OEAB, OEBA
V M
t PZH
t PHZ
V OH -0.3V
A n, B n
0V

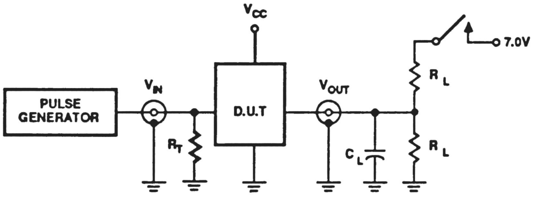
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level


OEAB, OEBA
V M
t PZL
t PLZ
A n, B n
V OL +0.3V

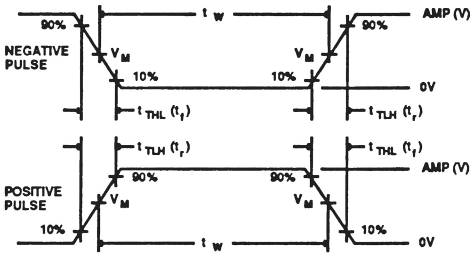
Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded area indicate when the input is permitted to change for predictable output

TEST CIRCUIT AND WAVEFORMS


V CC
7.0V
PULSE GENERATOR
V IN
R T
D.U.T
V OUT
C L
R L
R L

Test Circuit For 3-State Outputs


t W
AMP (V)
90%
NEGATIVE PULSE
V M
10%
0V
t THL (t f)
t TLH (t r)
POSITIVE PULSE
90%
10%

V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F3893

Quad FutureBus Backplane Transceiver

(3 State +Open Collector)

FEATURES

- **Ouad Backplane Transceiver**
- **Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms**
- **Reduced voltage swing (1 volt) produces less noise and reduces power consumption**
- **High speed operation enhances performance of backplane buses and facilities incident wave switching**
- **Compatible with IEEE 896 Futurebus Standards**
- **Built-in precision band-gap (BG) reference provides accurate receiver threshold and improved noise immunity**
- **Controlled output ramp and multiple GND pins minimize ground bounce**
- **Glitch-free power up / power down operation**
- **Pin and function compatible with NSC DS3893**

Preliminary Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3893	3.5ns	70mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin PLCC	N74F3893A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20μA/0.6mA
DE	Data Enable input	1.0/1.0	20μA/0.6mA
$\overline{RE}$	Receiver Enable input	1.0/1.0	20μA/0.6mA
I/O_0- I/O_3	Receiver inputs	1.0/1.0	20μA/0.6mA
I/O_0- I/O_3	Driver outputs	OC/33	OC/20mA
R_0 - R_3	Receiver outputs	50/33	1mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC = Open Collector

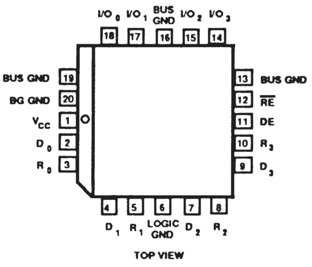
DESCRIPTION

The 74F3893 is a quad backplane transceiver and is intended to be used in very high speed bus systems.

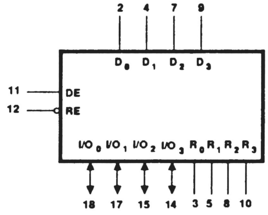
The 74F3893 interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading (< 7 pF). Incident wave switching is employed, therefore BTL propagation delays are short. Although the voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane.

PIN CONFIGURATION

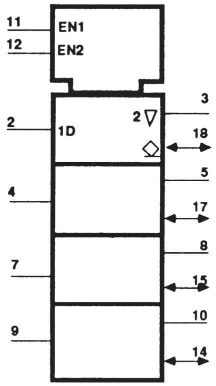


LOGIC SYMBOL

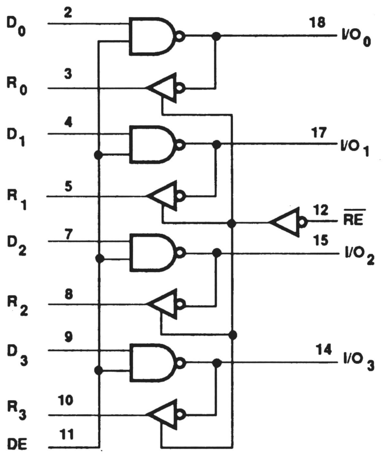


V_{CC} = Pin 1
LOGIC GND = Pin 6
BUS GND = Pin 13, 16, 19
BG GND = Pin 20

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 1

LOGIC GND = Pin 6

BUS GND = Pin 13, 16, 19

BG GND = Pin 20

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	High-level output voltage			4.5	V
V_{TH}	Receiver input threshold	1.475	1.55	1.625	V
I_{OL}	Low-level output current			20	mA
C_{IN}	Bus-port capacitance at $I/O_n=V_T=2V$			7	pF
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
I_{OH}	High-level output current	I/O_n(Power on)	V_{CC}=MIN, V_{IL} = MAX, V_{IH} =MIN, V_{OH} = MAX			10	100	μA
		I/O_n(Power off)	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} =MIN, V_{OH} = MAX				100	μA
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL}= MAX, I_{OH} = MAX		2.5			V
V_{OL}	Low-level output voltage	R_n	V_{CC} = MIN, V_{IN} = 2.4V, R_T=10Ω. V_T=2V	± 5%V_{CC}		0.35	0.5	V
		I/O_n	V_{CC} = MIN,V_{IH} = MIN, I_{OL} = 20mA	± 5%V_{CC}			1.2	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				40	μA
I_{IL}	Low-level input current	D_n , $\overline{RE}$	V_{CC} = MAX, V_I = 0.0V				-100	μA
		DE	V_{CC} = MAX, V_I = 0.0V				-400	μA
$I_{OZH} + I_{IH}$	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O =2.7V				50	μA
$I_{OZL} + I_{IL}$	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O =0.5V				-50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX				-200	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			70		mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

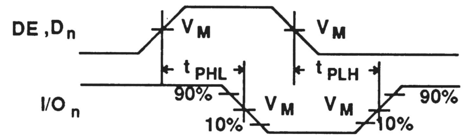
SYMBOL	PARAMETER	TEST CONDITION	Driver LIMITS					UNIT
			T_A = +25°C V_{CC}= 5V, V_T=2V C_L = 30pF R_T = 10Ω			T_A = 0°C to +70°C V_{CC}= 5V ±5%, V_T=2V C_L = 30pF R_T= 10Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to I/O_n	Waveform 1		3.5 3.5		2.0 2.0	7.0 7.0	ns
t_{TLH} t_{THL}	Transition time 10% to 90%, 90% to 10%	Waveform 1				1.0 1.0	5.0 5.0	ns
	Skew between Drivers in same package	Waveform 1					1.0	ns

SYMBOL	PARAMETER	TEST CONDITION	Driver Enable LIMITS					UNIT
			T_A = +25°C V_{CC}= 5V, V_T=2V C_L = 50pF			T_A = 0°C to +70°C V_{CC}= 5V ±5%, V_T=2V C_L = 50pF		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay DE to I/O_n	Waveform 1		3.5 3.5		2.0 2.0	7.0 7.0	ns

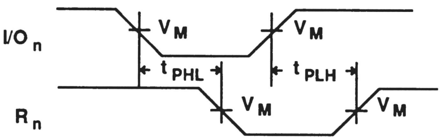
SYMBOL	PARAMETER	TEST CONDITION	Receiver LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF			T_A = 0°C to +70°C V_{CC} = 5V ±5% C_L = 50pF		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I/O_n to R_n	Waveform 2		3.5 3.5		2.0 2.0	8.0 8.0	ns
	Skew between Receivers in same package						1.0	ns

SYMBOL	PARAMETER	TEST CONDITION	Receiver Enable LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 5pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±5% C_L = 5pF R_L= 500Ω		
			Min	Typ	Max	Min	Max	
t_{PZH} t_{PZL}	Output Enable time to High or Low $\overline{RE}$ to R_n	Waveform 3 Waveform 4		10.0 9.0			12.0 12.0	ns
t_{PHZ} t_{PLZ}	Output Disable time fromHigh or Low $\overline{RE}$ to R_n	Waveform 3 Waveform 4		4.0 4.0			6.0 6.0	ns

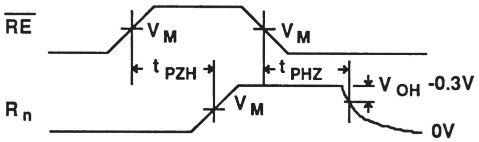
AC WAVEFORMS


DE ,D_n
V_M
V_M
t_{PHL}
t_{PLH}
I/O $_n$
90%
10%
V_M
V_M
90%
10%

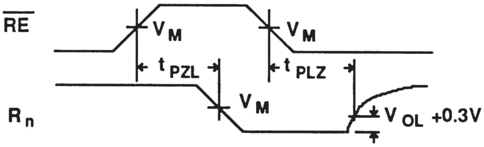
Waveform 1. Propagation Delay For Driver


I/O $_n$
V_M
V_M
t_{PHL}
t_{PLH}
R_n
V_M
V_M

Waveform 2. Propagation Delay For Receiver


$\overline{RE}$
V_M
V_M
t_{PZH}
t_{PHZ}
V_{OH} -0.3V
R_n
V_M
0V

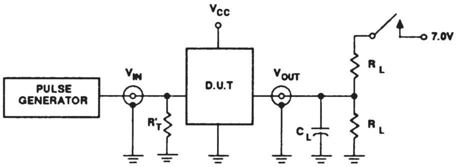
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level


$\overline{RE}$
V_M
V_M
t_{PZL}
t_{PLZ}
R_n
V_M
V_{OL} +0.3V

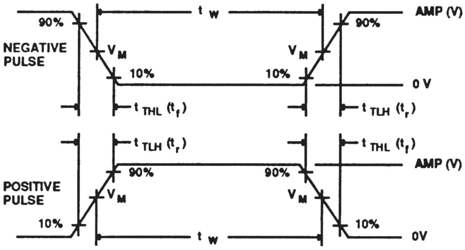
Waveform 4 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
7.0V
R_L
PULSE GENERATOR
V_{IN}
D.U.T
V_{OUT}
R'_T
C_L
R_L

Test Circuit For 3-State Outputs

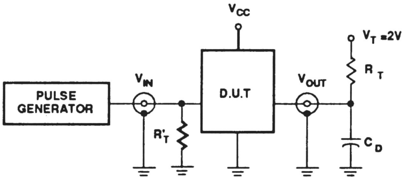

t_w
AMP (V)
90%
90%
NEGATIVE PULSE
V_M
V_M
10%
10%
0 V
t_{THL} (t_f)
t_{TLH} (t_r)
t_{TLH} (t_r)
t_{THL} (t_f)
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
t_w
0V

V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open


V_{CC}
V_T =2V
R_T
PULSE GENERATOR
V_{IN}
D.U.T
V_{OUT}
R'_T
C_D

Test Circuit For Open Collector Outputs

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistor; see AC CHARACTERISTICS for value.

FAST 74F8960, 74F8961

Futurebus Transceivers

Preliminary Specification **for**
74F8960-Octal Latched Bidirectional Future Transceiver, INV (OC)
Product Specification **for**
74F8961-Octal Latched Bidirectional Future Transceiver, NINV (OC)

FEATURES

- **Octal Latched Transceiver**
- **Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms**
- **High drive (100mA) open collector drivers on B-port**
- **Reduced voltage swing (1 volt) produces less noise and reduces power consumption**
- **High speed operation enhances performance of backplane buses and facilitates incident wave switching**
- **Compatible with IEEE 896 Futurebus Standard**
- **Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity**
- **Controlled output ramp and multiple GND pins minimize ground bounce**
- **Glitch-free power up / power down operation**

TYPE	TYPICAL PROPAGATION DELAY	MAX SUPPLY CURRENT (TOTAL)
74F8960	7.5ns	85mA
74F8961	7.5ns	85mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP (600 mil)[1]	N74F8960N, N74F8961N
28-Pin PLCC[1]	N74F8960A, N74F8961A

NOTE:
1. Thermal mounting techniques are recommended. See SMD Process ASpllications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	PNP latched inputs	3.5/0.0117	70μA/70μA
B_0 - B_7	Data inputs with threshold circuitry	5.0/0.167	100μA/100μA
OEA	A Output Enable input (active High)	1.0/0.033	20μA/20μA
$\overline{OEB}_0$, $\overline{OEB}_1$	B Output Enable inputs (active Low)	1.0//0.033	20μA/20μA
$\overline{LE}$	Latch Enable input (active Low)	1.0//0.033	20μA/20μA
A_0 - A_7	3-State outputs	150/40	3mA/24mA
B_0 - B_7	Open Collector outputs	OC*/166.7	OC*/100mA

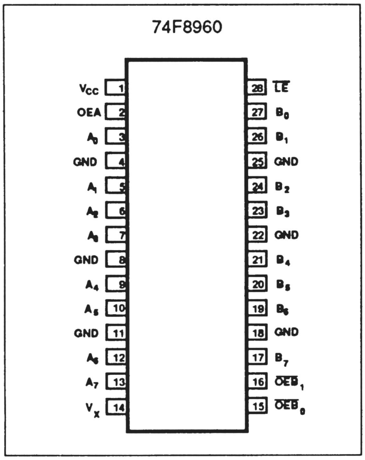
NOTES:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
* OC = Open Collector

DESCRIPTION

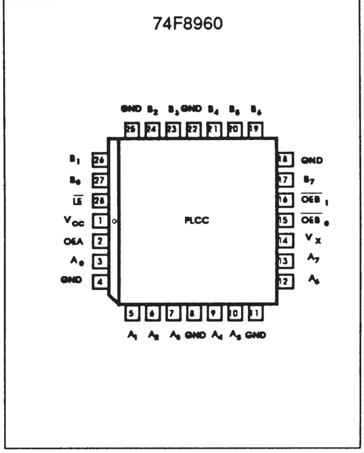
The 74F8960 and 74F8961 are octal bidirectional latched transceivers and are intended to provide the electrical interface to a high performance wired-OR bus. The B port inverting drivers are low-capacitance open collector with controlled ramp and are designed to sink 100 mA from 2 volts. The B port receivers have a 100 mV threshold region and a 4 ns glitch filter.

The B port interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading (<5 pF).

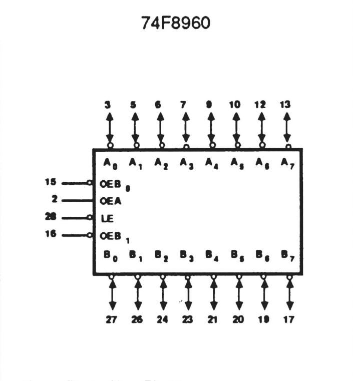
PIN CONFIGURATION DIP


74F8960
V_{CC} 1
OEA 2
A_0 3
GND 4
A_1 5
A_2 6
A_3 7
GND 8
A_4 9
A_5 10
GND 11
A_6 12
A_7 13
V_X 14
28 $\overline{LE}$
27 B_0
26 B_1
25 GND
24 B_2
23 B_3
22 GND
21 B_4
20 B_5
19 B_6
18 GND
17 B_7
16 $\overline{OEB}_1$
15 $\overline{OEB}_0$

PIN CONFIGURATION PLCC


74F8960
GND B_2 B_3 GND B_4 B_5 B_6
25 24 23 22 21 20 19
B_1 26
B_0 27
$\overline{LE}$ 28
V_{CC} 1
OEA 2
A_0 3
GND 4
18 GND
17 B_7
16 $\overline{OEB}_1$
15 $\overline{OEB}_0$
14 V_X
13 A_7
12 A_6
PLCC
5 6 7 8 9 10 11
A_1 A_2 A_3 GND A_4 A_5 GND

LOGIC SYMBOL


74F8960
3 5 6 7 9 10 12 13
A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7
15 OEB_0
2 OEA
28 LE
16 OEB_1
B_0 B_1 B_2 B_3 B_4 B_5 B_6 B_7
27 26 24 23 21 20 19 17

V_{CC} = Pin 1 V_X = Pin 14
GND = Pin 4, 8, 11, 18, 22, 25

DESCRIPTION (Continued)

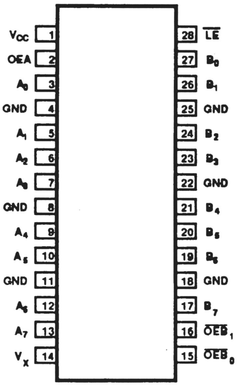
Incident wave switching is employed, therefore BTL propagation delays are short. Although the voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane. The 74F8960A and 74F8961A ports have TTL 3-State drivers and TTL receivers with a latch function. A separate High level control input (V_X) is provided to limit the A port output level to a given voltage level (such as 3.3V). For 5.0V systems, V_x is simply tied to V_{CC}.

74F8961 is the non-inverting version of 74F8960.

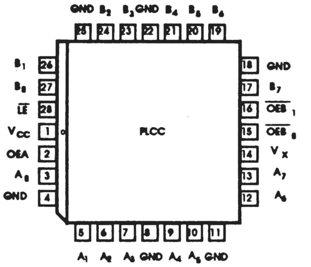
PIN CONFIGURATION

74F8961


V_{CC} 1
OEA 2
A_0 3
GND 4
A_1 5
A_2 6
A_3 7
GND 8
A_4 9
A_5 10
GND 11
A_6 12
A_7 13
V_X 14
28 $\overline{LE}$
27 B_0
26 B_1
25 GND
24 B_2
23 B_3
22 GND
21 B_4
20 B_5
19 B_6
18 GND
17 B_7
16 $\overline{OEB}_1$
15 $\overline{OEB}_0$

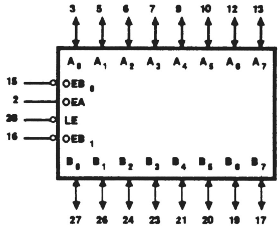
PIN CONFIGURATION PLCC

74F8961


GND 25
B_2 24
B_3 23
GND 22
B_4 21
B_5 20
B_6 19
B_1 26
B_0 27
$\overline{LE}$ 28
V_{CC} 1
OEA 2
A_0 3
GND 4
PLCC
18 GND
17 B_7
16 $\overline{OEB}_1$
15 $\overline{OEB}_0$
14 V_X
13 A_7
12 A_6
5 A_1
6 A_2
7 A_3
8 GND
9 A_4
10 A_5
11 GND

LOGIC SYMBOL

74F8961

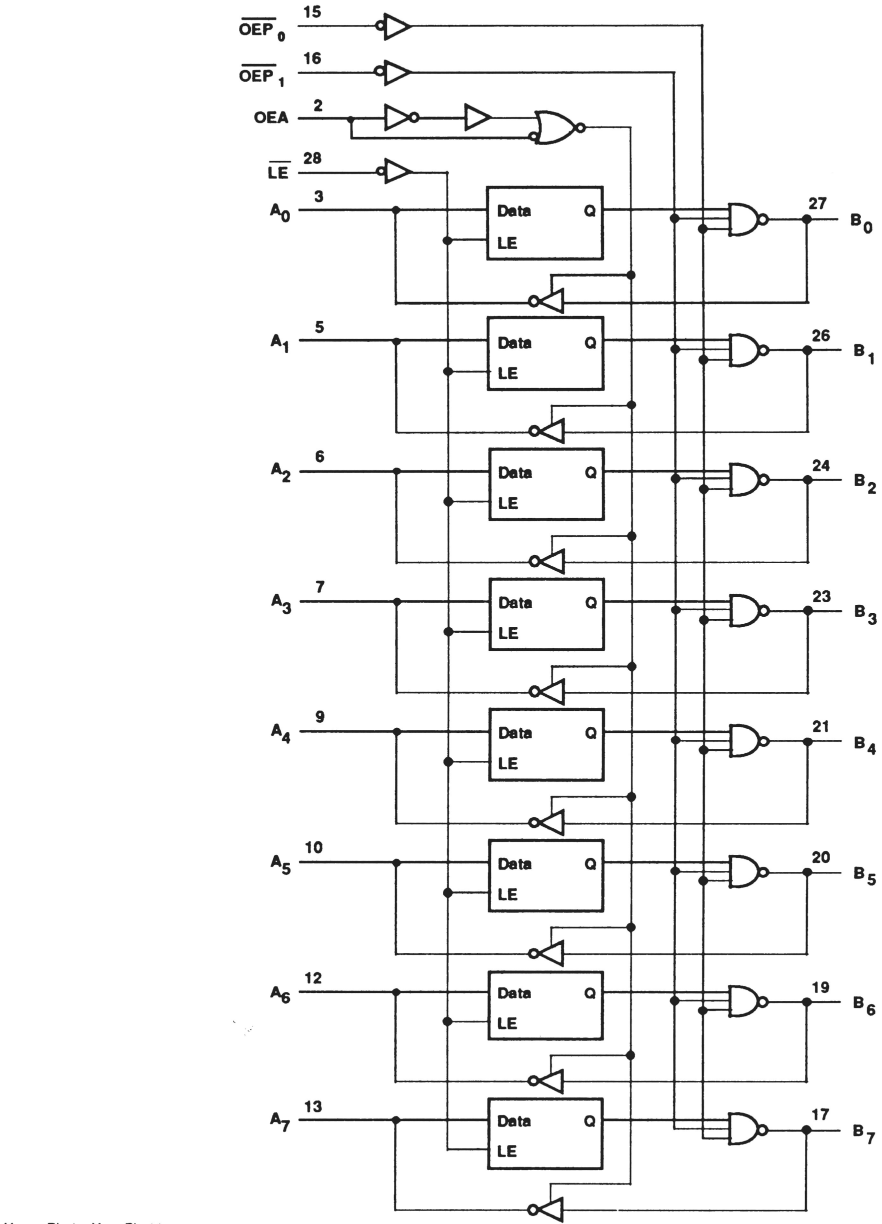

3
5
6
7
9
10
12
13
A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7
15 OEB_0
2 OEA
28 LE
16 OEB_1
B_0 B_1 B_2 B_3 B_4 B_5 B_6 B_7
27
26
24
23
21
20
19
17

V_{CC} = Pin 1 V_X = Pin 14
GND = Pin 4, 8, 11, 18, 22, 25

PIN DESCRIPTION

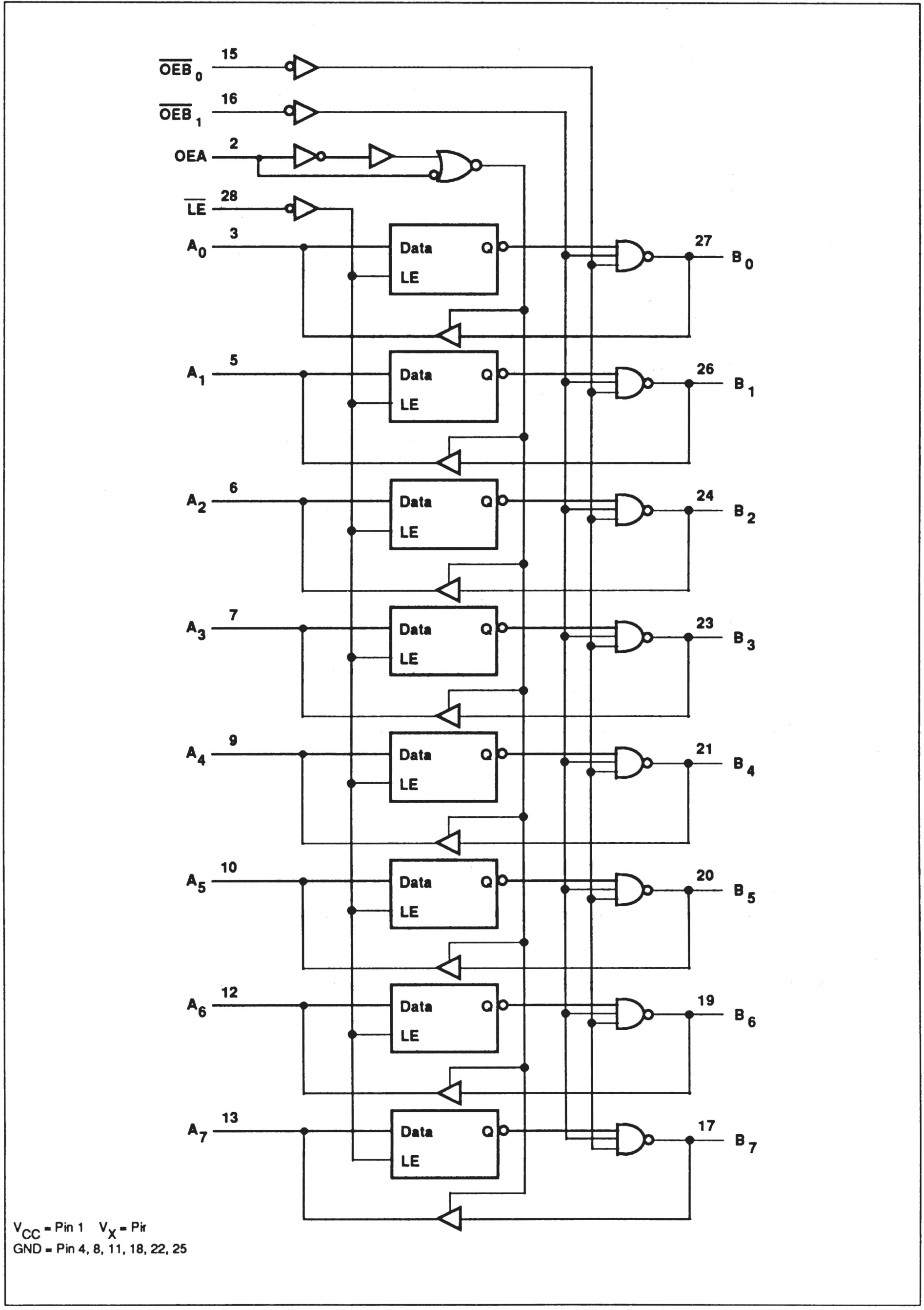
SYMBOL	PINS	TYPE	NAME AND FUNCTION
A_0	3	I/O	PNP latched input / 3-state output (with V_X control option)
A_1	5	I/O	
A_2	6	I/O	
A_3	7	I/O	
A_4	9	I/O	
A_5	10	I/O	
A_6	12	I/O	
A_7	13	I/O	
B_0	27	I/O	Data input with special threshold circuitry to reject noise / Open Collector output, High current drive
B_1	26	I/O	
B_2	24	I/O	
B_3	23	I/O	
B_4	21	I/O	
B_5	20	I/O	
B_6	19	I/O	
B_7	17	I/O	
$\overline{OEB}_0$	15	I	Enables the B outputs when both pins are Low
$\overline{OEB}_1$	16	I	
OEA	2	I	Enables the A outputs when High
$\overline{LE}$	28	I	Latched when High (a special delay feature is built in for proper enabling times)
V_X	14	I	Clamping voltage keeping V_{OH} from rising above V_X ($V_X = V_{CC}$ for normal use)

LOGIC DIAGRAM, 74F8960


$\overline{OEP}_0$
15
$\overline{OEP}_1$
16
OEA
2
$\overline{LE}$
28
A_0 3
A_1 5
A_2 6
A_3 7
A_4 9
A_5 10
A_6 12
A_7 13
Data
Q
LE
27 B_0
26 B_1
24 B_2
23 B_3
21 B_4
20 B_5
19 B_6
17 B_7

V_{CC} = Pin 1 V_X = Pin 14
GND = Pin 4, 8, 11, 18, 22, 25

LOGIC DIAGRAM, 74F8961


$\overline{OEB}_0$
15
$\overline{OEB}_1$
16
OEA
2
$\overline{LE}$
28
A_0
3
A_1
5
A_2
6
A_3
7
A_4
9
A_5
10
A_6
12
A_7
13
Data
LE
Q
27
B_0
26
B_1
24
B_2
23
B_3
21
B_4
20
B_5
19
B_6
17
B_7

V_{CC} = Pin 1 V_X = Pir
GND = Pin 4, 8, 11, 18, 22, 25

FUNCTION TABLE, 74F8960

INPUTS						LATCH	OUTPUTS		MODE
A_n	B_n^*	$\overline{LE}$	OEA	$\overline{OEB}_0$	$\overline{OEB}_1$	STATE	A_n	B_n	
H	X	L	L	L	L	H	Z	L	A 3-state, Data from A to B
L	X	L	L	L	L	L	Z	H^{**}	
X	X	H	L	L	L	Q_n	Z	$\overline{Q}_n$	A 3-state, Latched data to B
–	–	L	H	L	L	(1)	(1)	(1)	Feedback: A to B, B to A
–	H	H	H	L	L	$L^{(2)}$	L	$Z^{(2)}$	Preconditioned Latch enabling data transfer from B to A
–	L	H	H	L	L	$L^{(2)}$	H	$Z^{(2)}$	
–	–	H	H	L	L	Q_n	$\overline{Q}_n$	$\overline{Q}_n$	Latch state to A and B
H	X	L	L	H	X	H	Z	Z	B and A 3-state
L	X	L	L	H	X	L	Z	Z	
X	X	H	L	H	X	Q_n	Z	Z	
–	H	L	H	H	X	H	L	Z	B 3-state, Data from B to A
–	L	L	H	H	X	L	H	Z	
–	H	H	H	H	X	Q_n	L	Z	
–	L	H	H	H	X	Q_n	H	Z	
H	X	L	L	X	H	H	Z	Z	B and A 3-state
L	X	L	L	X	H	L	Z	Z	
X	X	H	L	X	H	Q_n	Z	Z	
–	H	L	H	X	H	H	L	Z	B 3-state, Data from B to A
–	L	L	H	X	H	L	H	Z	
–	H	H	H	X	H	Q_n	L	Z	
–	L	H	H	X	H	Q_n	H	Z	

H = High voltage level
L = Low voltage level
X = Don't care
– = Input not externally driven
Z = High Impedance (off) state
Q_n = High or Low voltage level one setup time prior to the Low-to-High $\overline{LE}$ transition
(1) = Condition will cause a feedback loop path; A to B and B to A
(2) = The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB}_0$ and $\overline{OEB}_1$ are Low and $\overline{LE}$ is High.
H* = Goes to level of pullup voltage.
B* = Precaution should be taken to insure B inputs do not float. If they do they are equal to Low state.

FUNCTION TABLE. 74F8961

INPUTS						LATCH	OUTPUTS		MODE
A_n	B_n*	$\overline{LE}$	OEA	$\overline{OEB_0}$	$\overline{OEB_1}$	STATE	A_n	B_n	
H	X	L	L	L	L	H	Z	H**	A 3-state, Data from A to B
L	X	L	L	L	L	L	Z	L	
X	X	H	L	L	L	Q_n	Z	Q_n	A 3-state, Latched data to B
–	–	L	H	L	L	(1)	(1)	(1)	Feedback: A to B, B to A
–	H	H	H	L	L	$H^{(2)}$	H	$Z^{(2)}$	Preconditioned Latch enabling data transfer from B to A
–	L	H	H	L	L	$H^{(2)}$	L	$Z^{(2)}$	
–	–	H	H	L	L	Q_n	Q_n	Q_n	Latch state to A and B
H	X	L	L	H	X	H	Z	Z	B and A 3-state
L	X	L	L	H	X	L	Z	Z	
X	X	H	L	H	X	Q_n	Z	Z	
–	H	L	H	H	X	H	H	Z	B 3-state, Data from B to A
–	L	L	H	H	X	L	L	Z	
–	H	H	H	H	X	Q_n	H	Z	
–	L	H	H	H	X	Q_n	L	Z	
H	X	L	L	X	H	H	Z	Z	B and A 3-state
L	X	L	L	X	H	L	Z	Z	
X	X	H	L	X	H	Q_n	Z	Z	
–	H	L	H	X	H	H	H	Z	B 3-state, Data from B to A
–	L	L	H	X	H	L	L	Z	
–	H	H	H	X	H	Q_n	H	Z	
–	L	H	H	X	H	Q_n	L	Z	

H = High voltage level
L = Low voltage level
X = Don't care
– = Input not externally driven
Z = High Impedance (off) state
Q_n = High or Low voltage level one setup time prior to the Low-to-High $\overline{LE}$ transition
(1) = Condition will cause a feedback loop path; A to B and B to A
(2) = The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB_0}$ and $\overline{OEB_1}$ are Low and $\overline{LE}$ is High.
H* = Goes to level of pullup voltage.
B* = Precaution should be taken to insure B inputs do not float. If they do they are equal to Low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_X	Threshold control		-0.5 to +7.0	V
V_{IN}	Input voltage	$\overline{OEB}_n$, OEA, $\overline{LE}$	-0.5 to +7.0	V
		A_0 - A_7, B_0 - B_7	-0.5 to 5.5	
I_{IN}	Input current		-40 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	A_0 - A_7	48	mA
		B_0 - B_7	200	
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage	Except B_0 - B_7	2.0			V
		B_0 - B_7	1.8			
V_{IL}	Low-level input voltage	Except B_0 - B_7			0.8	V
		B_0 - B_7			1.45	
I_{IK}	Input clamp current	Except A_0 - A_7			-18	mA
		A_0 - A_7			-40	
I_{OH}	High-level output current	A_0 - A_7			-3	mA
I_{OL}	Low-level output current	A_0 -A_7			24	mA
		B_0 - B_7			100	
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
I_{OH}	High level output current	B_0 - B_7	V_{CC} = MAX, V_{IL} =MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
I_{OFF}	Power-off output current	B_0 - B_7	V_{CC} = 0.0V, V_{IL} =MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
V_{OH}	High-level output voltage	A_0 - A_7[4]	V_{CC} = MIN, V_{IL}= MAX, V_{IH} = MIN	I_{OH} = -3mA, V_X = V_{CC}	2.5		V_{CC}	V
				I_{OH} = -0.4mA, V_X = 3.13V & 3.47V	2.5		V_X	V
V_{OL}	Low-level output voltage	A_0 - A_7[4]	V_{CC} = MIN, V_{IL}= MAX, V_{IH} = MIN	I_{OL} = 20mA, V_X = V_{CC}			0.5	V
		B_0 - B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA			1.15	V
				I_{OL} = 4mA	0.40			V
V_{IK}	Input clamp voltage	A_0 - A_7	V_{CC} = MIN, I_I = I_{IK}				-0.5	V
		Except A_0 - A_7	V_{CC} = MIN, I_I = I_{IK}				-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEB}_n$, OEA, $\overline{LE}$	V_{CC} = 0.0V, V_I = 7.0V				100	µA
		A_0 - A_7, B_0 - B_7	V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High-level input current	$\overline{OEB}_n$, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 2.7V, B_n - A_n = 0V				20	µA
		B_0 - B_7	V_{CC} = MAX, V_I = 2.1V				100	µA
I_{IL}	Low-level input current	$\overline{OEB}_n$, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 0.5V				-20	µA
		B_0 - B_7	V_{CC} = MAX, V_I = 0.3V				-100	µA
I_{OZH} + I_{IH}	Off-state output current, High-level voltage applied	A_0 - A_7	V_{CC} = MAX, V_O =2.7V				70	µA
I_{OZL} + I_{IL}	Off-state output current, Low-level voltage applied	A_0 - A_7	V_{CC} = MAX, V_O =0.5V				-70	µA
I_X	High-level control current		V_{CC} = MAX, V_X = V_{CC}, $\overline{LE}$ = OEA = $\overline{OEB}_n$ = 2.7V, A_0 - A_7 = 2.7V, B_0 - B_7 = 2.0V		-100		100	µA
			V_{CC} = MAX, V_X = 3.13V & 3.47 V, $\overline{LE}$ = OEA = 2.7V, $\overline{OEB}_n$ =A_0 - A_7 = 2.7V, B_0 - B_7 = 2.0V		-10		10	mA
I_{OS}	Short-circuit output current[3]	A_0 - A_7 only	V_{CC} = MAX, B_n = 1.6V, OEA = 2.0V, $\overline{OEB}_n$ = 2.7V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			70	100	mA
		I_{CCL}	V_{CC} = MAX, V_{IL} = 0.5V			100	145	mA
		I_{CCZ}	V_{CC} = MAX, V_{IL} = 0.5V			80	100	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. Unless otherwise specified, V_X = V_{CC} for all test conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH}=1.6V and V_{IL}=1.3V.

AC ELECTRICAL CHARACTERISTICS for 74F8960

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay B to A	Waveform 1, 2	5.5 6.0	7.5 7.5	12.0 10.5	5.0 6.0	12.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable time from High or Low OEA to A	Waveform 4.5	8.0 8.5	10.5 12.0	14.5 14.5	7.5 8.5	15.5 17.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low OEA to A	Waveform 4.5	2.0 2.0	4.5 4.5	7.0 7.5	2.0 2.0	7.5 8.0	ns

SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_D = 30pF R_U = 9Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_D = 30pF R_U = 9Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A to B	Waveform 1, 2	2.0 3.5	4.0 6.0	7.0 8.0	2.0 3.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to B	Waveform 1, 2	3.0 4.0	5.0 6.0	8.5 9.0	2.5 3.0	10.0 9.5	ns
t_{PLH} t_{PHL}	Enable/disable time $\overline{OEB}_n$ to B	Waveform 1, 2	2.5 4.5	4.5 7.5	7.5 10.5	1.5 3.5	8.5 10.5	ns
t_{TLH} t_{THL}	Transition time, B Port 1.3V to 1.7 V, 1.7V to 1.3V	Test Circuit and Waveforms	0.5 0.5	2.0 2.0	4.5 4.5	0.5 0.5	4.5 4.5	ns

AC SETUP REQUIREMENTS for 74F8960

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time A to $\overline{LE}$	Waveform 3	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time A to $\overline{LE}$	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_w(L)$	$\overline{LE}$ Pulse width, Low	Waveform 3	6.0			6.0		ns

AC ELECTRICAL CHARACTERISTICS for 74F8961

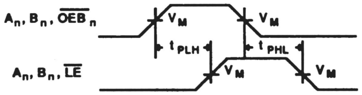
SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay B to A	Waveform 1, 2	5.5	7.5	12.0	5.0	12.0	ns
t_{PHL}			6.0	7.5	10.5	6.0	11.0	
t_{PZH}	Output Enable time from High or Low OEA to A	Waveform 4.5	8.0	10.5	14.5	7.5	15.5	ns
t_{PZL}			8.5	12.0	14.5	8.5	17.0	
t_{PHZ}	Output Disable time to High or Low OEA to A	Waveform 4.5	2.0	4.5	7.0	2.0	7.5	ns
t_{PLZ}			2.0	4.5	7.5	2.0	8.0	

SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_D = 30pF R_U = 9Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_D = 30pF R_U = 9Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay A to B	Waveform 1, 2	2.0	4.0	7.0	2.0	8.0	ns
t_{PHL}			3.5	6.0	8.0	3.0	9.0	
t_{PLH}	Propagation delay $\overline{LE}$ to B	Waveform 1, 2	3.0	5.0	8.5	2.5	10.0	ns
t_{PHL}			4.0	6.0	9.0	3.0	9.5	
t_{PLH}	Enable/disable time $\overline{OEB}_n$ to B	Waveform 1, 2	2.5	4.5	7.5	1.5	8.5	ns
t_{PHL}			4.5	7.5	10.5	3.5	10.5	
t_{TLH}	Transition time, B Port 1.3V to 1.7 V, 1.7V to 1.3V	Test Circuit and Waveforms	0.5	2.0	4.5	0.5	4.5	ns
t_{THL}			0.5	2.0	4.5	0.5	4.5	

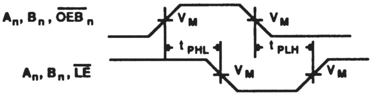
AC SETUP REQUIREMENTS for 74F8961

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$	Set-up time A to $\overline{LE}$	Waveform 3	5.0			5.0		ns
$t_s(L)$			5.0			5.0		
$t_h(H)$	Hold time A to $\overline{LE}$	Waveform 3	0.0			0.0		ns
$t_h(L)$			0.0			0.0		
$t_w(L)$	$\overline{LE}$ Pulse width, Low	Waveform 3	6.0			6.0		ns

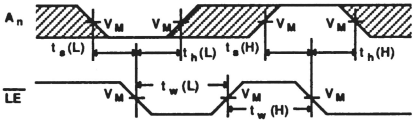
AC WAVEFORMS


A_n, B_n, $\overline{OEB}_n$
V_M
V_M
t_{PLH}
t_{PHL}
A_n, B_n, $\overline{LE}$
V_M
V_M

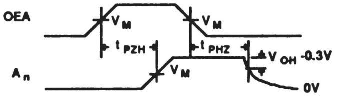
Waveform 1. Propagation Delay For Data To Output


A_n, B_n, $\overline{OEB}_n$
V_M
V_M
t_{PHL}
t_{PLH}
A_n, B_n, $\overline{LE}$
V_M
V_M

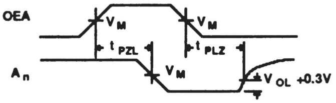
Waveform 2. Propagation Delay For Data To Output


A_n
V_M
V_M
V_M
V_M
$t_s(L)$
$t_h(L)$
$t_s(H)$
$t_h(H)$
$\overline{LE}$
V_M
$t_w(L)$
V_M
$t_w(H)$
V_M

Waveform 3. Data Setup And Hold Times And $\overline{LE}$ Pulse Widths


OEA
V_M
V_M
t_{PZH}
t_{PHZ}
V_{OH} -0.3V
A_n
V_M
0V

Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level

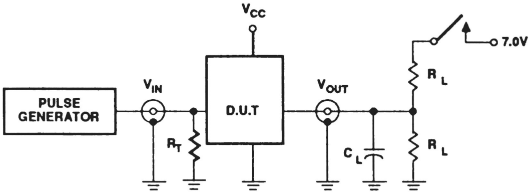

OEA
V_M
V_M
t_{PZL}
t_{PLZ}
A_n
V_M
V_{OL} +0.3V

Waveform 5 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

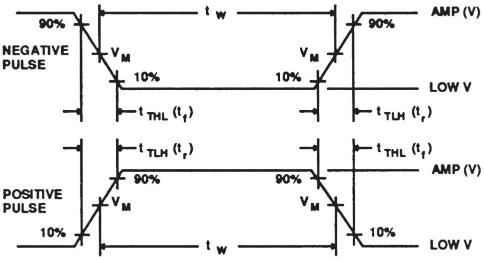
NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
7.0V
R_L
PULSE GENERATOR
V_{IN}
D.U.T
V_{OUT}
R_T
C_L
R_L

Test Circuit For 3-State Outputs On A Port

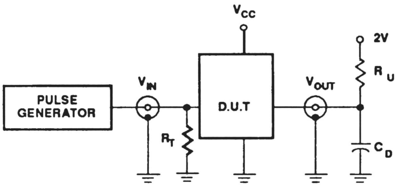

t_W
AMP (V)
90%
90%
NEGATIVE PULSE
V_M
V_M
10%
10%
LOW V
t_{THL} (t_f)
t_{TLH} (t_r)
t_{TLH} (t_r)
t_{THL} (t_f)
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
t_W
LOW V

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open


V_{CC}
2V
R_U
PULSE GENERATOR
V_{IN}
D.U.T
V_{OUT}
R_T
C_D

Test Circuit For Outputs On B Port

FAMILY 74F	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_U = Pull up resistor; see AC CHARACTERISTICS for value.

FAST 74F11240, 74F11244
Buffers

74F11240 Octal Inverter Buffer (3-State)
74F11244 Octal Buffer (3-State)
Preliminary Specification

FEATURES

- **Same function as 'F240 and 'F244but with ACL compatible pinout**
- **Light loading input structure reduces bus loading (20µA in High and Low states)**
- **Multiple, centered V_{CC} and GND pins minimize package inductance and reduced ground bounce**
- **Controlled output ramp minimizes ground bounce**
- **High internal speed provides performance upgrade over 'F240 and 'F244 while consuming less power**
- **Flow through pinout structure simplifies PC board design-Octal bus interface**
- **3-State buffer outputs sink 64mA and source 15mA**

DESCRIPTION

The 74F11240 and 74F11244 are functionally equivalent to the 74F240 and 74F244. However, the pinout of the 74F11240 and 74F11244 differs from the 74F240 and 74F244 in that additional centered V_{CC} and GND pins have been added to minimize the effects of package inductance. These pinouts are compatible with the ACL standard pinouts.The 74F11240 and 74F11244 also feature a light loading input structure, a controlled output ramp to minimize ground bounce and high performance A/C characteristics which provide an upgrade to existing 74F240 and 74F244.

The 74F11240 and 74F11244 are octal buffers that are ideal for driving bus lines of buffer memory address registers. The outputs are all capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}$, each controlling four of the 3-state outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F11240	5.0ns	46mA
74F11244	5.0ns	46mA

ORDERING INFORMATION

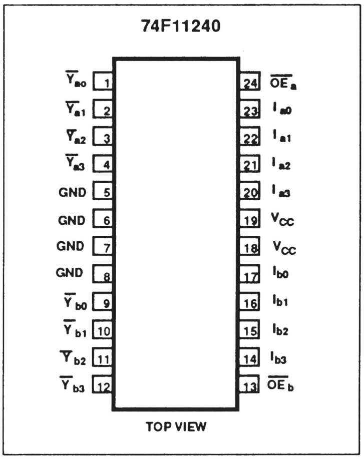
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic SLIM DIP (300mil)	N74F11240N, N74F11244N
24-Pin Plastic SOL	N74F11240D, N74F11244D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

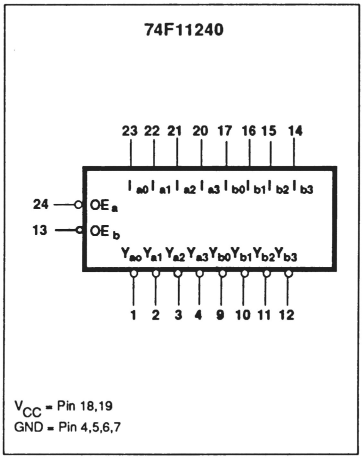
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{an}, I_{bn}	Data inputs	1.0/0.033	20µA/20µA
I_{an}, I_{bn}	Data inputs	1.0/0.033	20µA/20µA
$\overline{OE}_a$ $\overline{OE}_b$	Output enable input (active Low)	1.0/0.033	20µA/20µA
Y_{an}, Y_{bn}	Data outputs ('F244)	750/106.7	15mA/64mA
$\overline{Y}_{an}$, $\overline{Y}_{bn}$	Data outputs ('F240)	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

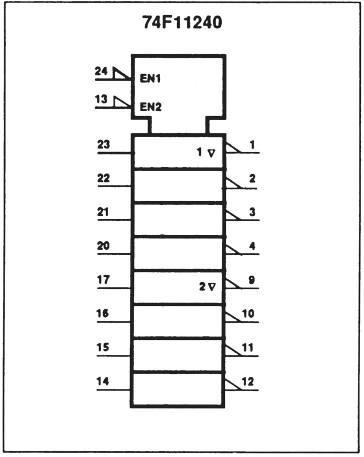
PIN CONFIGURATION


74F11240
$\overline{Y}_{a0}$ 1
$\overline{Y}_{a1}$ 2
$\overline{Y}_{a2}$ 3
$\overline{Y}_{a3}$ 4
GND 5
GND 6
GND 7
GND 8
$\overline{Y}_{b0}$ 9
$\overline{Y}_{b1}$ 10
$\overline{Y}_{b2}$ 11
$\overline{Y}_{b3}$ 12
24 $\overline{OE}_a$
23 I_{a0}
22 I_{a1}
21 I_{a2}
20 I_{a3}
19 V_{CC}
18 V_{CC}
17 I_{b0}
16 I_{b1}
15 I_{b2}
14 I_{b3}
13 $\overline{OE}_b$
TOP VIEW

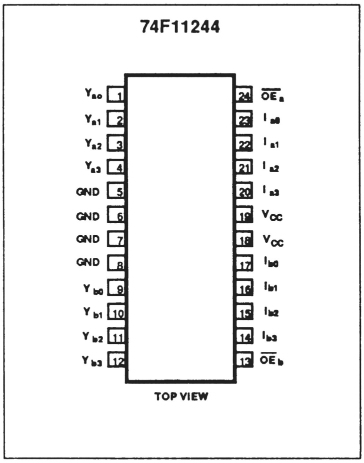
LOGIC SYMBOL


74F11240
23 22 21 20 17 16 15 14
I_{a0} I_{a1} I_{a2} I_{a3} I_{b0} I_{b1} I_{b2} I_{b3}
24 OE_a
13 OE_b
Y_{a0} Y_{a1} Y_{a2} Y_{a3} Y_{b0} Y_{b1} Y_{b2} Y_{b3}
1 2 3 4 9 10 11 12
V_{CC} = Pin 18,19
GND = Pin 4,5,6,7

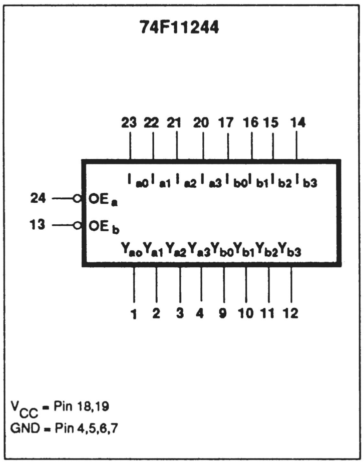
LOGIC SYMBOL(IEEE/IEC)


74F11240
24 EN1
13 EN2
23 1 ▽ 1
22 2
21 3
20 4
17 2 ▽ 9
16 10
15 11
14 12

PIN CONFIGURATION

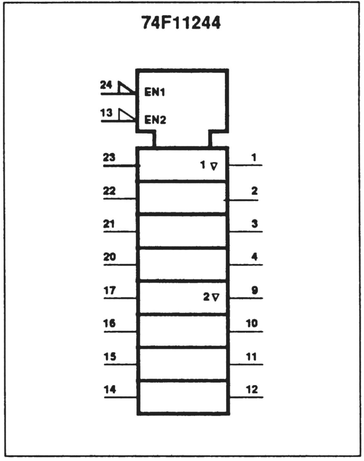

74F11244
Y_a0 1
Y_a1 2
Y_a2 3
Y_a3 4
GND 5
GND 6
GND 7
GND 8
Y_b0 9
Y_b1 10
Y_b2 11
Y_b3 12
24 OE_a
23 I_a0
22 I_a1
21 I_a2
20 I_a3
19 V_CC
18 V_CC
17 I_b0
16 I_b1
15 I_b2
14 I_b3
13 OE_b
TOP VIEW

LOGIC SYMBOL

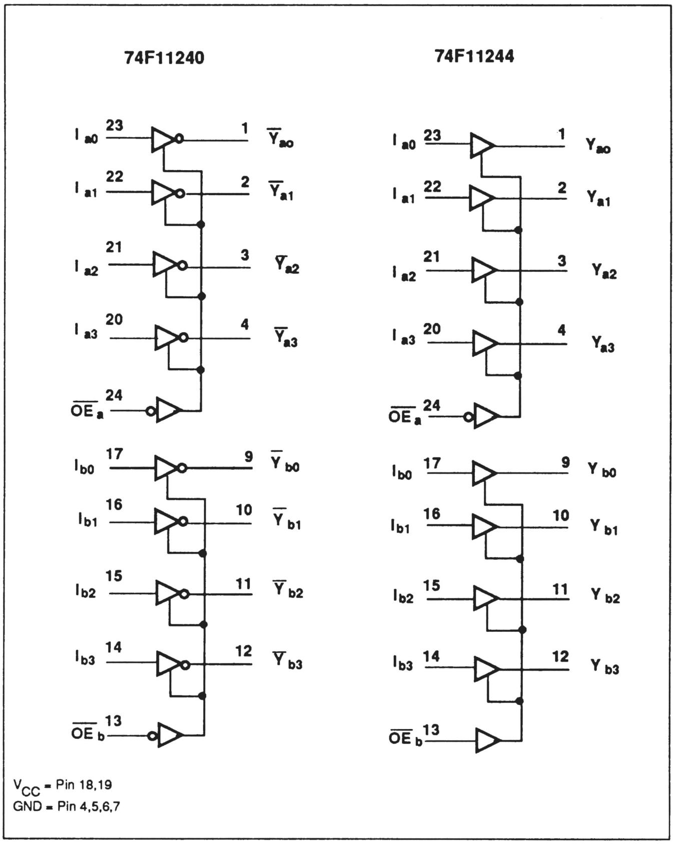

74F11244
23 22 21 20 17 16 15 14
I_a0 I_a1 I_a2 I_a3 I_b0 I_b1 I_b2 I_b3
24 OE_a
13 OE_b
Y_a0 Y_a1 Y_a2 Y_a3 Y_b0 Y_b1 Y_b2 Y_b3
1 2 3 4 9 10 11 12

V_{CC} = Pin 18,19
GND = Pin 4,5,6,7

LOGIC SYMBOL(IEEE/IEC)


74F11244
24
13
EN1
EN2
23
22
21
20
17
16
15
14
1▽
2▽
1
2
3
4
9
10
11
12

LOGIC DIAGRAM,


74F11240
74F11244
I_a0 23
1 Y_a0
I_a1 22
2 Y_a1
I_a2 21
3 Y_a2
I_a3 20
4 Y_a3
OE_a 24
I_b0 17
9 Y_b0
I_b1 16
10 Y_b1
I_b2 15
11 Y_b2
I_b3 14
12 Y_b3
OE_b 13

V_{CC} = Pin 18,19
GND = Pin 4,5,6,7

FUNCTION TABLE, 74F11240

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_a$	$\overline{Y}_b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

FUNCTION TABLE, 74F11244

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.8			V
					±5%V_{CC}	2.9	3.5		V
				I_{OH}=-15mA	±10%V_{CC}	2.6			V
					±5%V_{CC}	2.8			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=48mA	±10%V_{CC}		0.35	0.37	V
				I_{OL}=64mA	±5%V_{CC}		0.38	0.38	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	$\overline{OE}_a$, $\overline{OE}_b$	V_{CC} = MAX, V_I = 0.5V					-20	μA
		I_{an}, I_{bn}						-40	μA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					50	μA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-55		-132	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				46	47	mA
		I_{CCL}					45	45	mA
		I_{CCZ}					46	47	mA

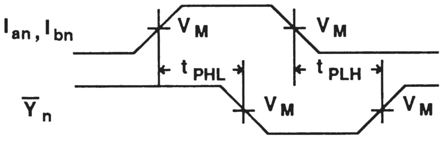
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

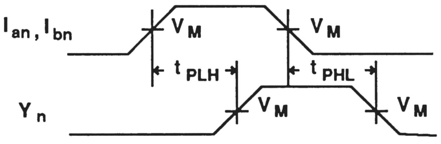
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to $\overline{Y}_n$	74F11240	Waveform 1	3.0 2.0	5.0 4.9	6.5 4.5	3.0 3.0	6.0 5.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	3.0 4.5	4.8 6.2	7.5 8.5	3.0 4.0	6.0 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 3 Waveform 4	3.0 3.0	3.3 2.9	7.0 7.0	2.0 2.0	6.0 6.0	ns
t_{TLH} t_{THL}	Transition time 10% to 90%, 90% to 10%		Test circuit and Waveforms		3.8 4.2		3.0 3.0	5.0 5.0	ns
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to Y_n	74F11244	Waveform 2	2.5 2.5	3.0 4.8	5.2 5.2	2.5 2.5	5.5 6.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.7 6.2	5.7 7.0	3.0 3.0	6.0 7.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 3 Waveform 4	2.0 2.0	3.5 3.4	6.0 6.0	2.0 2.5	5.5 5.0	ns
t_{TLH} t_{THL}	Transition time 10% to 90%, 90% to 10%		Test circuit and Wavforms		3.9 4.1		3.0 3.0	5.5 6.0	ns

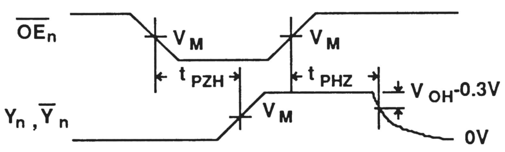
AC WAVEFORMS


I_{an}, I_{bn}
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Y}_n$
V_M
V_M

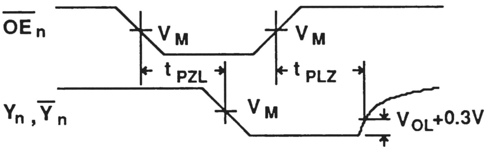
Waveform 1. For Inverting Outputs


I_{an}, I_{bn}
V_M
V_M
t_{PLH}
t_{PHL}
Y_n
V_M
V_M

Waveform 2. For Non-Inverting Outputs


$\overline{OE}_n$
V_M
V_M
t_{PZH}
t_{PHZ}
V_{OH}-0.3V
Y_n, $\overline{Y}_n$
V_M
0V

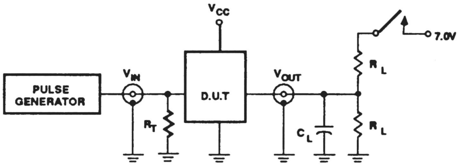
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level


$\overline{OE}_n$
V_M
V_M
t_{PZL}
t_{PLZ}
Y_n, $\overline{Y}_n$
V_M
V_{OL}+0.3V

Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
7.0V
PULSE GENERATOR
V_{IN}
D.U.T
V_{OUT}
R_L
R_T
C_L
R_L

Test Circuit For 3-State Outputs

SWITCH POSITION

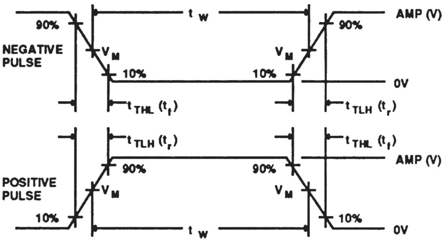
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


NEGATIVE PULSE
90%
V_M
10%
t_W
t_{THL} (t_f)
t_{TLH} (t_r)
AMP (V)
0V
POSITIVE PULSE
t_{TLH} (t_r)
t_{THL} (t_f)
90%
V_M
10%
t_W
AMP (V)
0V

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	**Rep. Rate**	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F11373, 74F11374

Latch/Flip-Flops

74F11373 Octal Transparent Latch (3-State)
74F11374 Octal D Flip-Flop (3-State)
Preliminary Specification

FEATURES

- Same function as 'F373 and 'F374 but with ACL compatible pinout
- 8-bit transparent latch-'F11373
- 8-Bit positive edge triggered register-'F11374
- Light loading input structure reduces bus loading (20µA in High and Low states)
- Multiple, centered V_{CC} and GND pins minimize package inductance and reduced ground bounce
- Controlled output ramp minimizes ground bounce
- High internal speed provides performance upgrade over 'F373 and 'F374 while consuming less power
- Flow through pinout structure simplifies PC board design
- 3-State Output buffers
- Common 3-state Output Enable
- Independent register and 3-state buffer operation

DESCRIPTION

The 74F11373 and 74F11374 are functionally equivalent to the 74F373 and 74F374. However, the pinout of the 74F11373 and 74F11374 differs from the 74F373 and 74F374 in that additional centered V_{CC} and GND pins have been

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F11373	6.0ns	40mA
74F11374	6.0ns	40mA

ORDERING INFORMATION

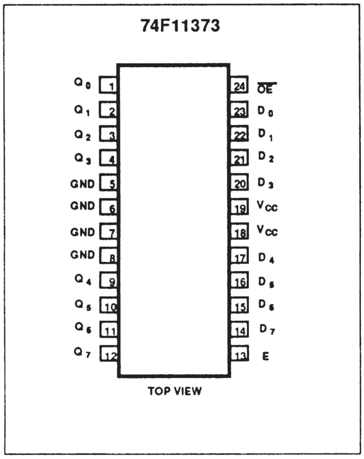
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic SLIM DIP (300 mil)	N74F11373N, N74F11374N
24-Pin Plastic SOL	N74F11373D, N74F11374D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

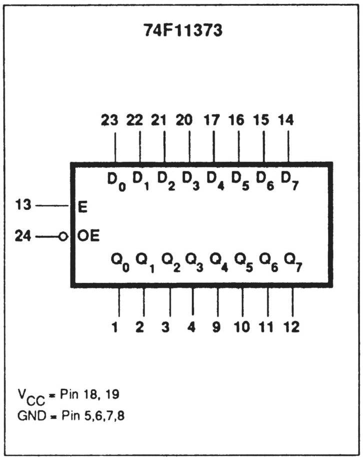
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/0.033	20µA/20µA
E ('F11373)	Latch enable input (active High)	1.0/0.033	20µA/20µA
$\overline{OE}$	Output enable input (active Low)	1.0/0.033	20µA/20µA
CP ('F11374)	Clock Pulse input (Active rising edge)	1.0/0.033	20µA/20µA
Q_0 - Q_7	3-State outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

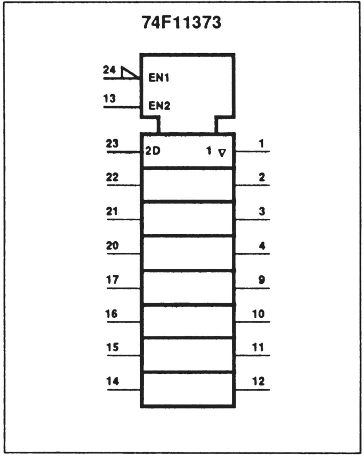

74F11373
Q0 1
Q1 2
Q2 3
Q3 4
GND 5
GND 6
GND 7
GND 8
Q4 9
Q5 10
Q6 11
Q7 12
24 OE
23 D0
22 D1
21 D2
20 D3
19 Vcc
18 Vcc
17 D4
16 D5
15 D6
14 D7
13 E
TOP VIEW

LOGIC SYMBOL

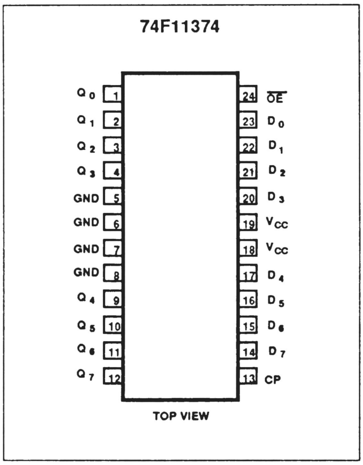

74F11373
23 22 21 20 17 16 15 14
D0 D1 D2 D3 D4 D5 D6 D7
13 E
24 OE
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
1 2 3 4 9 10 11 12

V_{CC} = Pin 18, 19
GND = Pin 5,6,7,8

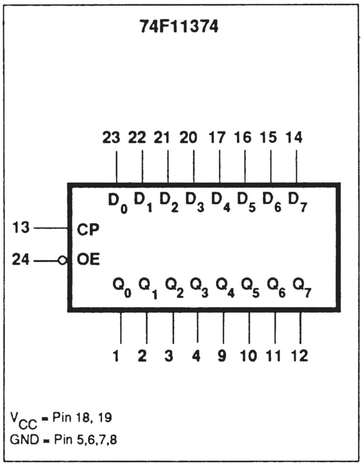
LOGIC SYMBOL(IEEE/IEC)


74F11373
24 EN1
13 EN2
23 2D 1▽ 1
22 2
21 3
20 4
17 9
16 10
15 11
14 12

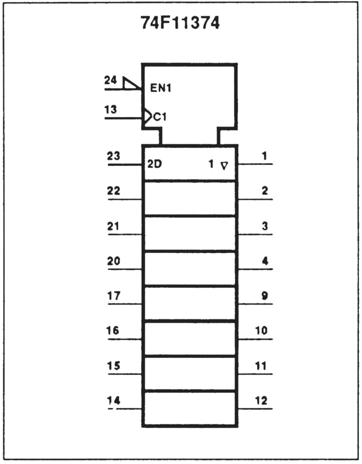
PIN CONFIGURATION


74F11374
Q0 1
Q1 2
Q2 3
Q3 4
GND 5
GND 6
GND 7
GND 8
Q4 9
Q5 10
Q6 11
Q7 12
24 OE
23 D0
22 D1
21 D2
20 D3
19 Vcc
18 Vcc
17 D4
16 D5
15 D6
14 D7
13 CP
TOP VIEW

LOGIC SYMBOL


74F11374
23 22 21 20 17 16 15 14
D0 D1 D2 D3 D4 D5 D6 D7
13 CP
24 OE
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
1 2 3 4 9 10 11 12
VCC = Pin 18, 19
GND = Pin 5,6,7,8

LOGIC SYMBOL(IEEE/IEC)


74F11374
24
EN1
13
C1
23
2D
1
22
2
21
3
20
4
17
9
16
10
15
11
14
12

added to minimize the effects of package inductance. These pinouts are compatible with the ACL standard pinouts.The 74F11373 and 74F11374 also feature a light loading input structure, a controlled output ramp to minimize bounce and high performance A/C characteristics which provide an upgrade to existing74F373 and 74F374.

The 74F11373 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High and stores the data that is present one set-up time before the High-to-Low enable transition.

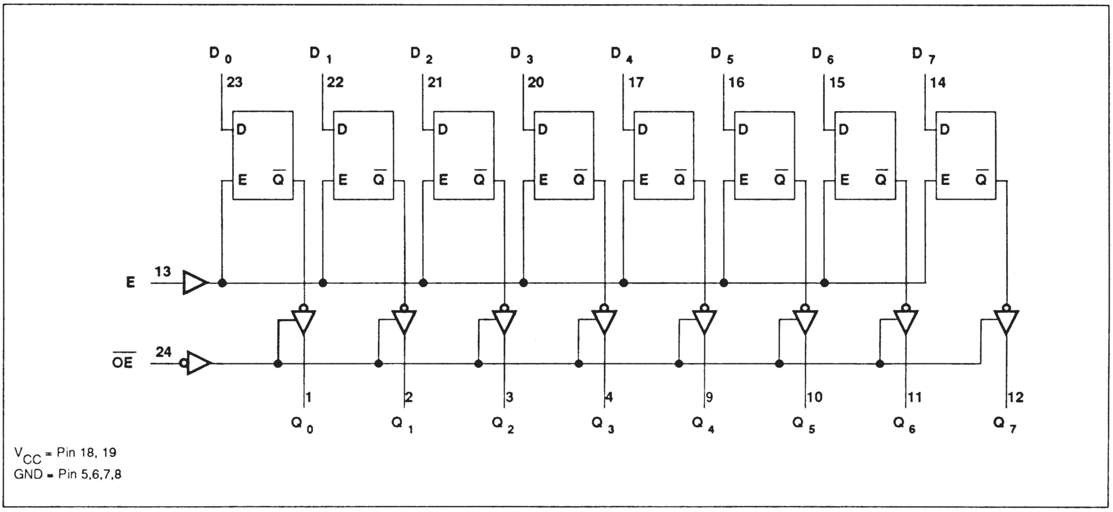
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74F11374 is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

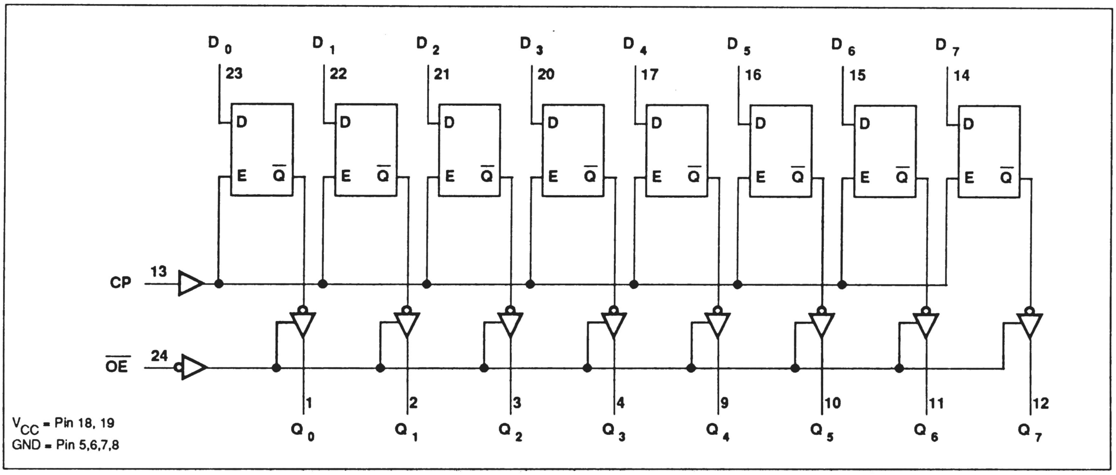
The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, 74F11373


D0 23
D1 22
D2 21
D3 20
D4 17
D5 16
D6 15
D7 14
D
E
Q
E 13
OE 24
1 Q0
2 Q1
3 Q2
4 Q3
9 Q4
10 Q5
11 Q6
12 Q7
VCC = Pin 18, 19
GND = Pin 5,6,7,8

LOGIC DIAGRAM, 74F11374



FUNCTION TABLE, 74F11373

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	D_n	REGISTER	Q_0 - Q_7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X D_n	NC D_n	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

FUNCTION TABLE, 74F11374

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	D_n	REGISTER	Q_0 - Q_7	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↑	X	NC	NC	Hold
H H	↑̸ ↑	X D_n	NC D_n	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↑̸ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
				V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
				V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				-20	μA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V				50	μA
I_{OZL}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 0.5V				-50	μA
I_{OS}	Short circuit output current[3]			V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	74F11373	V_{CC} = MAX			40	54	mA
		I_{CCL}					40	54	mA
		I_{CCZ}					40	54	mA
		I_{CCH}	74F11374	V_{CC} = MAX			40	54	mA
		I_{CCL}					40	54	mA
		I_{CCZ}					40	54	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

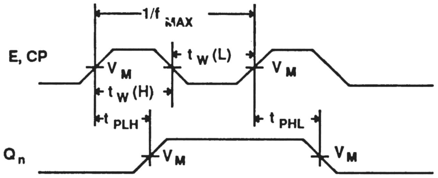
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F11373	Waveform 3	3.0 2.0	5.9 6.5	7.0 5.0	3.0 3.0	7.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n		Waveform 3	5.0 3.0	5.2 6.0	11.5 7.0	4.0 4.0	6.0 6.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	2.0 2.0	4.9 6.5	11.0 7.5	4.0 5.0	6.0 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	2.0 2.0	3.1 2.7	6.5 5.0	2.0 2.0	6.0 6.0	ns
t_{TLH} t_{THL}	Transition time 10% to 90%, 90% to 10%		Test Circuit and Waveforms		3.5 4.3		3.0 3.0	5.0 5.0	ns
f_{MAX}	Maximum Clock frequency	74F11374	Waveform 3	100			70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 3	4.0 4.0	5.1 5.9	8.5 8.5	4.0 4.0	6.0 6.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	2.0 2.0	4.9 6.5	11.5 7.5	4.0 4.0	6.0 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	2.0 2.0	3.1 2.7	7.0 5.5	2.0 2.0	5.0 5.0	ns
t_{TLH} t_{THL}	Transition time 10% to 90%, 90% to 10%		Test Circuit and Waveforms		3.5 4.3		3.0 3.0	5.0 6.0	ns

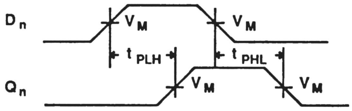
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time D_n to E	74F11373	Waveform 3	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to E		Waveform 3	0.0 0.0			0.0 0.0		ns
$t_w(H)$	E Pulse width, High		Waveform 1	6.0			6.0		ns
$t_s(H)$ $t_s(L)$	Set-up time D_n to CP	74F11374	Waveform 4	1.0 1.0			0.0 0.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP		Waveform 4	0.0 0.0			2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 1	7.0 6.0			7.0 6.0		ns

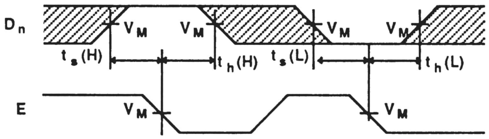
AC WAVEFORMS


E, CP
1/f MAX
V M
t W (L)
t W (H)
t PLH
t PHL
Q n
V M

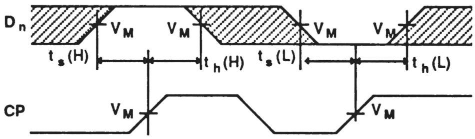
Waveform 1. Propagation Delay, Clock And Enable Inputs To Output, Enable, and Clock Pulse Widths, and Maximum Clock Frequency


D n
V M
t PLH
t PHL
Q n
V M

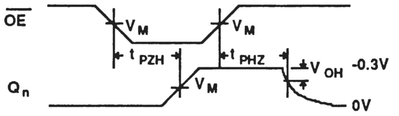
Waveform 2. Propagation Delay For Data To Outputs


D n
V M
t s (H)
t h (H)
t s (L)
t h (L)
E
V M

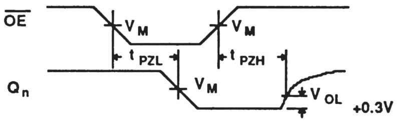
Waveform 3. Data Setup And Hold Times


D n
V M
t s (H)
t h (H)
t s (L)
t h (L)
CP
V M

Waveform 4. Data Setup And Hold Times


OE
V M
t PZH
t PHZ
V OH
-0.3V
Q n
0V

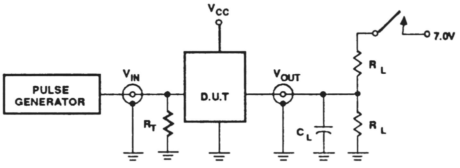
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level


OE
V M
t PZL
t PZH
Q n
V OL
+0.3V

Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V CC
7.0V
PULSE GENERATOR
V IN
R T
D.U.T
V OUT
C L
R L
R L

Test Circuit For 3-State Outputs

SWITCH POSITION

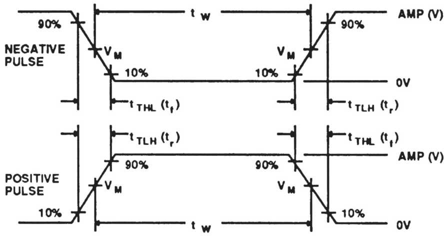
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


t w
AMP (V)
90%
NEGATIVE PULSE
V M
10%
0V
t THL (t f)
t TLH (t r)
POSITIVE PULSE
AMP (V)
90%
10%
0V

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F11543, 74F11544, Transceivers

74F11543 Octal Latched Transceiver, Non-Inverting (3-State)
74F11544 Octal Latched Transceiver, Inverting (3-State)
Preliminary Specification

FEATURES

- Same function as 'F543 and 'F544 but with ACL compatible pinout
- Combines 'F245 and 'F373 type functions in one chip
- 8-bit octal transceiver with D-type latch
- 'F11543 Non-inverting
  'F11544 Inverting
- 64mA current sinking capability (B port)
- Back-to-back latches for storage
- Separate controls for data flow in each direction
- Light loading input structure reduces bus loading (20µA in High and Low states)
- Multiple, centered V_{CC} and GND pins minimize package inductance and reduced ground bounce
- Controlled output ramp minimizes ground bounce
- High internal speed provides performance upgrade over 'F543 and 'F544 while consuming less power
- Flow through pinout structure simplifies PC board design
- 3-State Output buffers
- Common 3-state Output Enable
- Independent latch and 3-state buffer operation

DESCRIPTION

The 74F11543 and 74F11544 are func-

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F11543	6.0ns	80mA
74F11544	6.0ns	80mA

ORDERING INFORMATION

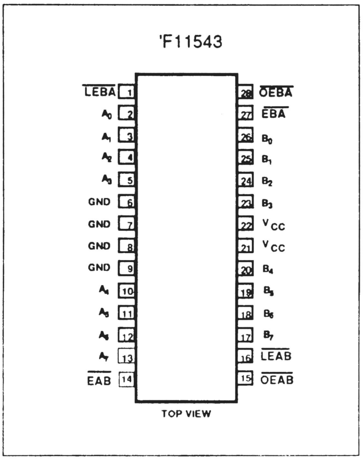
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic SLIM DIP (300 mil)	N74F11543N, N74F11544N
28-Pin Plastic SOL	N74F11543D, N74F11544D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

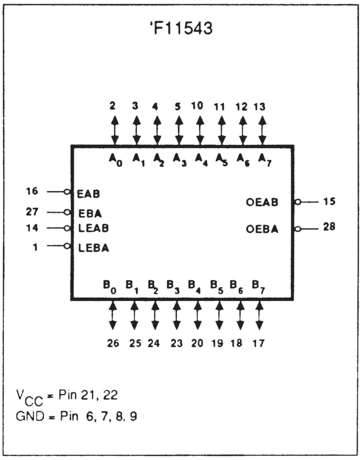
PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F11543	A_0 - A_7	Port A, 3-state inputs	3.5/0.116	70µA/70µA
	B_0 - B_7	Port B, 3-state inputs	3.5/0.116	70µA/70µA
'F11544	A_0 - A_7	Port $\overline{A}$, 3-state inputs	3.5/0.116	70µA/70µA
	B_0 - B_7	Port $\overline{B}$, 3-state inputs	3.5/0.116	70µA/70µA
'F11543 'F11544	$\overline{OEAB}$	A-to-B Output Enable input (Active Low)	1.0/0.033	20µA/20µA
	$\overline{OEBA}$	A-to-B Output Enable input (Active Low)	1.0/0.033	20µA/20µA
	$\overline{EBA}$	A-to-B Enable input (Active Low)	1.0/0.033	20µA/40µA
	$\overline{EBA}$	B-to-A Enable input (Active Low)	1.0/0.033	20µA/40µA
	$\overline{LEAB}$	A-to-B Latch Enable input (Active Low)	1.0/0.033	20µA/20µA
	$\overline{LEBA}$	B-to-A Latch Enable input (Active Low)	1.0/0.033	20µA/20µA
'F11544	A_0 - A_7	Port A, 3-state outputs	150/40	3.0mA/24mA
	B_0 - B_7	Port B, 3-state outputs	750/106.7	15mA/64mA
'F11543	A_0 - A_7	Port $\overline{A}$, 3-state outputs	150/40	3.0mA/24mA
	B_0 - B_7	Port $\overline{B}$, 3-state outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

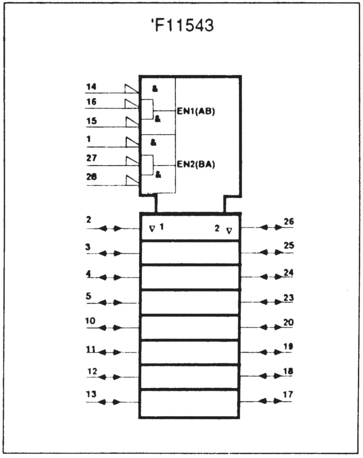
PIN CONFIGURATION


'F11543
LEBA 1
A0 2
A1 3
A2 4
A3 5
GND 6
GND 7
GND 8
GND 9
A4 10
A5 11
A6 12
A7 13
EAB 14
28 OEBA
27 EBA
26 B0
25 B1
24 B2
23 B3
22 VCC
21 VCC
20 B4
19 B5
18 B6
17 B7
16 LEAB
15 OEAB
TOP VIEW

LOGIC SYMBOL

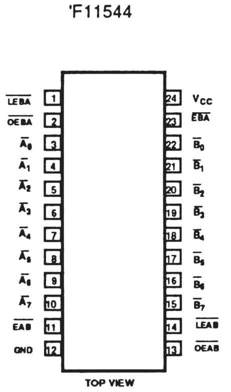

'F11543
2 3 4 5 10 11 12 13
A0 A1 A2 A3 A4 A5 A6 A7
16 EAB
27 EBA
14 LEAB
1 LEBA
OEAB 15
OEBA 28
B0 B1 B2 B3 B4 B5 B6 B7
26 25 24 23 20 19 18 17
VCC = Pin 21, 22
GND = Pin 6, 7, 8, 9

LOGIC SYMBOL(IEEE/IEC)

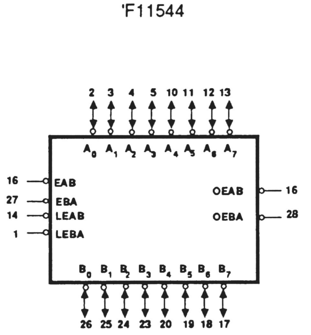

'F11543
14
16
15
1
27
28
&
EN1(AB)
EN2(BA)
▽1
2▽
2 3 4 5 10 11 12 13
26 25 24 23 20 19 18 17

tionally equivalent to the 74F543 and 74F544. However, the pinout of the 'F11543 and 'F11544 differs from the 'F543 and 'F544 in that additional centered V_{CC} and GND pins have been added to minimize the effects of package inductance. These pinouts are compatible with the ACL standard pinouts.The 'F11543 and 'F11544 also feature a light loading input structure, a controlled output ramp to minimize ground bounce and high performance A/C characteristics which provide an upgrade to existing 'F543 and 'F544. The 'F11543 and 'F11544 Octal Latched Transceivers contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{\mathrm{LEAB}}$, $\overline{\mathrm{LEBA}}$) and Output Enable ($\overline{\mathrm{OEAB}}$, $\overline{\mathrm{OEBA}}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.While the 'F11543 has non-inverting data path, the 'F11544 inverts data in both directions. The A outputs are guaranteed to sink 24mA while the B outputs are rated for 64mA.

PIN CONFIGURATION

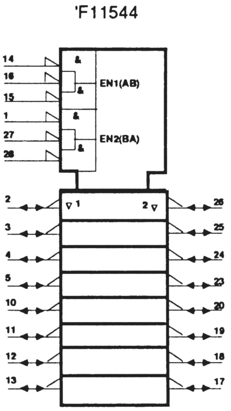

'F11544
$\overline{\mathrm{LEBA}}$ 1
$\overline{\mathrm{OEBA}}$ 2
$\overline{A}_0$ 3
$\overline{A}_1$ 4
$\overline{A}_2$ 5
$\overline{A}_3$ 6
$\overline{A}_4$ 7
$\overline{A}_5$ 8
$\overline{A}_6$ 9
$\overline{A}_7$ 10
$\overline{\mathrm{EAB}}$ 11
GND 12
24 V_{CC}
23 $\overline{\mathrm{EBA}}$
22 $\overline{B}_0$
21 $\overline{B}_1$
20 $\overline{B}_2$
19 $\overline{B}_3$
18 $\overline{B}_4$
17 $\overline{B}_5$
16 $\overline{B}_6$
15 $\overline{B}_7$
14 $\overline{\mathrm{LEAB}}$
13 $\overline{\mathrm{OEAB}}$
TOP VIEW

LOGIC SYMBOL


'F11544
2 3 4 5 10 11 12 13
A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7
16 EAB
27 EBA
14 LEAB
1 LEBA
OEAB 16
OEBA 28
B_0 B_1 B_2 B_3 B_4 B_5 B_6 B_7
26 25 24 23 20 19 18 17

V_{CC} = Pin 21, 22
GND = Pin 6, 7, 8, 9

LOGIC SYMBOL(IEEE/IEC)


'F11544
14
16
15
1
27
28
&
&
EN1(AB)
&
&
EN2(BA)
2
3
4
5
10
11
12
13
▽1
2▽
26
25
24
23
20
19
18
17

FUNCTIONAL DESCRIPTION

The 'F11543 and 'F11544 contain two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{\mathrm{EAB}}$) input must be Low in order to enter data from A_0-A_7 or take data from B_0-B_7, as indicated in the Function Table. With $\overline{\mathrm{EAB}}$ Low, a Low signal on the A-to-B Latch Enable ($\overline{\mathrm{LEAB}}$) input makes the A-to-B latches transparent; a subsequent Low-to High transition of the $\overline{\mathrm{LEAB}}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{\mathrm{EAB}}$ and $\overline{\mathrm{OEAB}}$ both Low, the 3-state B output buffers are active and display the data present at the outputs of the A latches.

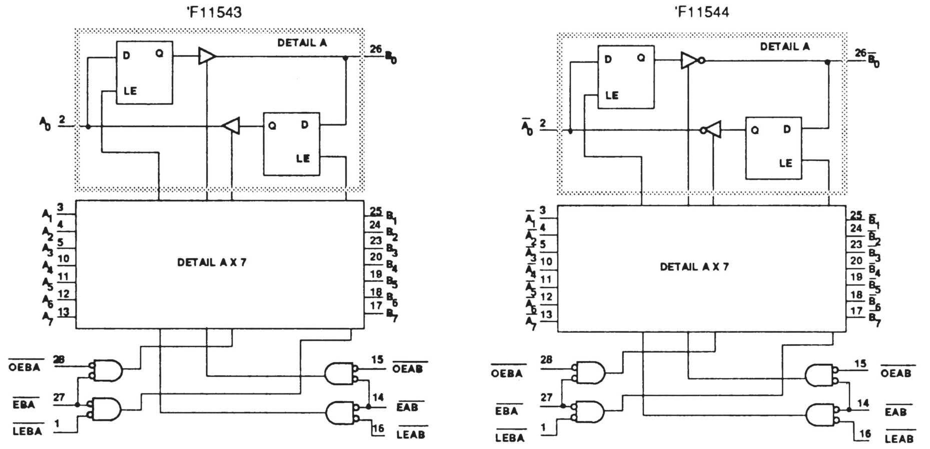
Control of data flow from B to A is similar, but using the $\overline{\mathrm{EBA}}$, $\overline{\mathrm{LEBA}}$, and $\overline{\mathrm{OEBA}}$ inputs.

FUNCTION TABLE for 'F11543 and 'F11544

INPUTS				OUTPUTS		STATUS
$\overline{\mathrm{OEXX}}$	$\overline{\mathrm{EXX}}$	$\overline{\mathrm{LEXX}}$	DATA	'F11543	'F11544	
H	X	X	X	Z	Z	Disabled
X	H	X	X	Z	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	L H	Latch + Display
L L	L L	L L	H L	H L	L H	Transparent
L	L	H	X	NC	NC	Hold

H= High voltage level
L= Low voltage level
h= High state must be present one setup time before the Low-to-High transition of $\overline{\mathrm{LEXX}}$ or $\overline{\mathrm{EXX}}$ (XX=AB or BA)
l = Low state must be present one setup time before the Low-to -High transition of $\overline{\mathrm{LEXX}}$ or $\overline{\mathrm{EXX}}$ (XX=AB or BA)
↑ =Low-to-High transition of $\overline{\mathrm{LEXX}}$ or $\overline{\mathrm{EXX}}$ (XX=AB or BA)
X=Don't care
NC=No change
Z =High impedance "off" state

LOGIC DIAGRAM


'F11543
'F11544
DETAIL A
D
Q
LE
DETAIL A X 7
A_0 2
26 B_0
A_1–A_7 3, 4, 5, 10, 11, 12, 13
B_1–B_7 25, 24, 23, 20, 19, 18, 17
$\overline{OEBA}$ 28
$\overline{EBA}$ 27
$\overline{LEBA}$ 1
$\overline{OEAB}$ 15
$\overline{EAB}$ 14
$\overline{LEAB}$ 16

V_{CC}=Pin 21, 22
GND=Pin 6, 7, 8, 9

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7, $\overline{A}_0$-$\overline{A}_7$	48	mA
		B_0-B_7, $\overline{B}_0$-$\overline{B}_7$	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7, $\overline{A}_0$-$\overline{A}_7$			-3	mA
		B_0-B_7, $\overline{B}_0$-$\overline{B}_7$			-15	mA
I_{OL}	Low-level output current	A_0-A_7, $\overline{A}_0$-$\overline{A}_7$			24	mA
		B_0-B_7, $\overline{B}_0$-$\overline{B}_7$			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage	A_0-A $\overline{A}_0$-$\overline{A}_7$		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
		B_0-B_7 $\overline{B}_0$-$\overline{B}_7$			I_{OH}=-15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A $\overline{A}_0$-$\overline{A}_7$		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
						±5%V_{CC}		0.35	0.50	V
		B_0-B_7 $\overline{B}_0$-$\overline{B}_7$			I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
					I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEAB}$, $\overline{OEBA}$, $\overline{EAB}$ $\overline{EBA}$,$\overline{LEAB}$, $\overline{LEBA}$		V_{CC} = MAX, V_I = 7.0V					100	μA
		Others		V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	Others		V_{CC} = MAX, V_I = 0.5V					-20	μA
		$\overline{EAB}$, $\overline{EBA}$							-40	μA
$I_{IH}+I_{OZH}$	Off-state current High level voltage applied			V_{CC} = MAX, V_O= 2.7V					70	μA
$I_{IL}+I_{OZL}$	Off-state current Low-level voltage applied			V_{CC} = MAX, V_O= 0.5V					-600	μA
I_{OS}	Short-circuit output current[3]	A_0-A_7, $\overline{A}_0$-$\overline{A}_7$		V_{CC} = MAX			-60		-150	mA
		B_0-B_7, $\overline{B}_0$-$\overline{B}_7$					-100		-225	mA
I_{CC}	Supply current (total)	'F11543	I_{CCH}	V_{CC} = MAX				70	105	mA
			I_{CCL}					95	135	mA
			I_{CCZ}					95	135	mA
		'F11544	I_{CCH}	V_{CC} = MAX				80	110	mA
			I_{CCL}					105	140	mA
			I_{CCZ}					100	135	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F11543					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	3.5 3.0	5.5 5.0	7.5 7.0	3.0 2.5	8.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	2.0 2.5	4.0 4.5	6.0 6.5	1.5 2.5	6.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to A_n	Waveform 1, 2	5.0 4.0	7.0 6.0	9.0 8.0	4.5 4.0	10.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEAB}$ to B_n	Waveform 1, 2	6.0 4.5	8.5 6.5	10.5 8.5	5.5 4.0	11.5 9.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	Waveform 4 Waveform 5	2.0 3.5	4.0 5.0	6.5 8.5	1.5 3.0	7.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	Waveform 4 Waveform 5	1.0 1.5	3.0 4.0	6.5 7.5	1.0 1.0	6.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{EBA}$ or $\overline{EAB}$ to A_n or B_n	Waveform 4 Waveform 5	4.5 5.5	7.0 7.5	9.5 10.0	4.0 5.0	11.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{EBA}$ or $\overline{EAB}$ to A_n or B_n	Waveform 4 Waveform 5	2.5 4.5	5.0 7.0	7.5 10.0	2.0 3.0	8.5 11.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	74F11543					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to $\overline{LEAB}$, $\overline{LEBA}$, $\overline{EAB}$, or $\overline{EBA}$	Waveform 3	2.0 3.5			2.0 3.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to $\overline{LEAB}$, $\overline{LEBA}$, $\overline{EAB}$, or $\overline{EBA}$	Waveform 3	1.0 2.0			1.0 2.0		ns
$t_w(L)$	Latch enable Pulse width, Low	Waveform 3	4.0			4.5		ns

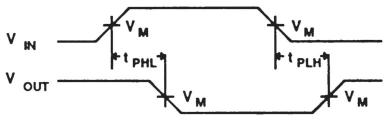
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F11544					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{B}_n$ or $\overline{B}_n$ to $\overline{A}_n$	Waveform 1	3.0 3.0	6.5 5.0	8.5 7.0	3.0 3.0	9.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to $\overline{A}_n$	Waveform 1, 2	4.0 4.0	7.0 7.0	8.5 8.5	4.0 4.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEAB}$ to $\overline{B}_n$	Waveform 1, 2	5.0 4.0	8.0 7.5	10.5 8.5	4.0 4.0	11.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ to $\overline{A}_n$ or $\overline{OEAB}$ to $\overline{B}_n$	Waveform 4 Waveform 5	3.0 4.0	5.0 7.0	7.0 9.0	2.5 4.0	7.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ to $\overline{A}_n$ or $\overline{OEAB}$ to $\overline{B}_n$	Waveform 4 Waveform 5	1.0 2.5	4.0 5.5	5.5 7.5	1.0 2.5	6.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{EBA}$ to $\overline{A}_n$ or $\overline{EAB}$ to $\overline{B}_n$	Waveform 4 Waveform 5	4.0 4.5	7.0 8.0	8.5 10.0	4.0 4.5	9.5 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{EBA}$ to $\overline{A}_n$ or $\overline{EAB}$ to $\overline{B}_n$	Waveform 4 Waveform 5	2.5 4.5	5.0 8.5	7.0 10.5	2.5 4.5	8.0 11.5	ns

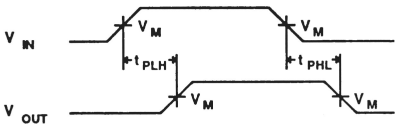
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	74F11544					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to $\overline{LEAB}$ or $\overline{LEBA}$	Waveform 3	2.5 2.5			2.5 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to $\overline{LEAB}$ or $\overline{LEBA}$	Waveform 3	2.5 2.5			3.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to $\overline{EAB}$ or $\overline{EBA}$	Waveform 3	2.5 2.5			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to $\overline{EAB}$ or $\overline{EBA}$	Waveform 3	2.5 2.5			3.0 3.0		ns
$t_w(L)$	Latch enable Pulse width, Low	Waveform 3	4.0			4.5		ns

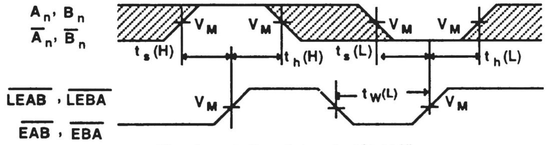
AC WAVEFORMS


V IN
V OUT
V M
t PHL
t PLH

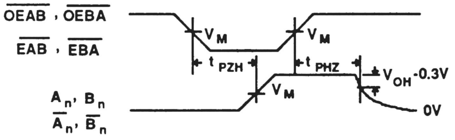
Waveform 1. Propagation Delay For Inverting Output


V IN
V OUT
V M
t PLH
t PHL

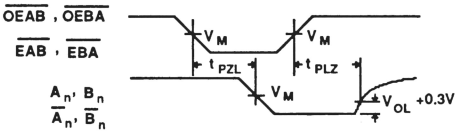
Waveform 2. Propagation Delay For Non-Inverting Output


A_n, B_n
$\overline{A}_n$, $\overline{B}_n$
$\overline{LEAB}$, $\overline{LEBA}$
$\overline{EAB}$, $\overline{EBA}$
V M
t s (H)
t h (H)
t s (L)
t h (L)
t W(L)

Waveform 3. Data Setup And Hold Times And Latch Enable pulse width


$\overline{OEAB}$, $\overline{OEBA}$
EAB, EBA
A_n, B_n
$\overline{A}_n$, $\overline{B}_n$
V M
t PZH
t PHZ
V OH -0.3V
0V

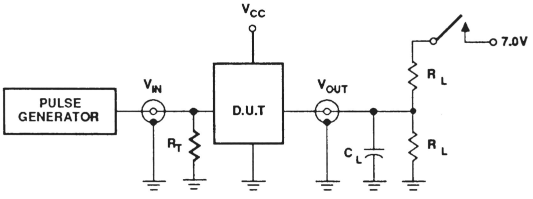
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level


$\overline{OEAB}$, $\overline{OEBA}$
EAB, EBA
A_n, B_n
$\overline{A}_n$, $\overline{B}_n$
V M
t PZL
t PLZ
V OL +0.3V

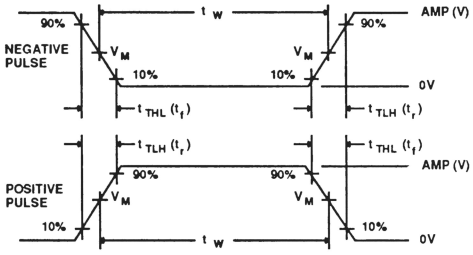
Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded area indicate when the input is permitted to change for predictable output

TEST CIRCUIT AND WAVEFORMS


V_{CC}
7.0V
PULSE GENERATOR
V_{IN}
R_T
D.U.T
V_{OUT}
C_L
R L
R L

Test Circuit For 3-State Outputs


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
V M
t w
AMP (V)
0V
t THL (t f)
t TLH (t r)

V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F11646, 74F11648 Transceivers/Registers

74F11646 Octal Transceiver/Register, Non-Inverting (3-State)
74F11648 Octal Transceivers/Register, Inverting (3-State)
Preliminary Specification

FEATURES

- **Same function as 74F646 and 74F648 but with ACL compatible pinout**
- **Combines 74F245 and 74F374 type functions in one chip**
- **Light loading input structure reduces bus loading (70µA in High and Low states)**
- **Multiple, centered V_{CC} and GND pins minimize package inductance and reduced ground bounce**
- **Controlled output ramp minimizes ground bounce**
- **High internal speed provides performance upgrade over 74F646 and 74F648 while consuming less power**
- **Flow through pinout structure simplifies PC board design**

DESCRIPTION

The 74F11646 and 74F11648 are functionally equivalent to the 74F646 and 74F648. However, the pinout of the 74F11646 and 74F11648 differs from the 74F646 and 74F648 in that additional-centered V_{CC} and GND pins have been added to minimize the effects of package inductance. These pinouts are compatible with the ACL standard pinouts.The 74F11646 and 74F11648 also feature a light loading input structure, a controlled output ramp to minimize ground bounce and high performance AC characteristics which provide an upgrade to the existing 74F646 and 74F648.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F11646	115MHz	120mA
74F11648	115MHz	120mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic SLIM DIP (300 mil)	N74F11646N, N7411F648N
28-Pin Plastic SOL[1]	N74F11646D, N7411F648D

NOTE 1: Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

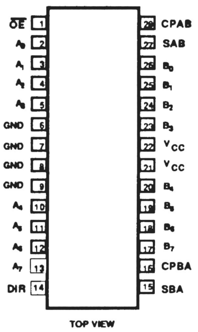
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A inputs	3.5/0.116	70µA/70µA
B_0 - B_7	B inputs	3.5/0.116	70µA/70µA
CPAB	A-to-B clock input	1.0/0.033	20µA/20µA
CPBA	B-to-A clock input	1.0/0.033	20µA/20µA
SAB	A-to-B select input	1.0/0.033	20µA/20µA
SBA	B-to-A select input	1.0/0.033	20µA/20µA
DIR	Data flow Directional control Enable input	1.0/0.033	20µA/20µA
$\overline{OE}$	Output enable input	1.0/0.033	20µA/20µA
A_0 - A_7	A outputs	750/106.7	15mA/64mA
B_0 - B_7	B outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

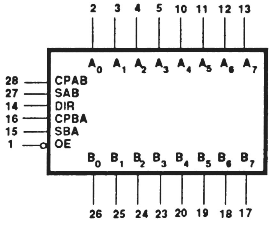
'F11646



$\overline{OE}$ 1
A_0 2
A_1 3
A_2 4
A_3 5
GND 6
GND 7
GND 8
GND 9
A_4 10
A_5 11
A_6 12
A_7 13
DIR 14
28 CPAB
27 SAB
26 B_0
25 B_1
24 B_2
23 B_3
22 V_{CC}
21 V_{CC}
20 B_4
19 B_5
18 B_6
17 B_7
16 CPBA
15 SBA
TOP VIEW

LOGIC SYMBOL

'F11646

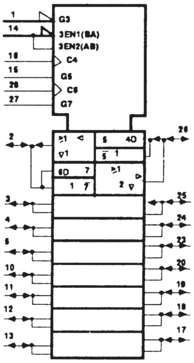


2 3 4 5 10 11 12 13
A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7
28 CPAB
27 SAB
14 DIR
16 CPBA
15 SBA
1 OE
B_0 B_1 B_2 B_3 B_4 B_5 B_6 B_7
26 25 24 23 20 19 18 17

V_{CC} = Pin 21, 22
GND = Pin 6,7,8, 9

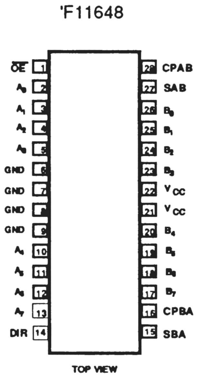
LOGIC SYMBOL(IEEE/IEC)

'F11646

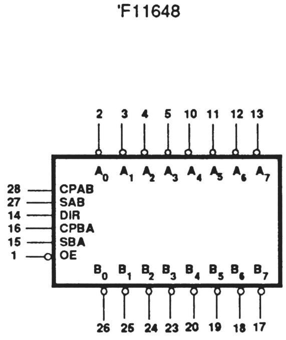


1
14
16
15
28
27
G3
3EN1(BA)
3EN2(AB)
C4
G5
C6
G7
≥1
▽1
5
4D
$\overline{5}$ 1
6D 7
1 $\overline{7}$
≥1
2 ▽
2
3
4
5
10
11
12
13
26
25
24
23
20
19
18
17

PIN CONFIGURATION

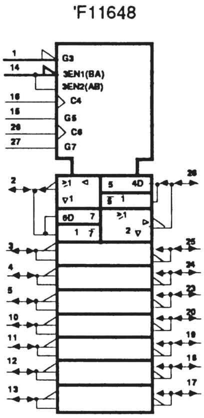

'F11648
OE 1
A0 2
A1 3
A2 4
A3 5
GND 6
GND 7
GND 8
GND 9
A4 10
A5 11
A6 12
A7 13
DIR 14
28 CPAB
27 SAB
26 B0
25 B1
24 B2
23 B3
22 VCC
21 VCC
20 B4
19 B5
18 B6
17 B7
16 CPBA
15 SBA
TOP VIEW

LOGIC SYMBOL


'F11648
2 3 4 5 10 11 12 13
A0 A1 A2 A3 A4 A5 A6 A7
28 CPAB
27 SAB
14 DIR
16 CPBA
15 SBA
1 OE
B0 B1 B2 B3 B4 B5 B6 B7
26 25 24 23 20 19 18 17

V_{CC} = Pin 21, 22
GND = Pin 6, 7, 8, 9

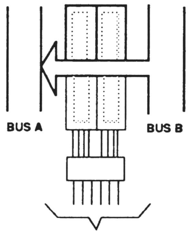
LOGIC SYMBOL(IEEE/IEC)


'F11648
1
14
G3
3EN1(BA)
3EN2(AB)
16
C4
15
G5
28
C6
27
G7
2
≥1
▽1
6D
7
1
5
4D
1
≥1
2▽
26
3 4 5 10 11 12 13
25 24 23 20 19 18 17

The 74F11646 and 74F11648 Transceivers/ Registers consist of bus transceiver circuits with 3-state outputs, D-type flipflops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the from internal registers. Data on the A or B bus will clocked into the registers as the appropriate clock pin goes High. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both. The select(SAB, SBA) pins determine whether data is stored or transfered through the device in real-time.The DIR determines which bus will receive data when the $\overline{OE}$ is active Low. In the isolation mode($\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register.

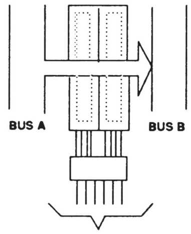
When an output function is disabled,the input function is still enabled and may be used to store and transmit data. Only one of the two busses , A or B may be driven at a time. The following examples demonstrates the four fundamental bus-management functions that can be performed with the 74F11646 and 74F11648.

REAL TIME BUS TRANSFER BUS B TO BUS A



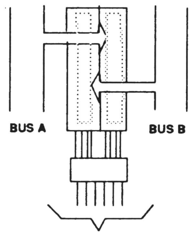
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER BUS A TO BUS B



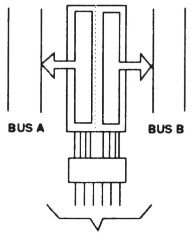
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
X	H	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

TRANSFER STORED DATA TO A OR B



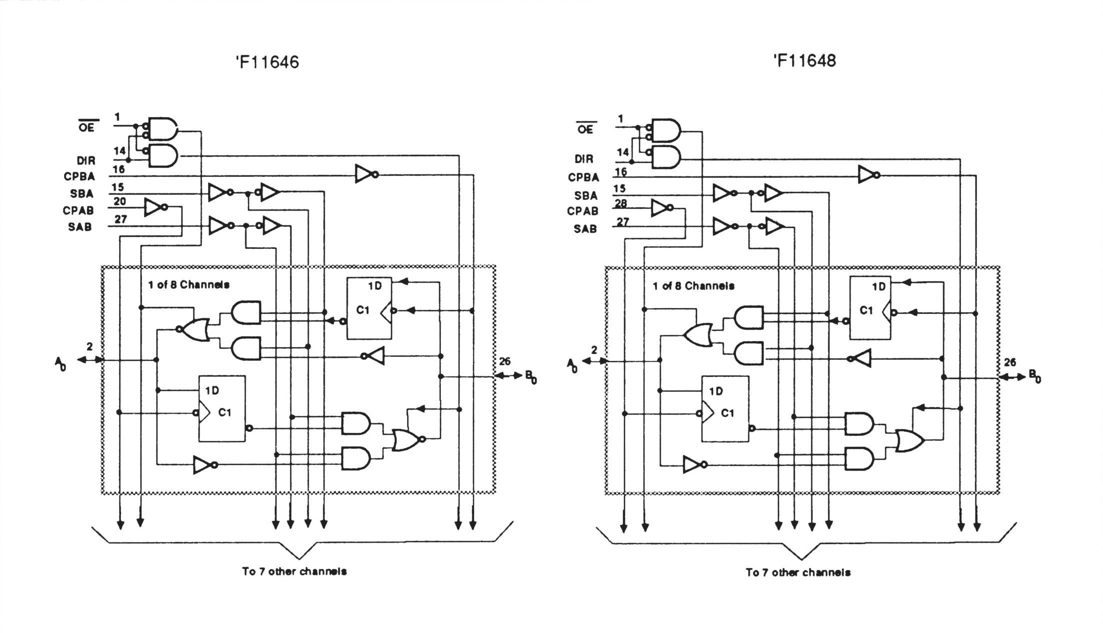
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	A_0-A_7	B_0-B_7	'F11646	'F11648
X	X	↑	X	X	X	input *Unspecified	Unspecified input *	Store A, B unspecified*	Store A, B unspecified*
X	X	X	↑	X	X			Store B, A unspecified*	Store B, A unspecified*
H	X	↑	↑	X	X	Input	Input	Store A and B data	Store A and B data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real time B data to A bus	Real time $\overline{B}$ data to A bus
L	L	X	H or L	X	H			Stored B data to A bus	Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real time A data to B bus	Real time $\overline{A}$ data to B bus
L	H	H or L	X	H	X			Stored A data to B bus	Stored $\overline{A}$ data to B bus

H= High voltage level
L= Low voltage level
X=Don't care
↑ =Low-to-High clock transition
*= The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enable, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

LOGIC DIAGRAM


'F11646
$\overline{OE}$
1
DIR
14
CPBA
16
SBA
15
CPAB
20
SAB
27
1 of 8 Channels
1D
C1
1D
C1
A_0
2
26
B_0
To 7 other channels
'F11648
$\overline{OE}$
1
DIR
14
CPBA
16
SBA
15
CPAB
28
SAB
27
1 of 8 Channels
1D
C1
1D
C1
A_0
2
26
B_0
To 7 other channels

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH}=-15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	$\overline{OE}$,DIR, CPAB, CPBA SAB, SBA	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{IH}+I_{OZH}	Off-state output current High level voltage applied	A_0-A_7, B_0-B_7	V_{CC} = MAX, V_O= 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low level voltage applied		V_{CC} = MAX, V_O = 0.5V					-70	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				110	145	mA
		I_{CCL}					120	155	mA
		I_{CCZ}					130	170	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F11646					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.0 4.5	7.0 6.5	8.5 7.5	4.5 4.0	9.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 2,3	3.0 2.0	5.0 4.5	7.0 5.0	2.5 2.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2,3	5.0 5.0	7.0 6.5	7.5 7.5	4.5 4.5	9.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	5.0 5.0	7.0 7.0	9.0 9.0	4.5 4.5	10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable time DIR to A_n or B_n	Waveform 5 Waveform 6	4.5 4.5	6.5 6.5	8.0 8.0	4.0 4.0	9.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	5.5 5.5	8.0 8.0	9.5 9.5	5.0 5.0	10.5 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to A_n or B_n	Waveform 5 Waveform 6	4.5 4.5	7.5 7.5	9.0 9.0	4.0 4.0	10.0 10.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	74F11646					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.0 6.0			4.0 6.0		ns

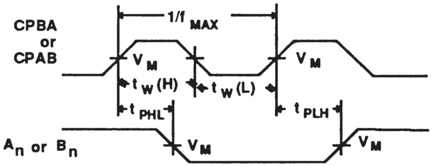
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F11648					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.0 4.0	7.0 6.5	8.5 7.5	4.5 3.5	10.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 2,3	2.0 2.5	5.0 4.5	6.5 6.5	2.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2,3	4.5 4.5	7.0 6.5	7.5 7.5	4.5 4.5	9.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	4.5 4.5	7.0 7.0	9.0 9.0	4.0 4.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable time DIR to A_n or B_n	Waveform 5 Waveform 6	4.0 4.0	6.5 6.5	8.5 8.5	3.5 3.5	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	5.0 5.0	8.0 8.0	9.5 9.5	4.5 4.5	10.5 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to A_n or B_n	Waveform 5 Waveform 6	5.0 5.0	7.5 7.5	9.5 9.5	4.5 4.5	10.5 10.5	ns

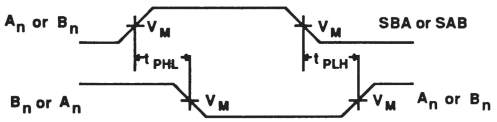
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	74F11648					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.0 4.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	3.5 6.5			4.0 7.0		ns

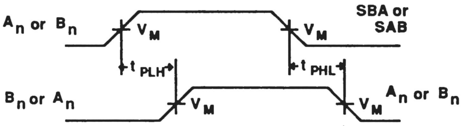
AC WAVEFORMS


CPBA or CPAB
1/f MAX
V M
t W (H)
t W (L)
t PHL
t PLH
A n or B n
V M

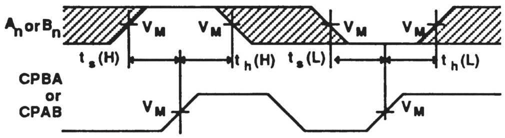
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency


A n or B n
V M
SBA or SAB
t PHL
t PLH
B n or A n
V M
A n or B n

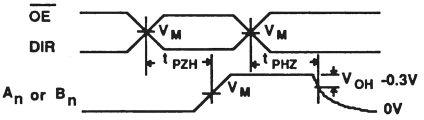
Waveform 2. Propagation Delay, An or Bn to Bn or An and SBA or SAB to An or Bn


A n or B n
V M
SBA or SAB
t PLH
t PHL
B n or A n
V M
A n or B n

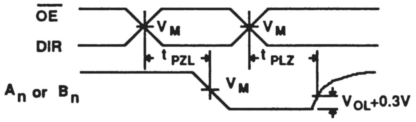
Waveform 3. Propagation Delay, An or Bn to Bn or An and SBA or SAB to An or Bn


A n or B n
V M
t s (H)
t h (H)
t s (L)
t h (L)
CPBA or CPAB
V M

Waveform 4. Data Setup And Hold Times


OE
DIR
V M
t PZH
t PHZ
V OH -0.3V
A n or B n
0V

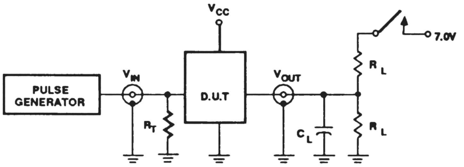
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level


OE
DIR
V M
t PZL
t PLZ
A n or B n
V OL+0.3V

Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V CC
7.0V
R L
PULSE GENERATOR
V IN
D.U.T
V OUT
R T
C L
R L

Test Circuit For 3-State Outputs

SWITCH POSITION

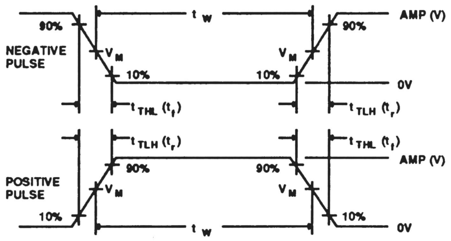
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


t w
AMP (V)
90%
NEGATIVE PULSE
V M
10%
0V
t THL (t f)
t TLH (t r)
POSITIVE PULSE

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F11651, 74F11652 Transceivers/Registers

74F11651 Octal Transceiver/Register, Inverting (3-State)
74F11652 Octal Transceiver/Register, Non-Inverting (3-State)
Preliminary Specification

FEATURES

- Same function as 'F651 and 'F652 but with ACL compatible pinout
- Independent register and 3-state buffer operation
- Multiplexed real-time and stored data
- Choice of non-inverting and inverting data paths
- Light loading input structure reduces bus loading (70µA in High and Low states)
- Multiple, centered V_{CC} and GND pins minimize package inductance and reduced ground bounce
- Controlled output ramp minimizes ground bounce
- High internal speed provides performance upgrade over 'F651 and 'F652 while consuming less power
- Flow through pinout structure simplifies PC board design
- 3-State Output buffers
- Common 3-state Output Enable

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F11651	110MHz	120mA
74F11652	110MHz	120mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Cerdip (300mil)	N74F11651F, N7411F652F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

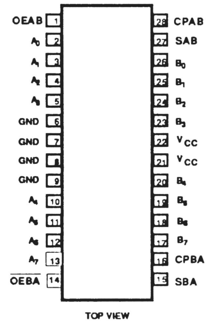
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A inputs	3.5/0.116	70µA/70µA
B_0 - B_7	B inputs	3.5/0.116	70µA/70 A
CPAB	A-to-B clock inputs	1.0/0.033	20µA/20µA
CPBA	B-to-A clock inputs	1.0/0.033	20µA/20µA
SAB	A-to-B select input	1.0/0.033	20µA/20µA
SBA	B-to-A select input	1.0/0.033	20µA/20µA
OEAB	A-to-B output enable input	1.0/0.033	20µA/20µA
$\overline{OEBA}$	B-to-A output enable input	1.0/0.033	20µA/20µA
A_0 - A_7	A outputs	750/106.7	15mA/64mA
B_0 - B_7	B outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

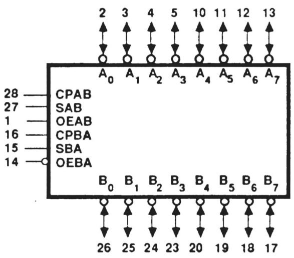
The 74F11651 and 74F11652 are functionally equivalent to the 74F651 and 74F652. However, the pinout of the 74F11651 and 74F11652 differs from the 74F651 and 74F652 in that additional centered V_{CC} and GND pins have been added to minimize the effects of package inductance. These pinouts are compatible with the ACL standard pinouts.The 74F11651 and 74F11652 also feature a light loading input structure, a controlled output ramp to minimize ground bounce, and high performance AC characteristics which provide an upgrade to the existing 74F651 and 74F652.

PIN CONFIGURATION


OEAB 1
A0 2
A1 3
A2 4
A3 5
GND 6
GND 7
GND 8
GND 9
A4 10
A5 11
A6 12
A7 13
OEBA 14
28 CPAB
27 SAB
26 B0
25 B1
24 B2
23 B3
22 VCC
21 VCC
20 B4
19 B5
18 B6
17 B7
16 CPBA
15 SBA
TOP VIEW

LOGIC SYMBOL

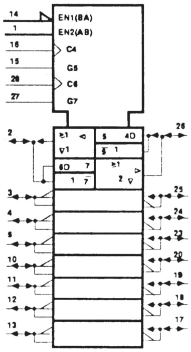
'F11651


2 3 4 5 10 11 12 13
A0 A1 A2 A3 A4 A5 A6 A7
28 CPAB
27 SAB
1 OEAB
16 CPBA
15 SBA
14 OEBA
B0 B1 B2 B3 B4 B5 B6 B7
26 25 24 23 20 19 18 17

V_{CC} = Pin 21, 22
GND = Pin 6, 7, 8, 9

LOGIC SYMBOL(IEEE/IEC)

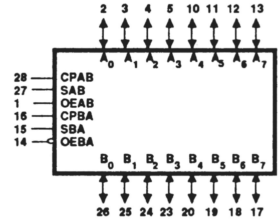
'F11651


14
1
16
15
28
27
EN1(BA)
EN2(AB)
C4
G5
C6
G7
2
≥1
∇1
5
4D
1
6D
7
1
7
≥1
2
26
3
4
5
10
11
12
13
25
24
23
20
19
18
17

The 74F11651 and 74F11652 Transceivers/ Registers consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{\text{OEBA}}$) and Select (SAB, SBA) pins are provided for bus management. The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'F11651 and 'F11652. The select pins determine whether data is stored or transferred through the device in real time. The output enable pins determine the direction of the data flow.

LOGIC SYMBOL

'F11652

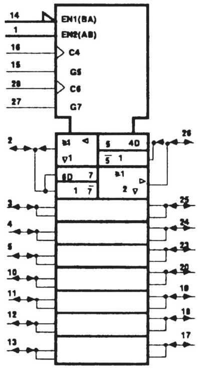


2 3 4 5 10 11 12 13
A0 A1 A2 A3 A4 A5 A6 A7
28 CPAB
27 SAB
1 OEAB
16 CPBA
15 SBA
14 OEBA
B0 B1 B2 B3 B4 B5 B6 B7
26 25 24 23 20 19 18 17

V_{CC} = Pin 21, 22
GND = Pin 6, 7, 8, 9

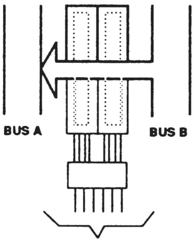
LOGIC SYMBOL(IEEE/IEC)

'F11652



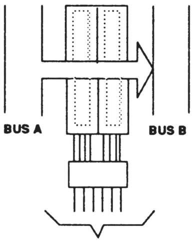
14
1
16
15
28
27
EN1(BA)
EN2(AB)
C4
G5
C6
G7
2
26
3
4
5
10
11
12
13
25
24
23
20
19
18
17

REAL TIME BUS TRANSFER BUS B TO BUS A



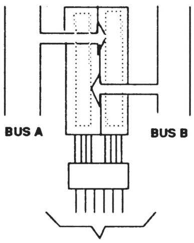
OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER BUS A TO BUS B



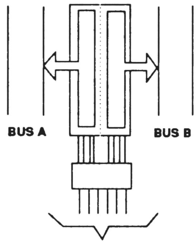
OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



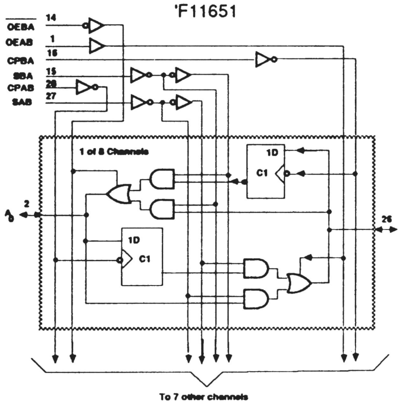
OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

TRANSFER STORED DATA TO A OR B

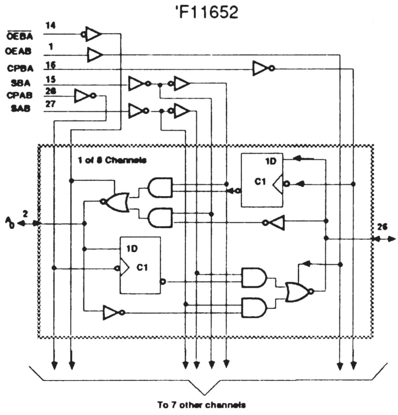


OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

LOGIC DIAGRAM



'F11651
OEBA
OEAB
CPBA
SBA
CPAB
SAB
14
1
16
15
28
27
1 of 8 Channels
1D
C1
1D
C1
A0
2
26
B0
To 7 other channels



'F11652
OEBA
OEAB
CPBA
SBA
CPAB
SAB
14
1
16
15
28
27
1 of 8 Channels
1D
C1
1D
C1
A0
2
26
B0
To 7 other channels

FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA	An	Bn	'F651/'F651A	'F652/'F652A
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B data	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified*	Store A, Hold B	Store A, Hold B
H	H	↑	↑	L	X	Input	output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified*	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	L	output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real time $\overline{B}$ data to A bus	Real time B data to A bus
L	L	X	H or L	X	H			Stored $\overline{B}$ data to A bus	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real time $\overline{A}$ data to B bus	Real time A data to B bus
H	H	H or L	X	H	X			Stored $\overline{A}$ data to B bus	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ data to B bus Stored $\overline{B}$ data to A bus	Stored A data to B bus Stored B data to A bus

NOTES:

H= High voltage level

L= Low voltage level

*= The data output function may be enabled or disabled by various signals at the $\overline{\text{OEBA}}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

↑ =Low-to-High clock transition

X=Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
				I_{OH}=-15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=64mA	±10%V_{CC}			0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	μA
		A_0-A_7, B_0-B_7	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	OEAB, $\overline{\text{OEBA}}$, CPAB, CPBA SAB, SBA	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	μA
$I_{IH}+I_{OZH}$	Off-state current High level voltage applied	A_0-A_7, B_0-B_7	V_{CC} = MAX, V_I = 2.7V					70	μA
$I_{IL}+I_{OZL}$	Off-state current Low-level voltage applied		V_{CC} = MAX, V_I = 0.5V					-70	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				110	145	mA
		I_{CCL}					120	155	mA
		I_{CCZ}					130	170	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

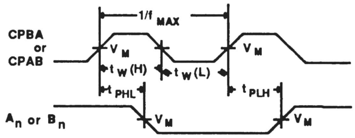
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	90	110		80		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.0 4.5	7.0 6.5	9.5 9.0	4.5 4.0	11.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 2,3	2.0 2.0	5.0 4.5	8.0 8.0	2.0 2.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2,3	4.0 4.0	7.0 6.5	9.0 8.5	4.0 4.0	11.5 9.0	ns
t_{PZH} t_{PZL}	Output Enable time OEAB or $\overline{OEBA}$ to A_n or B_n	Waveform 7 Waveform 8	4.0 5.0	7.0 8.5	9.0 10.0	3.5 4.5	10.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time OEAB or $\overline{OEBA}$ to A_n or B_n	Waveform 7 Waveform 8	4.5 4.5	8.0 8.0	9.5 9.5	4.0 4.0	10.5 9.5	ns

AC SETUP REQUIREMENTS

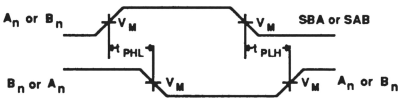
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.0 4.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low[1] $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.5 6.5			4.5 6.5		ns

Note: 1.Setup time is to protect against current surge caused by enabling 16 outputs (64mA per output) simultaneously.

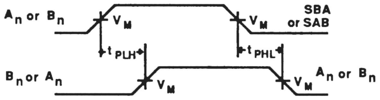
AC WAVEFORMS


CPBA or CPAB
1/f MAX
V M
t W (H)
t W (L)
t PHL
t PLH
A n or B n

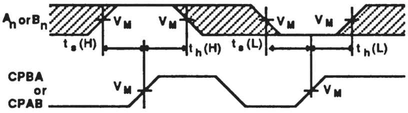
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency


A n or B n
V M
SBA or SAB
t PHL
t PLH
B n or A n
A n or B n

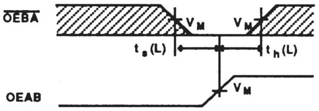
Waveform 2. Propagation Delay, An to Bn or Bn to An and SAB or SBA to An or Bn


A n or B n
V M
SBA or SAB
t PLH
t PHL
B n or A n
A n or B n

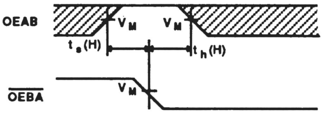
Waveform 3. Propagation Delay, An to Bn or Bn to An and SAB or SBA to An or Bn


A n or B n
V M
t s (H)
t h (H)
t s (L)
t h (L)
CPBA or CPAB

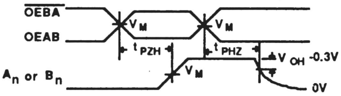
Waveform 4. Data Setup And Hold Times


OEBA
V M
t s (L)
t h (L)
OEAB

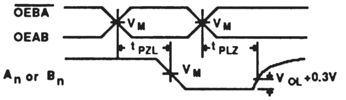
Waveform 5. OEBA to OEAB Setup And Hold Times


OEAB
V M
t s (H)
t h (H)
OEBA

Waveform 6. OEAB to OEBA Setup And Hold Times


OEBA
OEAB
V M
t PZH
t PHZ
V OH -0.3V
A n or B n
0V

Waveform 7. 3-State Output Enable Time To High Level And Output Disable Time From High Level

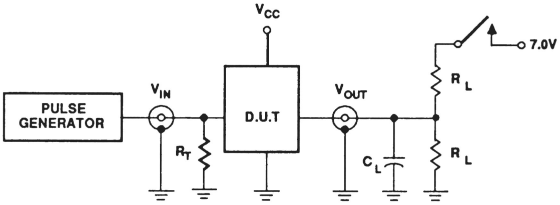

OEBA
OEAB
V M
t PZL
t PLZ
A n or B n
V OL +0.3V

Waveform 8. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

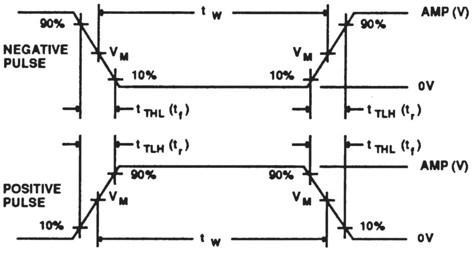
NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V CC
7.0V
PULSE GENERATOR
V IN
R T
D.U.T
V OUT
C L
R L
R L

Test Circuit For 3-State Outputs


t w
AMP (V)
90%
NEGATIVE PULSE
V M
10%
0V
t THL (t f)
t TLH (t r)
POSITIVE PULSE
AMP (V)
90%
V M
10%
0V
t w

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST application notes

AN213

74F30XXX FAMILY APPLICATIONS

High Current Buffers/Transceivers

Application Note

The 74F30XXX Family

- 74F3037 Quad 2-Input NAND, Totem-Pole Buffer
- 74F3038 Quad 2-Input NAND, Open Collector Buffer
- 74F3040 Dual 4-Input NAND Totem-Pole Buffer
- 74F30240 Octal, Inverting, Open Collector Buffer
- 74F30244 Octal, Non-Inverting Open Collector Buffer
- 74F30245 Octal, Non-Inverting, Transceiver
- 74F30640 Octal, Inverting, Transceiver

Major Family Features

- Incident-Wave, 30Ω Transmission Line Drivers
- High Output Currents - I_{OL}/I_{OH} = +160mA/−67mA
- 74FXXX Speeds - Gate Speeds <6.5 ns
- "Flow-Through" Signal Design
- Multiple, Center-Package Supply Pins
- Low V_{CC} Shut-Off Circuit
- Low Impedance Voltage Reference
- Active (Dynamic) Pull-Off Circuit
- "Light-Load" ±20μA NPN Inputs
- Applications Described on Page 6

KEY DESIGN PARAMETERS $V_{CC} = 5.0\text{ V} \pm 10\%$ & $T_A = 0°C$ to $70°C$

SYM	PARAMETER	MIN.	TYP.	MAX.	UNIT
I_{IL}	F3037/38/40, $V_{IL} = 0.5V$, V_{CCmax}			-20	μA
I_{IH}	F3037/38/40, $V_{IL} = 2.7V$, V_{CCmax}			20	μA
I_I	F30240/244 Input Leakage, Hi/Low	-20		+20	μA
I_I	F30245/640 A_N Port I/O Leakage, Hi/Low	-70		+70	μA
I_{OL}	$V_{OL} = 0.55V$, V_{CCmin} (All Devices)	100			mA
I_{OL1}	$V_{OL1} = 0.8V$, V_{CCmin} (All Devices)	160			mA
I_{OH}	F3037/40, $V_{OH} = 2.5V$, V_{CCmin}	-45			mA
I_{OH1}	F3037/40, $V_{OH1} = 2.0V$, V_{CCmin}	-67			mA
I_{OZ}	F30245/640, B_N Hi-Z Leakage, Hi/Low	-70		+70	μA
I_{OL}	F30245/640, A_N, $V_{OL} = 0.50V$, V_{CCmin}	24			mA
I_{OH}	F30245/640, A_N, $V_{OH} = 2.4V$, V_{CCmin}			-3.0	mA
I_O	F3037/40, $V_{OH} = 2.25$, V_{CCmax}	-60		-160	mA
I_{OS}	F3037/40, $V_{OH} = 0.0V$, V_{CCmax}		-300		mA
I_{OS}	F30245/640, A_N, $V_{OH} = 0.0V$, V_{CCmax}			-150	mA
t_P	F3037 Prop. Delays (PD), HL or LH	1.5		6.5	ns
t_P	F30245/640, A_N to B_N PD, HL or LH	1.0		13.5	ns
t_P	F30245/640, B_N to A_N PD, HL or LH	1.0		7.0	ns
t_{PZ}	F30245/640 A_N & B_N Hi-Z PD, HL or LH	1.0		8.0	ns
I_{CC}	F30XXX Per Gate, V_{CCmin}		8		mA
V_{CCZ}	F30XXX Octals, Low V_{CC} Hi-Z Outputs	2.0			Volts
P_{Dmax}	24-Pin Plastic DIP, $T_A = 70°C$, $T_J = 130°C$		1		Watt
θ_{JA}	24-Pin Plastic DIP Thermal Resistance		60		°C/W
θ_{JA}	16-Pin Plastic DIP Thermal Resistance		83		°C/W

Introduction

The Signetics 74F30XXX Family is a new series of very high output current, high performance drivers designed to handle low impedance environments of printed circuit board transmission lines and signal busses. This Family can drive lines with characteristic impedances as low as 30Ω at standard 74F speed.

This Application Note explains how the 74F30XXX's design innovations (2 patents) will give you several major advantages over other high current TTL gate, buffer and transceiver designs. It also illustrates how to use the 74F30XXX's superior characteristics in many applications that currently cannot be handled by standard TTL buffer products.

The totem-pole structure of the 74F3037/40 can easily sink 100mA @ 0.55V (160mA @ 0.8V) and source −45 mA @ 2.5V (−67mA @ 2.0V). The open collector (OC) 74F3038 Quad and 74F30240/244 Octal Buffers use only the 74F3037/40's high current pull-down output structure. The 74F30245/640 Octal Transceivers use high current OC outputs for the B_N port with the A_N port's 3-State outputs able to handle +24/−3mA at TTL (0.5V/2.4V) logic output voltage levels.

Speed is not sacrificed for high output current drive. The 74F30XXX's propagation delays are similar to standard 74F

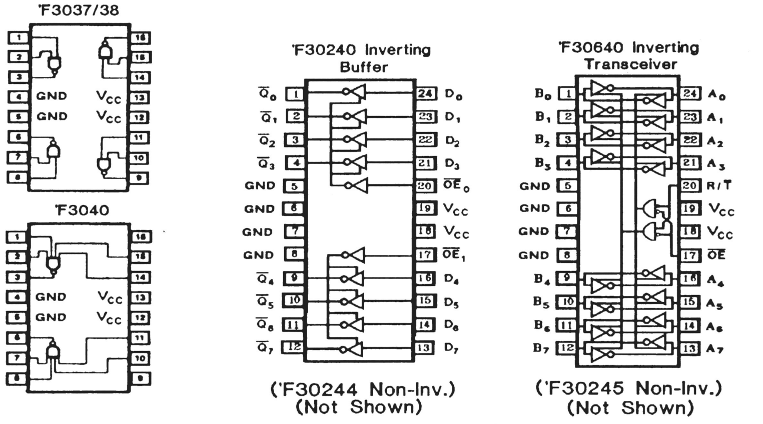

'F3037/38
GND
GND
VCC
VCC
'F3040
GND
GND
VCC
VCC
'F30240 Inverting Buffer
Q̄0 Q̄1 Q̄2 Q̄3 GND GND GND GND Q̄4 Q̄5 Q̄6 Q̄7
D0 D1 D2 D3 OE0 VCC VCC OE1 D4 D5 D6 D7
'F30640 Inverting Transceiver
B0 B1 B2 B3 GND GND GND GND B4 B5 B6 B7
A0 A1 A2 A3 R/T VCC VCC OE A4 A5 A6 A7
('F30244 Non-Inv.) (Not Shown)
('F30245 Non-Inv.) (Not Shown)

Figure 1a. 74F30XXX Block Diagram & Pin Configuration

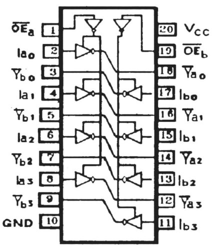

OEa Ia0 Yb0 Ia1 Yb1 Ia2 Yb2 Ia3 Yb3 GND
VCC OEb Ya0 Ib0 Ya1 Ib1 Ya2 Ib2 Ya3 Ib3

Figure 1b. 74F240

devices. As an example, the 74F3037 and the 74F37 both have guaranteed propagation delays between 1.5 and 6.5ns (min/max).

Flow-Through Design

Figure 1a shows the Block Diagrams and Pin Configuration of 5 of the 7 parts of the 74F30XXX Family (74F30244/245 not shown). Notice that each device has at least one ground pin for every two outputs and one V_{CC} pin for every four outputs. Also, the 74F30XXX Octals use a "broadside" design to allow signals to "flow-through" the package. I/O control pins are placed on both sides of the V_{CC} pins.

Comparing the standard 74F240 Pin-Configuration (Figure 1b) with that of the 74F30240, you can see that the 74F30XXX's Flow-through design simplifies the design and layout of large, bus-oriented PC boards.

Input Structures

As shown in Figure 2a (74F3037/40 Circuit Diagram), the input structure is a simple diode AND gate driving the base of Q1. D1 is the input Schottky clamp diode. D2 is the AND input terminal with an input threshold of 2 V_{BE} voltage drops and an I_{IL} (V_I = 0.5V) of 600μA. When all of the inputs are HIGH and one input goes LOW, the input speed-up Schottky diode, D3, discharges the base stored-charge of Q3A & Q3B to ground allowing them to be quickly turned OFF.

A patented "Light-Load" NPN input is used on the inputs of the 74F30240/244 Octal Buffers and the A_N port inputs of the 74F30245/640 Octal Transceivers (Figure 4a). Its input bias current is less than ±20μA for V_I between 0.0V and 5.5V. This NPN input also has a patented NPN transistor turn OFF speed-up circuit (D2/Q2/D4). These patents are discussed in the "Light-Load Input Drivers and Transceivers" Applications Note AN215.

74F3037/40 Output Drive

Figure 3 shows a simplified version of the 74F3037/40's typical output LOW (I_{OL}) and HIGH (I_{OH}) currents versus the output voltage. Note the symmetry of the HIGH and LOW output resistance. As V_{OL} is swept from 0.16V to 5V, R_{OL} (output LOW resistance) changes from ~2.4Ω to ~23Ω. For the same output voltage sweep, R_{OH} (output HIGH resistance) goes from ~23Ω to ~3.6Ω to Hi-Z.

At V_O = 1.5V, the 74F3037's HI and LOW output resistances are approximately 23Ω. If the slope of these sourcing and sinking 23Ω resistances are extended to zero output current, they appear to be switched between equivalent supply busses of +4.75V and -7.75V. This symmetrical output resistance characteristics and the 12.5V apparent output swing are the major reasons that the 74F3037/40 show such excellent 30Ω unterminated transmission line, incident wave switching performance.

Referring to Figure 2a, both Q6 and R8 of the 74F3037/40 are very large area devices producing a relatively large, parasitic capacitance to ground at the collector of Q6. During LOW-to-HIGH output transitions. This 7-10pF capacitance produces a small amount of additional transient I_{OH} drive which helps produce a smooth output transition.

74F3037/40 Output Feed-Through Current

The 74F3037/40's totem-pole output has been designed with virtually no output current spiking or feed-through current. Feed-through current can occur during any output transition when both the pull-up and pull-down output transistors are ON simultaneously. In standard TTL circuits, feed-through current is one of the prime contributors to power supply noise and increased power dissipation with increasing frequency of operation.

To minimize feed-through current, internal circuit delays are used to prevent the upper and lower structures of the 74F3037/40's totem pole output from being ON at the same time. Without this feed-through current, supply plane noise is significantly reduced.

Many standard TTL gate output structures have feed-through currents which are limited only by their pull-up I_{OS} resistors. This condition significantly reduces the amount of output current available during switching transitions. Under heavy load conditions, feed-through can cause non-linearities or flattening in the output switching waveforms. The innovative 74F3037/40 design virtually eliminates feed-through current, allowing the outputs to have significantly more available output transition current and producing very linear output switching transitions.

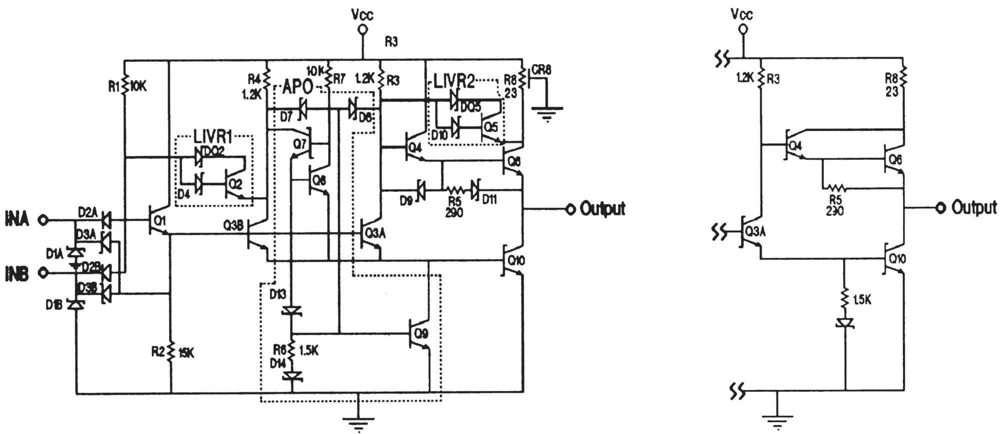


Figure 2a. 74F3037/40 Circuit Diagram

Figure 2b. Non-LIVR Buffer Output

Figure 2. 74F3037/40 Circuit Diagram & Non-LIVR Buffer

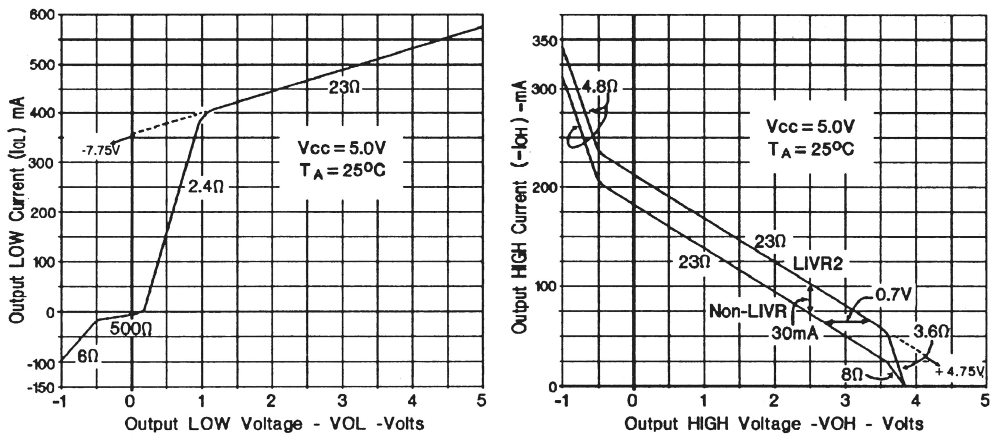


Figure 3a. Output LOW Current
For the 74F3037/40

Figure 3b. Output HIGH Current
For the 74F3037/40 w/ & w/o LIVR

Figure 3. 74F3037/40 Sinking & Sourcing Output Driver Capabilities

Low Impedance Voltage Reference

The patented Low Impedance Voltage Reference is a temperature compensating voltage reference used throughtout the 74F30XXX Family for input speed up (LIVR1) and output noise immunity improvement (LIVR2). The 74F3037 (Figure 2a) is used in the following analyses of the LIVR1 and LIVR2 circuits.

LIVR1 Operation

Refering to Figure 2a, the combination Q1, Q3B and LIVR1 (D4, DQ2 and Q2) is a "kicker circuit" which reduces input propagation delay. LIVR1 is connected between the base of the input transistor, Q1, and the collector of Q3B. When all inputs switch HIGH, current from R1 flows into the base of Q1. Q1's collector-emitter current rapidly turns ON the phase-splitter transistor, Q3A, which turns OFF the output pull-up structure. When the collector voltage of Q3B has dropped sufficiently to forward bias LIVR1, it begins to regulate Q1's base drive, and a low quiescent Q3A/B base drive current is established. With Q1's collector tied directly to Vcc, it cannot saturate and, therefore, can be turned OFF quickly.

LIVR2 Operation

This section compares a standard Schottky Darlington pull-up (non-LIVR Figure 2b) with that of the 74F3037/40's LIVR2 pull-up (Figure 2b). For simplicity, the same circuit resistor values will be used.

Assumptions:

- The Q6 $V_{CE(SAT)}$ of the Darlington output pull-up structure will be aproximatley 0.9V.
- The LIVR2 allows the Q6 $V_{CE(SAT)}$ to drop to 0.2V
- R8, the Ios resistor, for both output HIGH driver circuits is 23Ω.

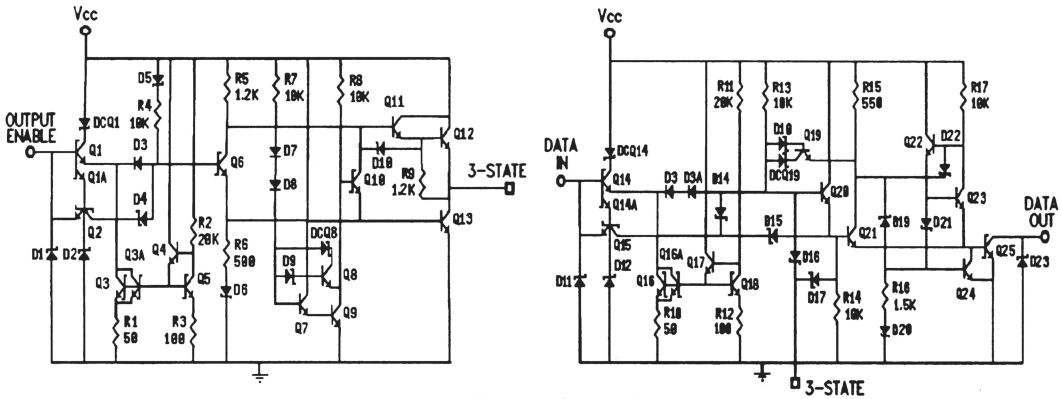


Figure 4a. Output Enable Cell

Figure 4b. Data Cell

Vcc
OUTPUT ENABLE
DCQ1
Q1
Q1A
D5
R4 10K
D3
D4
D1
D2
Q2
Q3A
Q3
Q4
Q5
R1 50
R3 100
R2 20K
R5 1.2K
Q6
R6 500
D6
R7 10K
D7
D8
D9
DCQ8
Q7
Q8
Q9
R8 10K
Q11
D10
Q10
R9 1.2K
Q12
Q13
3-STATE
Vcc
DATA IN
DCQ14
Q14
Q14A
Q15
D11
D12
Q16
Q16A
Q17
R10 50
R11 20K
R12 100
R13 10K
D3
D3A
D14
D18
Q19
DCQ19
D15
Q18
D16
D17
Q20
R14 10K
R15 550
Q21
D19
R16 1.5K
D20
Q22
D22
Q23
D21
R17 10K
Q24
Q25
D23
DATA OUT
3-STATE

Figure 4. 74F30240 Circuit Diagrams

Applications of the 74F30XXX Family

Under these conditions, the LIVR2 output can supply an additional 30mA (23Ω x 0.7V) output HIGH current (I_{OH}) at any specified output HIGH voltage. Also, at the same I_{OH}, the LIVR2 increases V_{OH} by ~0.7V over that of the standard non-LIVR, Darlington pull-up. Refer to Figure 3b.

Active Pull-Off Circuitry

The patented Active Pull-Off (APO) circuit (Figure 2a) consists of a dynamic base discharge and a quiescent pull-off network for the output pull-down transistor (Q10). The APO reduces I_{CCL} (I_{CC} with outputs LOW) requirements by about 30% in comparison to passive pull-off circuits by eliminating the standby pull-off current. This circuit is also part of the timing network for eliminating any totem pole feed-through current.

Low V_{CC} Shut-Down Circuit

In a multi-card bus system where power to one card could be disrupted for any reason, the powerless card must not effect access to the system by the other cards. Systems with common signal busses and power supply planes must continue to operate regardless of any subsystem failure. Many bus driver products in common use today do not provide an output disable circuitry that disables or Hi-Zs all shared system interconnections when V_{CC} drops below its nominal operating range.

The Signetics 74F30XXX octals have solved this problem with a very effective Low V_{CC} Shut-Down circuit. This circuit is shown in the 74F30240's Output Enable Cell (Figure 4a). It detects when V_{CC} falls below 4 V_{BE} voltage drops (R7 biasing D7, D8, Q7 & Q9) then turns Q9 OFF and Q10/Q13 ON by allowing the current through R8 to drive Q10's base instead of being shunted to ground by Q9. This V_{CCZ} value will be >2.0V for T_A = 0° to 70°C.

When Q13 is ON, D16 and D17 (in the 74F30240's Data Cell Figure 4b) shunt the base drive of both Q20 and Q21 to ground. With these transistors OFF, the Data Cell's open collector output (Q25) cannot be turned ON.

The 74F30245/640 Octal Transceivers also have blocking-diodes in the output pull-ups of the A_N port which effectively block any output leakage current through the pull-up path when power is off.

Power Dissipation

The Active Pull-Off and the Low Impedance Voltage Reference circuits used throughout the 74F30XXX Family significantly reduce the I_{CC} over standard advanced Schottky design techniques. In fact, without these innovations, the 74F30XXX Family would not be practical due to lower performance and excessive transient and quiescent power dissipation.

Because the 74F3037/40's totem-pole output has virtually no output feed-through current, I_{CC} does not increase significantly due to increasing frequency. This is not true for most other TTL logic families.

For the 74F30240, the I_{CCH} is about 1/3 of the I_{CCL}. The guaranteed values of I_{CCH} and I_{CCL} are <23mA and <95mA. For reference, the standard 74F240's I_{CCH}/I_{CCL} guarantees are 18/70mA, which is 75% of the 74F30240 version.

The 74F30240 in a 24-pin, 0.3 inch lead centers, plastic dual in-line package is an example of the chip/package power dissipation handling capabilities of the Family:

- With I_{CCL} = 95mA @ V_{CC} = 5.5V, 8 fully loaded outputs @ I_{OL} = 160mA and V_{OL} = 0.5V @ 70°C, the total package power dissipation will be equal to 1.16W.
- Using T_A = 70°C, T_J = 130°C and θ_{JA} = 50°C/W (with an air flow of 200 LFPM) yields a package power dissipation capability of 1.2W.

However, assuming that not all conditions will be worst case simultaneously, the total chip power dissipation should never exceed 1.0W. In designs utilizing 74F30XXX parts near their maximum specified drive capabilities, conservative design precautions dictate that the thermal resistance of the packages be reduced by increasing the air-flow across and/or heat sinking the packages.

Ground & V_{CC} Bounce

A major problem with sourcing and sinking large amounts of current at a dV/dt of >1V/ns is inductance in the ground leads of a package (Figure 5a) which causes "ground bounce" during output transitions due to the load currents being switched ON and OFF. Another component of "ground bounce" in standard TTL circuits is feed-through current which has been eliminated in the 74F3037/40 totem-pole output devices. Changes in output current must overcome the inductances of the package power supply and output leads before being able to drive any load. In doing so, voltages are developed across these inductances which can effect the internal logic thresholds of high-speed logic devices.

V_{CC} bounce is not nearly as critical as ground bounce since a TTL gate's input threshold is referenced only to package ground lead. Also, the V_{CC}-to-output current (I_{OH}) (zero for open collector devices) is usually much smaller than output-to-ground current (I_{OL}).

Figure 5b illustrates the measured lead inductance for both 16- and 24-pin plastic DIPs. Note that the center pins of any PDIP package, being the closest to the chip, have the lowest inductance. Lead length and cross-sectional area equate to inductance. The longer the ground lead, the greater the lead inductance and the larger the ground bounce.

$dV_{GND} = L(dI/dt)$

A comparison of the actual measured lead inductance for 16- and 24-pin plastic DIPs with both corner and center (with and without multiple) supply pins devices is shown below:

#/PINS	PWR PINS	# V_{CC}/GND PINS	EQUIV. IND.
16-Pins	Corner	16/8	10.5nH
16-Pins	Center	12/4	3.3nH
16-Pins	Center	12,13/4,5	1.7nH
24-Pins	Corner	24/12	18.1nH
24-Pins	Center	18/6	3.7nH
24-Pins	Center	18,19/5,6,7,8	1.9/1.2nH

On the 24-pin PDIP the ratio between the lead inductance of a single, corner ground lead (18.1nH) and 4 center grounds (1.2nH) is 15:1.

Using the example of a 74F30240 with all eight outputs switching simultaneously from a HIGH-to-LOW state into 30Ω loads, I_{CC} changes plus the total output current into the ground lead will be:

dI_{CC} = 95mA(LOW) - 23mA(HIGH) = 72mA

dI_{OUT} = 8 x (5.0V-0.5V)/30Ω = 8 x (0.15A) = 1.2A

$dI_{GND} = dI_{CC} + dI_{OUT}$ = 72mA + 1.2A = 1.27A

For 1 Corner Ground Pin - L_{GND} = 18.1nH

$dV_{GND} = L(dI/dt)$ = 18.1nH x (1.27A/2ns) = 11.5V

For 4 Center Ground Pins L_{GND} = 1.2nH

$dV_{GND} = L(dI/dt)$ = 1.2nH x (1.27A/2ns) = 763mV

In use, the internal ground bounce will not actually reach these calculated voltage levels. The ground bounce is divided between the equivalent inductance in series with the 8 outputs (paralleled 1.6nH) and the 4 ground supply pins' equivalent inductance (1.2nH).

Also, because the length of the PC board trace to any load increases the effective output lead inductance and, because the supply pins are tied to large, low inductance supply planes, the ground bounce voltage is significantly reduced by dividing the potential ground voltage rise between the output and supply inductances.

Minimizing the effects of supply bounce on the internal logic threshold levels of TTL logic chips allows faster systems to be built. If corner supply pins parts are used, the logic LOW level threshold can be jeopardized by ground bounce, whereas, the ground bounce on the 74F30240/244/245/640 chips, with their multiple, center supply pin design, only effects the chip's thresholds by <0.7V during HIGH-to-LOW transitions.

Living with Ground Bounce

If non-inverting buffers and transceivers (74F30244/ 245) are used, the ground bounce actually enhances the noise immunity of the chip. Changes in the current through the ground lead inductance reinforce the input thresholds by creating a very effective dynamic input hysteresis.

Care should be taken to minimize supply bounce during output switching transitions. These include minimizing supply lead inductance by keeping their PC board traces as short and as wide as possible. Inductance in the output lead actually reduces supply bounce as mentioned earlier.

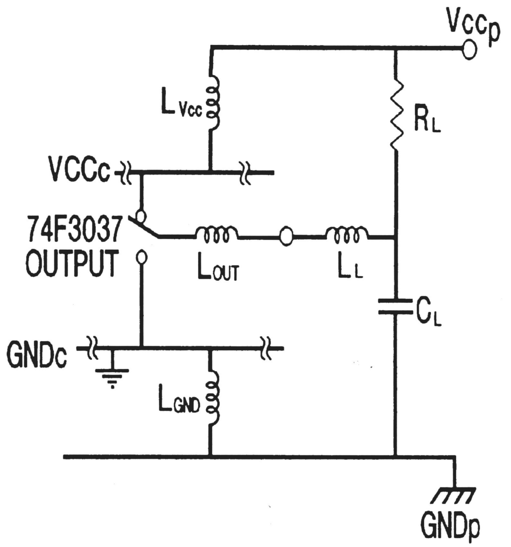


Figure 5a. Plastic DIP Lead Inductance

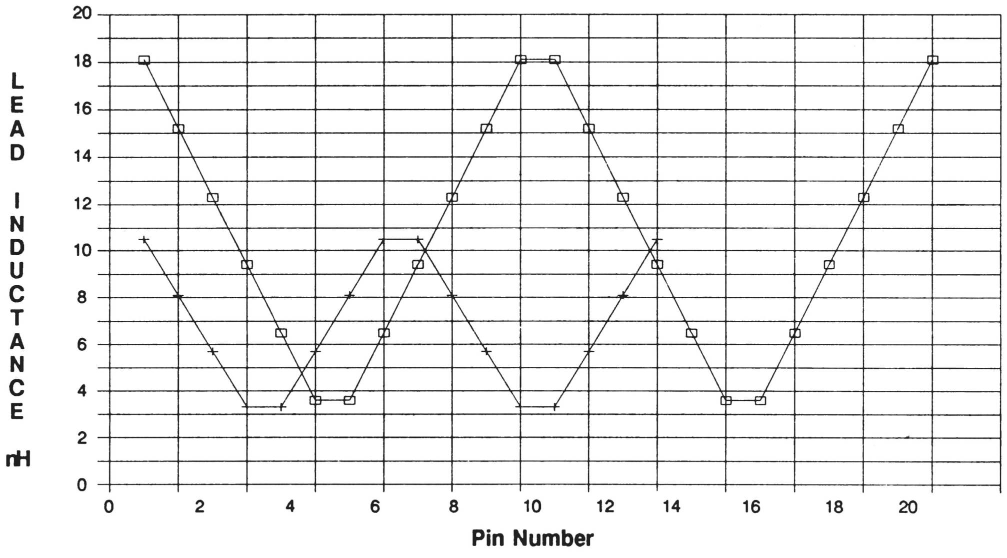


Figure 5b. Lead Inductance Per Lead for 16- & 24-Pin Plastic DIPs

High Performance Transmission Line Drivers

Introduction

The use of the 74F30XXX Family devices in high performance printed circuit board applications requires an understanding of some fundamental transmission line principles. It is assumed that you have some background in transmission line theory. Because of the unique requirements of every system, specific PC board design techniques will not be covered. The Signetics ECL Manual has some good background information on high performance PC board design.

This Application Note is intended to provide enough practical information to utilize the significant high performance advantages of the 74F30XXX Family in driving low impedance, high performance PC board transmission lines.

Incident wave signal switching of a transmission line requires the driver be able to achieve and maintain initial TTL input logic levels without having to wait for a signal reflection. The driver must also be able to continue to supply enough sinking and sourcing current to guarantee good noise margin during line reflections or crosstalk.

With standard TTL buffers unable to support incident wave switching, waiting for a reflection before a driver can achieve solid TTL input logic levels would be a major source of system timing error and noise. The reflected signal will take several nanoseconds to return to the driver source. During this time, the incident signal level could be in the input threshold region of a receiving gate creating the potential for that gate to oscillate or detect incorrect logic states.

PC board busses and backplanes usually have low, irregular characteristic impedances, Z_O, and are difficult to terminate properly (See Figure 6). To obtain incident wave switching of TTL voltage levels in this environment requires very high current drivers. Where proper termination is impractical, the 74F3037/40 Totem-Pole Output Gates could be the only solution. They can drive unterminated transmission lines of $Z_O \geq 30\Omega$.

All 74F30XXX devices can drive properly terminated, low impedance transmission lines. When the line is correctly terminated, during the LOW-to-HIGH output transition, the driver output (whether open collector or totem-pole) will switch to V_{EQ} (the equivalent termination voltage) in <2ns, as if it were driving a resistor network tied directly to the output. If the V_{EQ} is less than 5V, the Family can also drive line impedances lower than 30Ω (See Figure 6b):

$$Z_O = dV/I_{OL} = [V_{EQ} - V_{OL}]/I_{OL}$$

where:

$$V_{OL} = 0.5V \; @ \; I_{OL} = 160mA$$

$$Z_O \; (V_{EQ} = 5.0V) = [5.0V - 0.5V]/160mA \cong 30\Omega$$

$$Z_O \; (V_{EQ} = 3.0V) = [3.0V - 0.5V]/160mA \cong 16\Omega$$

When a buffer or transceiver is placed in the middle of a 70Ω PC board (typical) bus transmission line, its output sees two paralleled 70Ω impedances or 35Ω. With this heavy loading, standard TTL buffer outputs cannot generate TTL input logic level. However, the 74F30XXX Family was developed specifically for these types of difficult bus driver applications.

Characteristic Impedance

A driver switching the voltage onto a transmission line will see neither capacitance nor inductance but primarily resistance. This resistance, Z_O, is the characteristic impedance of the transmission line. The characteristic line impedance is calculted by:

$$Z_O = \sqrt{[L_D/(C_D + C_i)]}$$

where: (See Figure 6)

C_D = Distributed Capacitance Per Unit Length
C_i = Total Input Capacitance Per Unit Length
L_D = Distributed Inductance Per Unit Length

In large device arrays such as memory PC boards, C_D, C_i and L_D (and therefore Z_O) are determined primarily by both the pitch of the package pins and the pitch the package placement rather than the number of devices attached to a bus. Example, SIP (single in-line packages) memory chips can be placed much closer together than

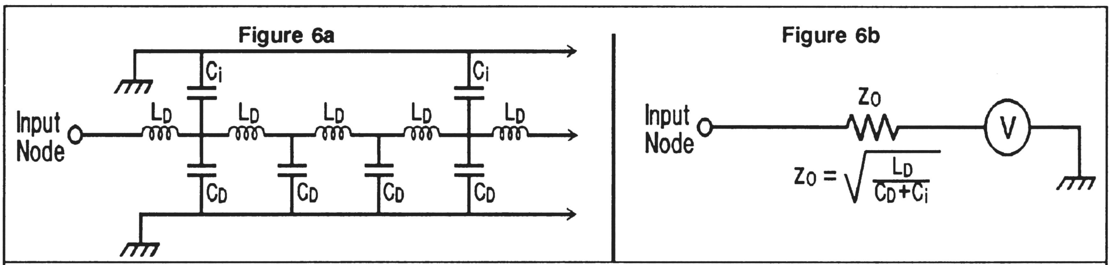


Figure 6a

Figure 6b

a.... A simplified signal bus or transmission line model showing the first 2 DRAM inputs on the line. C_i is a DRAM's input capacitance. C_D is the distributed PC trace capacitance. L_D is the distributed PC trace inductance.

b.... Equivalent circuit for the Input Node. If Z_O is given by the equation shown. The current to drive the Input Node is: $I_{OL} = V_{EQ}/Z_O$, where V is the difference between the Input Node voltage and the quiescent voltage on the line.

Figure 6. Transmission Line Model

can DIPs. Therefore, the input capacitance per unit length of the PC trace, C_i, can be much larger for SIPs than for DIPs, which reduces Z_0. Also, the newer surface mount packaging technologies tend to produce transmission lines with lower characteristic impedance than through-hole (DIP/SIP) technologies.

Line Propagation Delays & Reflections

The basic resistive characteristic of Z_0 and the signal propagation speed of transmission lines, regardless of their termination, is a function of its cross section area and distributed/mutual L & C. The line termination determines only the magnitude and polarity of the reflected signal, not the initial impedance seen by a bus driver.

Three rules of thumb:

- Modern PC board designs can easily produce transmission lines with Z_0 of 70Ω or lower.
- Signal propagation speeds will be in the 1.5ns per foot range. Although, with very large distributed input capacitance per unit length (C_i), 4.5-5.0ns/ft is possible.
- An abrupt change in Z_0 causes a signal to be partially reflected. $V_{(reflected)}/V_{(incident)}$ is determined by the impedance immediately before and after the change. The magnitude of the propagated and reflected signal voltages will be::

$$V_{(ref)} = V_{(inc)}[(Z_1 - Z_0)/(Z_1 + Z_0)]$$
$$V_{OUT} = V_{(inc)} + V_{(ref)}$$
$$= 2V_{(inc)}[(Z_1)/(Z_1 + Z_0)]$$

where:

$V_{(ref)}$ = Reflected Signal Voltage
$V_{(inc)}$ = Incident Signal Voltage
V_{OUT} = Total Propagated & Reflected Signal
Z_0 = Incident Line Z_0
Z_1 = Next Section Line Z_0

Also, because of the real-world limitation of PC board design, the characteristic impedance of a line will change at different points along the line. These impedance variations will cause reflections. However, since the driver only has one shot at incident wave switching of a line (at the driving point), the signal wave traveling away from the source should initially encounter the lowest line impedance followed by incrementally increasing or the same characteristic impedances, if possible.

When the transmission line's Z_0 decreases, the propagating signal voltage will be reduced and a negative reflection generated. Also, if the propagating signal sees an increase in Z_0, the signal voltage will be increased and a positive reflection voltage will be generated.

Incident Wave Switching Line Drivers

When comparing logic families, you will find that the 74F30XXX drivers are the only products available which are able to handle incident wave switching into a 30Ω transmission line. Under very heavy loading, the 74F3037/40 outputs produce significantly greater HIGH logic level noise margin than any competing standard device.

The 74F3037/40 has been designed specifically for the higher current and speed requirements of high performance PC board busses and transmission lines where the Z_0 may have significant variations. Their totem-pole output structure provides enough current drive capability to force TTL input logic levels into a 30Ω load tied to either V_{CC} or GND.

Figure 7 illustrates the excellent noise immunity provided by the totem pole output structure of a 74F3037 output (P_0) driving a 40", 30Ω transmission line terminated with only the input of another 74F3037 (P_1). The 40" line's propagation delay is about 5ns or t_{TPD} = 1.5ns/ft. The waveforms are simplified to illustrate the concept. In an actual system, you could expect to see many small reflections traveling along the transmission line.

Since the line is nearly an open circuit at P_1, the 4.0V HIGH-to-LOW output transition tries to double when it arrives at P_1 (+5ns), driving P_1 negative until the input clamp is forward biased. This signal is reflected back to the P_0 source (+10ns), pulling it below ground momentarily.

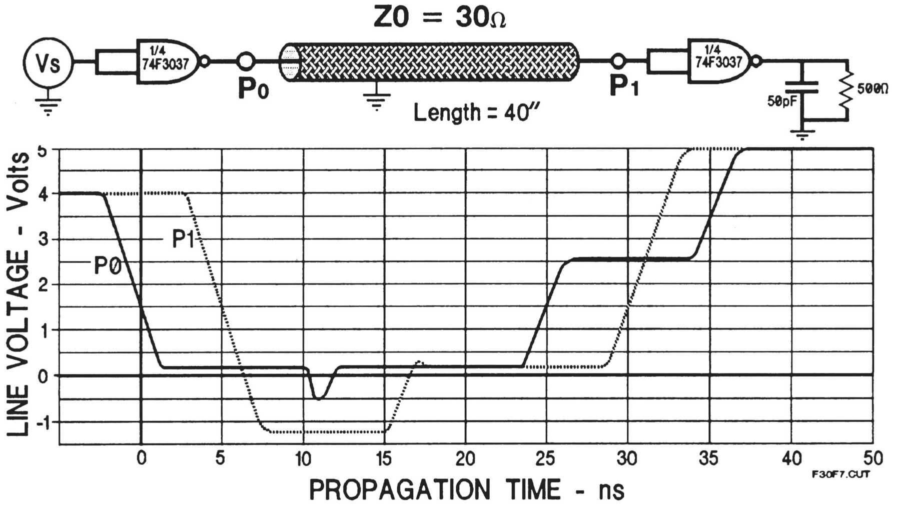


Figure 7. 74F3037/40 Driving Unterminated 30Ω Transmission Line (Simplifed

At the LOW-to-HIGH output transition, the 74F3037 initially achieves a full 2.5V level before running out of steam. The 2.5V signal travels down the line to P_1 (+5ns) where it is doubled and reflected. The reflected signal arrives back at P0 (+10ns), reenforcing the HIGH level to nearly 5.0V and completely turning off the 74F3037 pull-up structure. With the pull-up structure OFF, no additional charge can be pumped into the line, and the line voltage stops rising.

Open Collector Buffers & Transceivers

Figure 8 is an illustration of a typical multi-tap 70Ω transmission line with each end terminated by a resistive voltage divider producing a V_{EQ} = 3.0V and R_{EQ} = Z_O = 70Ω. As shown, one of the B_N port outputs of a 74F30245 Open Collector Octal Transceiver (with no output pull-up resistor) can be placed anywhere along the middle of a transmission line (PC board trace). This output has to drive the equivalent of two paralleled 70Ω ($Z_O/2$ = 35Ω) transmission lines tied to 3.0V.

During the LOW-to-HIGH driver output transition, the OC driver output turns OFF, and the signal snaps up to 3.0V in less than 2ns. The output reacts as if it were tied to a 3.0V, 35Ω resistive termination. No reflections of the incident signal voltage occur from either end of the transmission line because both are terminated with Z_O. These terminations also absorb the HIGH-to-LOW output transition signal voltage without reflection.

Crosstalk

Crosstalk signals or injected noise can be inductively and/or capacitively coupled between two parallel signal lines. Crosstalk between adjacent transmission lines can be significant with large mutual inductance and capacitance even when the ends of the transmission lines are correctly terminated or tied to a line driver.

Crosstalk noise travels down a transmission line (similar to actual data) and is absorbed or reflected at the terminations at each end of the line.

Crosstalk noise is a basic characteristic of the physical layout of adjacent transmission lines, not a failure of the driver. Long parallel signal lines can have a fairly high mutual inductance and capacitance if care is not taken in their design. The increased crosstalk due to narrower spacing between lines could pose system problems as denser memory and surface mount technology (SMT) packaging become more popular.

Shielding should be used to reduce the electromagnetic and electrostatic field strengths between adjacent lines. Multilayer PC boards significantly reduce mutual inductance and capacitance by isolating signal planes from each other through the use of alternating signal and ground planes. Further isolation can be achieved by inserting narrow, grounded filaments between each signal line on the same wiring plane.

Concerns that the 74F30XXX Family can produce more crosstalk is valid. However, the Family was specifically designed to drive large amounts of output current at very high speeds. Therefore, PC board design must take into consideration the high output current and fast edge rates generated by 74F30XXX devices.

Negative Reflections Cause MOS Failures

If the minimum input voltage specification of -1.0V is exceeded, the reliability of MOS devices can be seriously degraded. Transmission lines using end termination techniques should be incorporated into high performance PC board designs to minimize the negative excursion of reflected signals. Correct line termination is essential to prevent blowing up MOS device I/O ports connected to PC board bus lines!

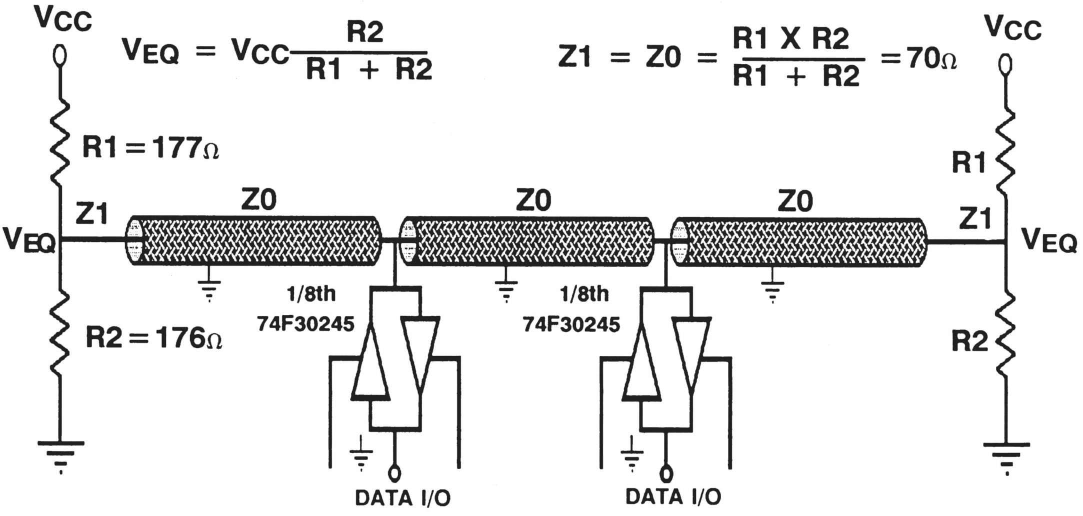

Vcc
$V_{EQ} = V_{CC}\frac{R2}{R1 + R2}$
$Z1 = Z0 = \frac{R1 \times R2}{R1 + R2} = 70\Omega$
Vcc
R1 = 177Ω
R1
Z1
Z0
Z0
Z0
Z1
VEQ
VEQ
1/8th
74F30245
1/8th
74F30245
R2 = 176Ω
R2
DATA I/O
DATA I/O

Figure 8. 74F30245 Multiple-Tap, Correctly Terminated 70Ω Transmission Line Transceiver

Summary of Recommendations

Significant factors influencing PC board designs are easily overlooked. Here are a few recommendations that must be taken into consideration:

- Keep signal line lengths as short as possible to reduce crosstalk, reflections and signal timing skews. Break long lines into shorter parallel lengths.
- In applications where there can be significant variations in Z_O, use 74F3037/40 Totem-Pole output drivers. If possible, terminate a transmission line with an impedance that is equal to or slightly higher than the Z_O at the terminal end of the line. If variations in Z_O must occur, Z_O should increase as the distance from the driver increases. Try to keep the incremental Z_O changes per unit length of transmission line to a minimum.
- To keep the negative reflected voltage at the I/Os of MOS devices less than 1.0V, correctly terminate the end(s) of the signal transmission line. For additional protection, you can also use the Schottky clamp diodes available across all I/O pins of Signetics' 74FXXX and 74F30XXX devices.
- The most elegant solution to driving low Z_O transmission lines is to use the Signetics 74F30XXX Octal Open Collector Output Buffers and Transceivers. If both ends of the line are terminated with its characteristic impedance (Z_O), these drivers can be tapped into any point along the line. Direct and injected crosstalk signals are absorbed at the end terminations minimizing system noise. The line driver will see heavy, predominantly resistive loads.
- Since you now need the speed and drive capabilities of the 74F30XXX Family, you are automatically in the high performance end of the speed spectrum. In these high-speed applications, multi-layer PC boards are virtually mandatory. Keep the ground paths as wide and as short as possible to minimize induced ground noise.
- Capacitively bypass the supply pins of all devices with a 0.1 - 0.33μF ceramic and/or tantalum capacitor as close to the supply pins as possible.

High Current Driver Applications

Figure 9 illustrates that under controlled conditions, the open collector 74F30240 and 74F30244 Octal Buffers can be used to drive eight power MOSFETs, lamps (incandescent and LED), solenoids and relays.

Octal Power MOSFET Driver

Power MOSFETs are well known for their extraordinary switching speeds -- much faster than the best power bipolar transistors of equivalent current/voltage handling capabilities. When comparing MOSFETs to equivalent power bipolar transistors, MOSFETs exhibit many advantages:

- Turn ON & OFF in 2ns vs. Bipolar's 200ns
- Negative vs. Positive Gain Tempco — No Thermal Run-Away Characteristic
- Gate Turn-ON Thresholds Between 2V and 6V
- Low R_{ON} with 0V V_{DS} offset vs. $V_{CE(OFFSET)} > 0.15V$
- $R_{ON} < 0.15$ Ohm @ $I_{DS} > 10A$
- Voltage-to-R_{ON} vs. Current-to-Current Amplification
- Capacitive AC Input vs. Current Base Drive Equivalent Gate Capacitance <2000pF
- Low Cost 50V to 250V Power Transistors @ >12A

The rise/fall switching speeds of MOSFETs are of primary consideration in high efficiency switching applications such as switched mode power supplies. The 74F30244 Buffer can easily switch an equivalent power MOSFET gate capacitance of 1000pF in <50ns.

An excellent example of today's leading edge power MOSFETs is the Siliconix BUZ71. At 25°C, the BUZ71's specifications are:

- V_{GSON} = ON Gate-Source Threshold <5.0V
- I_{DSON} = Drain-Source ON Current >12A
- V_{DSO} = Drain-Source Breakdown Voltage >50V
- R_{DSON} = Drain-Source ON Resistance <0.150Ω
- C_{GS} = Gate-Source Capacitance <650pF
- C_{DG} = Drain-Gate Capacitance <160pF
- P_{DSON} = Chip ON Power Dissipation <22W
- P_L = Power to Load = 500W

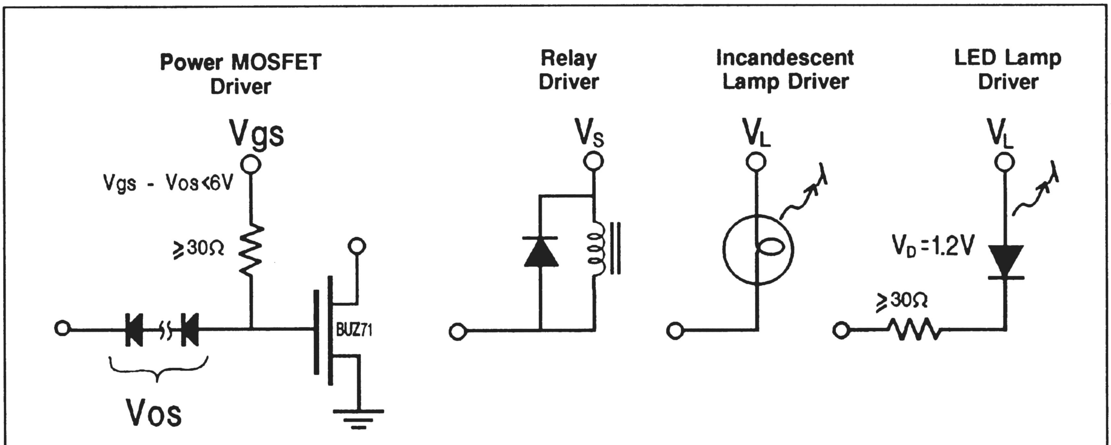


Figure 9. High Current driver Applications

The high current capabilities of the 74F30244 can easily drive the AC loading of the 650pF gate-source capacitance and 160pF drain-gate Miller capacitance. However, an offset voltage (Vos = 3 Schottky diodes or more) should be provided to speed the LOW-to-High transition and increase the gate supply voltage. Since power MOSFETs are very fast and an oscillating driver could cause load switching problems, a non-inverting driver (such as the 74F30244) should be used to take advantage of the dynamic input threshold hysteresis generated by ground bounce.

Octal Solenoid or Relay Drivers

Since solenoids and relays are inductive circuit elements, the ON load current exponentially increases from zero to quiescent value of current. When the driver tries to turn OFF the load current, a quenching diode, placed across the coil, prevents the output of the driver from being damaged by the coil's back-EMF inductive kick.

A 74F30240 can easily handle eight 160mA, 5V solenoid or relays with the back-EMF diodes in place.

Octal Incandescent Lamp Drivers

All incandescent lamps have positive filament resistance temperature coefficients. At room temperature, a lamp's filament resistance can easily be less than 10% of its ON resistance. Therefore, a 100mW (5V at 20mA) lamp could have a cold or inrush current of 200mA. The absolute maximum output LOW current specified for the 74F30XXX Family is 320mA. For this reason, we suggest that the inrush not exceed 320mA in incandescent lamp applications. Therefore, assuming a 10:1 ON:OFF resistance ratio, the ON current should be in the 32mA range. Outputs may be paralleled for additional output drive current.

When the lamp is turned ON, the initial filament current exponentially decays to the quiescent ON current within 10 to 100ms depending upon its size. When the lamp is turned OFF, the thermal decay time constant is very long compared to the turn-ON time constant, greater than 100 times, since the filament, being in a vacuum, has a very high thermal resistance. Therefore, the only time the inrush or cold filament current must be taken into consideration is in applications in which the lamp is OFF for seconds.

Octal LED Lamp Drivers

LEDs (Light Emitting Diodes) have none of the inrush current problems of incandescent lamps. Low cost LEDs are available with spectral emissions from infrared (IR) to green. The intrinsic forward-biased diode voltage drop ranges from 1.2V to 1.6V, depending on the technology -- GaAs, GaAsP, as well as other mixtures. Visible LEDs, red-yellow-green, are used as indicators and don't require fast switching times. If the design requires low cost, high current octal LED drivers, the 74F30240/244 Buffers are excellent solutions.

IR LEDs are used in communications applications where the receiver is a photo-sensitive semiconductor material. Silicon PIN diodes make excellent, very high- speed receivers for emmissions of IR LEDs. Both the emitter's spectral energy output and the receiver's maximum spectral sensitivity are in the 900Å range. The 74F3037 is an ideal Fiber Optic Communications (FOC) IR LED transmitter driver.

Fiber Optic Communications (FOC)

74F3037 FOC LED Driver

High performance, low cost FOC LED transmitter drivers using the 74F3037 can achieve data rates greater than 170MBaud depending upon the length of the fiber optic cable. Using 5% tolerance components, 1/2 of a 74F3037 and a Hewlett-Packard HFBR-1402.4 FOC LED, a one kilometer, 170MBaud FOC link can be produced with an optical output pulse width distortion of less than 15% (See Figure 10). Since the FOC LED is much harder to turn ON than OFF, the 74F3037's fast, HIGH level turn ON and large pull-up output current is nearly an ideal combination for high-speed fiber optic communication. The peaking capacitor, C, compensates for the LED's slow turn-ON time and peaks the LED's light output during both the ON and OFF transitions. Contact Hewlett-Packard's Optical Communication Div., San Jose, CA, for more information on FOC LED transmitters, PIN photo diode receivers and fiber optic cable.

FOC Photo PIN Diode Receiver

The receiver consists of an HP HFBR-2208 Photo Pin Diode driving a Signetics NE5212 Transimpedance Current, Differential Amplifier followed by a Signetics 10116 Triple ECL Line Receiver. The Trans-Z Amp's ~7KΩ (single-ended) internal feedback resistance converts the PIN diode's photon generated currents into 100mV differential output swings. The NE5212's outputs are capacitively-coupled into the input of the 3-stage ECL amplifier where it is quantized into solid ECL logic levels in the last stage.

The NE5212 Trans-Z Amp has a nearly flat DC-to-120MHz bandwidth. Contact Signetics Linear Division for more information on this and many other FOC products.

One more important point ---- the cost of this FOC transmitter/receiver pair is less than $50 using off-the-shelf standard parts.

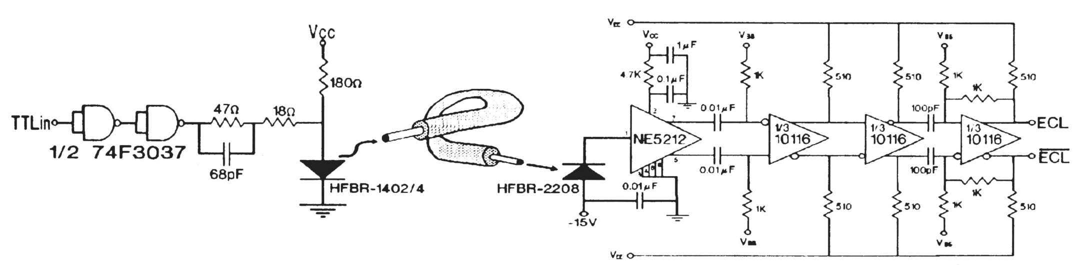


Figure 10a. FOC Transmitter

Figure 10b. FOC Receiver

Figure 10. 74F3037 Fiber Optic Communications Applications

AN214
74F Extended Octal–Plus Family Applications

Application Note

74F Extended Octal-Plus Family Features

- 8-, 9- & 10-Bit "Light-Load" Bus Products
  - Buffers/Drivers
    - With & Without Latches or Registers
    - With & Without 8-Bit Parity Checker/Generator
  - Tranceivers
    - With & Without Dual Registers
    - With & Without 8-Bit Parity Checker/Generator
- Patented "Light-Load" Inputs:
  - Input Current = ±20µA per Input
  - Transceiver I/O Pins = ±70µA
- High Performance Output Drive Currents:
  - I_{OL} = 64mA/48mA @ ±5%/10% V_{CC}
  - I_{OH} = –15mA/–3mA @ ±5%/10% V_{CC}
- "Flow–Through" or "Broadside" I/O Pin-Configuration
- Ideal for MOS CPU, Peripherals and Semi-custom Bus Interface
- 24-Pin, 300mil, Plastic Slim-DIPs
- High Performance Buffers – – – – – $t_{P(max)}$ = 7.5ns
- High Performance Latches/Registers – f_T = 100MHz

Introduction

The 74F Extended Octal-Plus© Family incorporates all of the latest Signetics' octal, 9–bit and 10–bit buffer, transceiver, latch and register functions. All devices in this Family utilize the Signetics patented "Light–Load" NPN, ±20µA input current structure and have "Flow–Through" or "Broadside" input/output pin configurations where the inputs and outputs are lined–up on opposite sides of a standard 24–pin Slim–DIP package. The "Light–Load" inputs, "Broadside" design and high functional density/performance of the Family make this product line ideal for buffering the limited drive capabilities of standard, custom and semicustom MOS VLSI devices to the rigorous environments of today's leading edge high performance logic designs. The Family also is an excellent choice for all general interface applications.

"Flow–Through" Design

The "Flow–Through" or "Broadside" chip layout/package design is illustrated in Figure 214–1 showing the Block Diagrams and Pin Configurations of the 74F828 10–Bit Inverting Buffer. Note that all of these "Broadside" designs allow logic signals to flow into one side and out of the other without crossing or folding back on signal paths such as the 74F240 Octal Buffers (Figure 214–2). If you compare the physical layout requirements of the path of PC board bus lines for the 74F828 to that of the 74F240's "Zig-Zag" path, you will see the significant advantages of the 74F Extended Octal–Plus© Family's "Flow–Through" design in simplifying the design and layout of large, high density, bus–oriented PC boards.

The 24–Pin, 300mil Slim–DIP Solution

With the advent of advanced Schottky TTL technology came the ability to significantly increase the functional density of standard logic building blocks. However, not until the development of the 24–pin, 300mil Slim–DIP package was it possible to take full advantage of these new chip densities. The entire Family provides significant advantages in package count, pin count and packing density when compared to older technologies. Further density enhancements can be achieved by using Signetics' surface mounted packages.

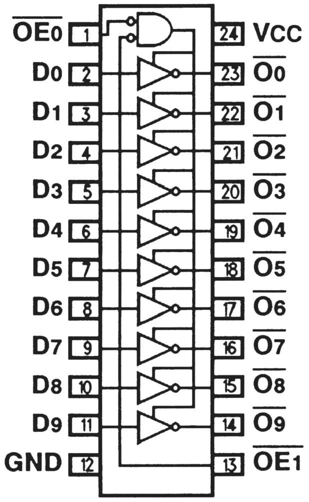


Figure 214-1. 74F828 Broadside Pin Configuration

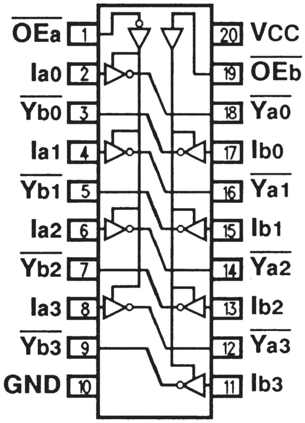
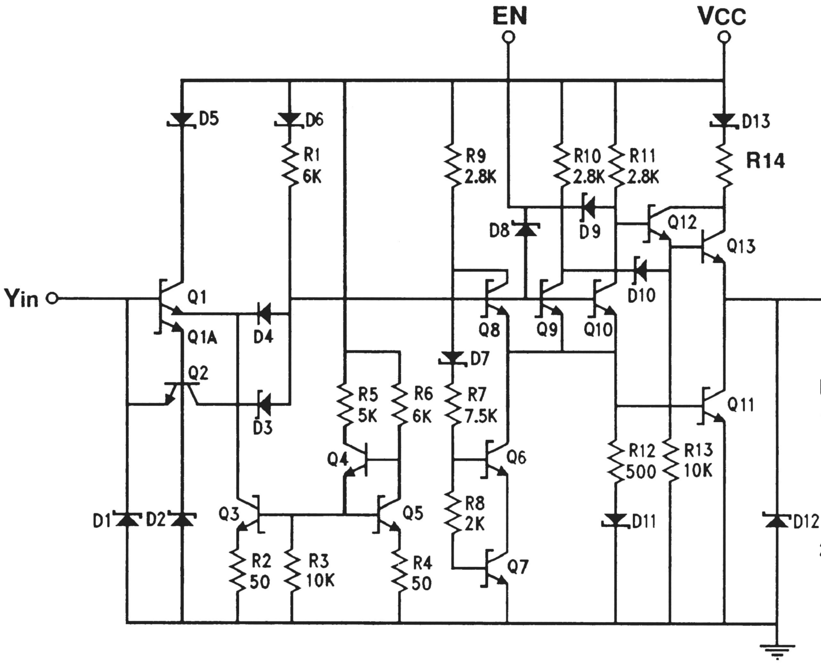


Figure 214-2. 74F240 "Zig-Zag" Pin Configuration

74F Extended Octal-Plus Family Applications

AN214



I_{OL} Options:

1) If I_{OH}/I_{OL} = –15/64 mA

R14	=	12 Ω
R11	=	2.8K Ω
R10	=	2.8K Ω
R12	=	500 Ω

2) If I_{OH}/I_{OL} = –3/24 mA

R14	=	30 Ω
R11	=	5K Ω
R10	=	5K Ω
R12	=	2K Ω

Figure 214–3. 74F455 Buffer/Drive Cell Circuit Diagram

By combining high functional density into a 24–pin, 300mil Slim–DIP package, the Signetics 74F Extended Octal–Plus© Family allows the reduction of PC board parts count and cost while optimizing layout with "Broadside" chip designs, reducing total system power dissipation and increasing system reliability.

The 8-, 9- & 10-Bit Series 24–Pin Solution

Whether your system requires an 8-, 9- or 10-bit bus interface, the Extended Octal-Plus© Family has standardized solutions in 24–pin/Slim–DIP/Broadside input/output packages with corner power supply pins (12 & 24) and standard designations for common control functions located at or near the package corners. Octals offer more mode control inputs than do the 9– or 10–bit products. Virtually all Family devices with 3–State outputs are guaranteed to source/sink –15/64mA @ V_{OH}/V_{OL} = 2.0/0.55V (Except for the 74F841–846 Latched Drivers which are spec'ed at –15mA/48mA). The A_N port outputs of several of the Family's transceivers are guaranteed to supply -3mA/48mA).

The Octal Parity Bus Series offers several notable exceptions to the above standard pinouts. This Series has three parts with two center–package ground pins to minimize ground–bounce noise. All outputs (except the A_N port of the 74F657 Parity Bus Transceiver spec'ed at -3mA/24mA) are guaranteed to source/sink more than –15mA/64mA.

Table 214–1. Family Output Drive Capabilities using the 74F657 Parity Bus Transceiver

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions, V_{IL} = MAX and V_{IH} = MIN)

PARAMETER			TEST CONDITIONS		Min	Typ	Max	UNITS
V_{OH}	HIGH–level Output Voltage	All Outputs	I_{OH} = –3mA	± 10%V_{CC}	2.4			V
V_{OH}	HIGH–level Output Voltage	All Outputs	I_{OH} = –3mA	± 5%V_{CC}	2.7	3.4		V
V_{OH}	HIGH–level Output Voltage	B_N Port, PARITY $\overline{\text{ERROR}}$	I_{OH} = –15mA	± 10%V_{CC}	2.0			V
V_{OH}	HIGH–level Output Voltage	B_N, PARITY $\overline{\text{ERROR}}$	I_{OH} = –15mA	± 5%V_{CC}	2.0			V
V_{OL}	LOW–Level Output Voltage	A_N Port	I_{OL} = 24mA	± 10%V_{CC}		0.35	0.50	V
V_{OL}	LOW–Level Output Voltage	A_N Port	I_{OL} = 24mA	± 5%V_{CC}		0.35	0.50	V
V_{OL}	LOW–Level Output Voltage	B_N Port, PARITY, $\overline{\text{ERROR}}$	I_{OL} = 48mA	± 10%V_{CC}		0.40	0.55	V
V_{OL}	LOW–Level Output Voltage	B_N Port, PARITY, $\overline{\text{ERROR}}$	I_{OL} = 64mA	± 5%V_{CC}		0.40	0.55	V
I_{OS}	A_N Output HIGH Level Short Circuit Current (R14 = 30Ω)		VCC = MAX.				–150	mA
I_{OS}	B_N Output HIGH Level Short Circuit Current (R14 = 12Ω)		VCC = MAX.				-225	mA

74F Extended Octal-Plus Family Applications

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Current PC board, multi–layer technology make it possible to take into consideration the physical location of input/output pins, transmission line characteristics and supply power distribution. Lining up all inputs and output on opposite sides of the package allows the address, data and control bus signal to flow in a direct physical path from the µP CPU through the bus interface chips and onto the appropriate bus. This "Broadside" bus design approach produces very clean PC board layouts and may, in fact eliminate an entire PC board interconnection layer. Standardization of power supply, mode control and input/output pins whether 8-, 9- or 10-bit bus functions permits simplified, structured PC board layout.

Input Structures

Referring to Figure 214–3, the 74F455 Inverting Buffer/Driver Cell Circuit Diagram is an example of the Family's input and output circuitry. The patented Signetics "Light-Load" NPN input structure (Q1/3/4/5, R1/2/3/4/5/6 & D4) and turn–OFF speed–up circuit (Q2 & D2/3) are used throughout the 74F Extended Octal-Plus© Family. The "Light-Load" NPN input is actually a high speed, differential amplifier with the reference side, the anode of D4, clamped at two diode voltage drops above ground (BE junctions of Q8/9/10 and Q11 of ~1.4V at 25°C). When the V_{IH} rises above this clamp voltage, the BE junction of Q1 is forward based allowing beta amplified, CE current to flow into the <1.0mA constant current source, Q3 (driven by Q4/5 & R2/3/4/5/6) . The beta of Q1 is guaranteed, by design, to be >50, thereby, guaranteeing that the input base bias current will be $<20\mu A$. The emitter of Q1 rises to $1V_{BE}$ (~300mV) below the V_{IH}, reverse biasing D4 and permitting Q8/9/10 base bias current to flow through R1.

The patented turn-OFF circuit consisting of Q2 and D2/3 produces a dynamic speed to help turn Q8/9/10 OFF quickly. During the time that the Q1 is turned-ON (input = $V_{IH} > 2.0V$), the reverse-biased Schottky diode, D2, acting as a capacitor, will be charged to the voltage at the emitter of Q1A or $1V_{BE}$ voltage drop below the input ($>2.0 - 1V_{BE}$). When the input in switched to $<V_{IL}$ (or $<0.8V$), the D2 stored charge discharges through the BE of Q2. Q2 CE current through D3 rapidly turns Q8/9/10 OFF.

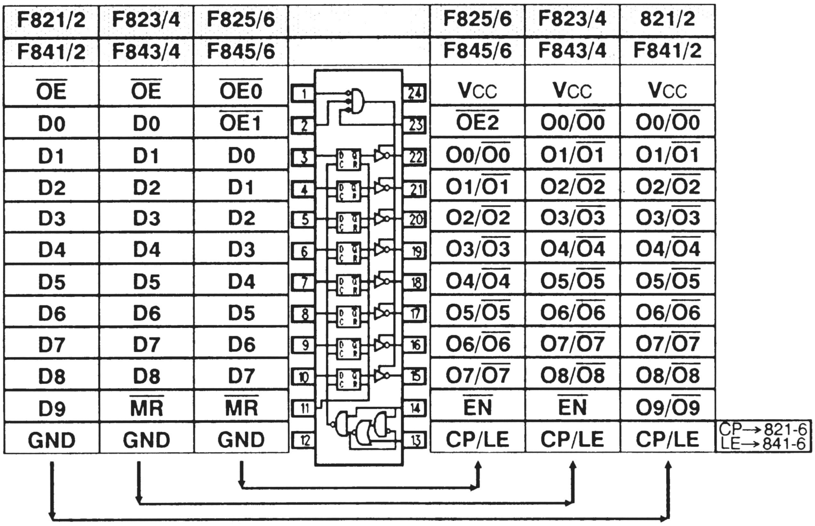
These circuit innovations produce high performance, very low input bias current ($\pm 20\mu A$) gate inputs. This input leakage represents a 30X reduction over the standard 74F Family's 600uA input current with virtually no loss in speed. The 74F Extended Octal-Plus© Transceivers have an input loading current of $\pm 70\mu A$ which is the combination of the "Light-Load" NPN input structure's $\pm 20\mu A$ and the 3–State Hi-Z output's $\pm 50\mu A$ leakage current.

The low "Light-Load" input current and high speed performance make this Family ideal for interfacing to low drive capability, slower MOS CPU, peripherals and semi–custom chips used in most of today's state–of–the–art logic designs. Besides very low input current requirements, this "Light-Load" input has another significant advantage over "traditional" input structures: Very lower input capacitance (smaller stored charge) due to very small devices geometries. Therefore, when Extended Octal-Plus devices are connected to a bus, they present less AC bus loading and do not significantly lower the characteristic impedance of the bus to the extend "traditional" input structures do. Thus, the amount of the AC current a bus driver has to produce to change the state of the bus is lowered and in many cases can make a difference between incident wave switching of the bus vs. losing time waiting for a reflected wave.

The Signetics 74F "Light-Load" Input Structure is discussed in more detail in Application Note AN215.

Output Drive Capabilities

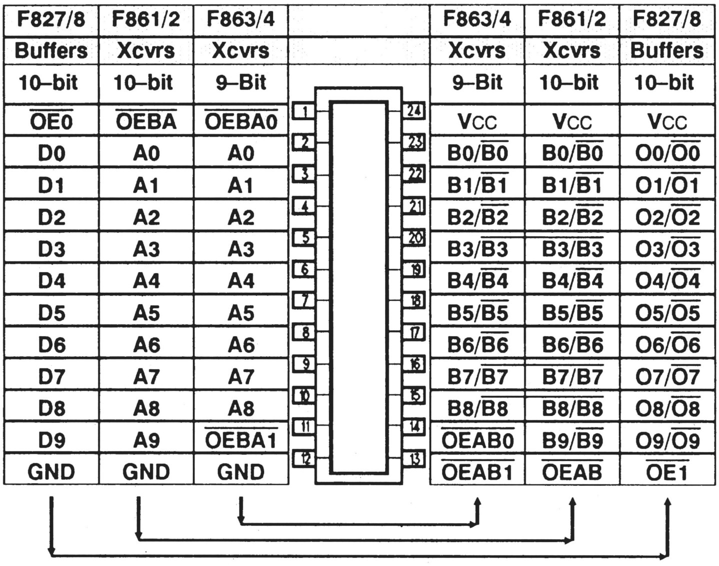
Virtually all devices in the Extended Octal-Plus© Family are guaranteed to source/sink more than –15mA/64mA @ V_{OH}/V_{OL} = 2.0/0.55V. One exception is the 74F841–thru–846 Series of Bus Interface Latches which are specified at –15/48mA. Several of the Family's transceiver products have lower A_N output drive



F821/2 F841/2	F823/4 F843/4	F825/6 F845/6			F825/6 F845/6	F823/4 F843/4	821/2 F841/2
$\overline{OE}$	$\overline{OE}$	$\overline{OE0}$	1	24	Vcc	Vcc	Vcc
D0	D0	$\overline{OE1}$	2	23	$\overline{OE2}$	O0/$\overline{O0}$	O0/$\overline{O0}$
D1	D1	D0	3	22	O0/$\overline{O0}$	O1/$\overline{O1}$	O1/$\overline{O1}$
D2	D2	D1	4	21	O1/$\overline{O1}$	O2/$\overline{O2}$	O2/$\overline{O2}$
D3	D3	D2	5	20	O2/$\overline{O2}$	O3/$\overline{O3}$	O3/$\overline{O3}$
D4	D4	D3	6	19	O3/$\overline{O3}$	O4/$\overline{O4}$	O4/$\overline{O4}$
D5	D5	D4	7	18	O4/$\overline{O4}$	O5/$\overline{O5}$	O5/$\overline{O5}$
D6	D6	D5	8	17	O5/$\overline{O5}$	O6/$\overline{O6}$	O6/$\overline{O6}$
D7	D7	D6	9	16	O6/$\overline{O6}$	O7/$\overline{O7}$	O7/$\overline{O7}$
D8	D8	D7	10	15	O7/$\overline{O7}$	O8/$\overline{O8}$	O8/$\overline{O8}$
D9	$\overline{MR}$	$\overline{MR}$	11	14	EN	EN	O9/$\overline{O9}$
GND	GND	GND	12	13	CP/LE	CP/LE	CP/LE

CP→821-6
LE→841-6

Figure 215-4a. 74F82X & 74F8X Registered/Latched Buffer Pin Configurations



F827/8 Buffers 10-bit	F861/2 Xcvrs 10-bit	F863/4 Xcvrs 9-Bit	Pin	Pin	F863/4 Xcvrs 9-Bit	F861/2 Xcvrs 10-bit	F827/8 Buffers 10-bit
$\overline{OE0}$	$\overline{OEBA}$	$\overline{OEBA0}$	1	24	VCC	VCC	VCC
D0	A0	A0	2	23	B0/$\overline{B0}$	B0/$\overline{B0}$	O0/$\overline{O0}$
D1	A1	A1	3	22	B1/$\overline{B1}$	B1/$\overline{B1}$	O1/$\overline{O1}$
D2	A2	A2	4	21	B2/$\overline{B2}$	B2/$\overline{B2}$	O2/$\overline{O2}$
D3	A3	A3	5	20	B3/$\overline{B3}$	B3/$\overline{B3}$	O3/$\overline{O3}$
D4	A4	A4	6	19	B4/$\overline{B4}$	B4/$\overline{B4}$	O4/$\overline{O4}$
D5	A5	A5	7	18	B5/$\overline{B5}$	B5/$\overline{B5}$	O5/$\overline{O5}$
D6	A6	A6	8	17	B6/$\overline{B6}$	B6/$\overline{B6}$	O6/$\overline{O6}$
D7	A7	A7	9	16	B7/$\overline{B7}$	B7/$\overline{B7}$	O7/$\overline{O7}$
D8	A8	A8	10	15	B8/$\overline{B8}$	B8/$\overline{B8}$	O8/$\overline{O8}$
D9	A9	$\overline{OEBA1}$	11	14	$\overline{OEAB0}$	B9/$\overline{B9}$	O9/$\overline{O9}$
GND	GND	GND	12	13	$\overline{OEAB1}$	$\overline{OEAB}$	$\overline{OE1}$

Figure 214-4b. 74F827/8 & 74F861–4 Buffers & Transceivers Pin Configurations

capabilities to reduce package power dissipation. Refer to Tables 214–1 and 3.

For example, the 74F657 Parity Bus Transceiver has two output ports with different capacities: The A_N port is guaranteed to source/sink -3mA/24mA (I_{OH}/I_{OL} = 2.4/0.50V), and the B_N port has an output drive capability of –15mA/64mA at 2.0V/0.55V. The 74F657's A_N port is designed to interface the chip side of the PC board to the backplane bus, while the B_N Port is capable of driving a transmission line or bus backplane line.

Referring to Figure 214–3, all of the Family's 3-State, totem-pole output structures have a Schottky blocking diode, D13, in their pull-up output structures. These diodes block leakage current from flowing into the outputs when V_{CC} is either open or shorted to ground.

This gives a very important advantage of being able to power down a PCB (or several PCBs) without disabling the bus and even without producing any glitching on the bus due to an undesired

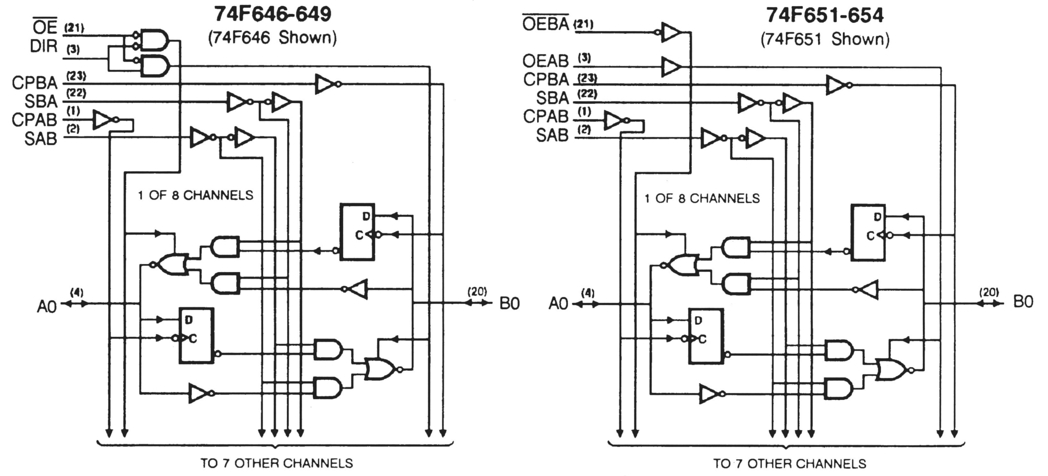
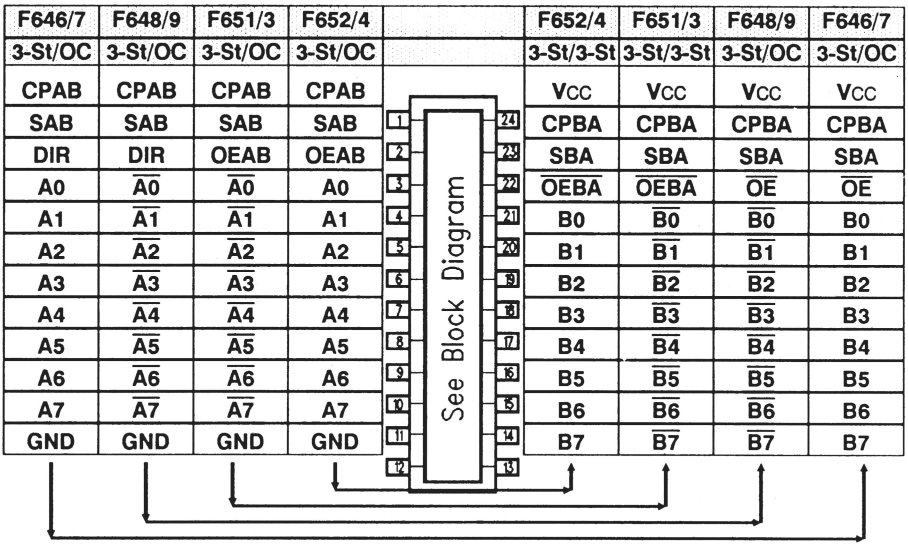

74F646-649
(74F646 Shown)
$\overline{OE}$ (21)
DIR (3)
CPBA (23)
SBA (22)
CPAB (1)
SAB (2)
1 OF 8 CHANNELS
D
C
D
C
A0 (4)
(20) B0
TO 7 OTHER CHANNELS
74F651-654
(74F651 Shown)
$\overline{OEBA}$ (21)
OEAB (3)
CPBA (23)
SBA (22)
CPAB (1)
SAB (2)
1 OF 8 CHANNELS
D
C
D
C
A0 (4)
(20) B0
TO 7 OTHER CHANNELS

Figure 214-5a. 74F646–649 & 74F651–654 Registered Transceivers Simplified Logic Block Diagram



F646/7	F648/9	F651/3	F652/4	F652/4	F651/3	F648/9	F646/7
3-St/OC	3-St/OC	3-St/OC	3-St/OC	3-St/3-St	3-St/3-St	3-St/OC	3-St/OC
CPAB	CPAB	CPAB	CPAB	V_{CC}	V_{CC}	V_{CC}	V_{CC}
SAB	SAB	SAB	SAB	CPBA	CPBA	CPBA	CPBA
DIR	DIR	OEAB	OEAB	SBA	SBA	SBA	SBA
A0	$\overline{\text{A0}}$	$\overline{\text{A0}}$	A0	$\overline{\text{OEBA}}$	$\overline{\text{OEBA}}$	$\overline{\text{OE}}$	$\overline{\text{OE}}$
A1	$\overline{\text{A1}}$	$\overline{\text{A1}}$	A1	B0	$\overline{\text{B0}}$	$\overline{\text{B0}}$	B0
A2	$\overline{\text{A2}}$	$\overline{\text{A2}}$	A2	B1	$\overline{\text{B1}}$	$\overline{\text{B1}}$	B1
A3	$\overline{\text{A3}}$	$\overline{\text{A3}}$	A3	B2	$\overline{\text{B2}}$	$\overline{\text{B2}}$	B2
A4	$\overline{\text{A4}}$	$\overline{\text{A4}}$	A4	B3	$\overline{\text{B3}}$	$\overline{\text{B3}}$	B3
A5	$\overline{\text{A5}}$	$\overline{\text{A5}}$	A5	B4	$\overline{\text{B4}}$	$\overline{\text{B4}}$	B4
A6	$\overline{\text{A6}}$	$\overline{\text{A6}}$	A6	B5	$\overline{\text{B5}}$	$\overline{\text{B5}}$	B5
A7	$\overline{\text{A7}}$	$\overline{\text{A7}}$	A7	B6	$\overline{\text{B6}}$	$\overline{\text{B6}}$	B6
GND	GND	GND	GND	B7	$\overline{\text{B7}}$	$\overline{\text{B7}}$	B7

Figure 214-5b. 74F646–649 & 74F651–653 Dual Registered Transceivers Pin Configurations

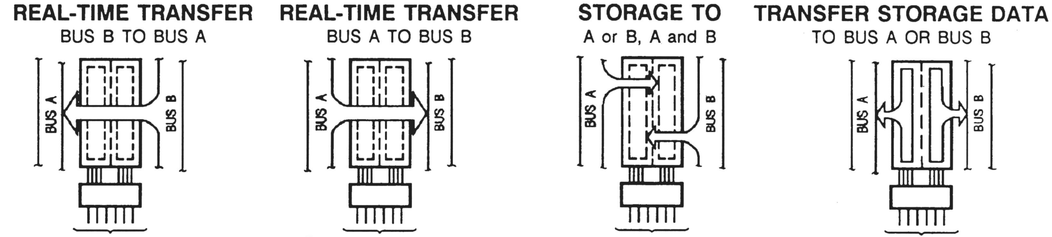
change in the output state of the device being powered down.

The output short–circuit (I_{OS}) limiting resistor (R14), the anode-to-cathode resistance/voltage drop of D13 and the collector-to-emitter/base-to-emitter resistance/voltage drop of Q13 limit the amount of current that can be sourced from a HIGH level output at a specified V_{OH}. For most of the parts in the Family, R14 is equal to 12Ω. The A_N port of several of the transceivers utilize an R14 of 30Ω producing I_{OH} (@ V_{OH} = 2.0V) of –6mA versus –15mA from the B_N ports 12Ω R14.

The output HIGH level sourcing current, I_{OH}, at a specified output voltage, V_{OH}, can be calculated by subtracting the voltage drops of D13, the pull-up darlington transistor, Q12/13, and the desired V_{OH} level from V_{CC} and dividing by the value of R14 plus the anode-to-cathode resistance of D13 and the collector-to-emitter/base-to-emitter resistance.

Assumptions:
$V_{D13} \cong 0.5V$ @ $R_{ON} = 3\Omega$ @ 25°C),
$V_{Q12/13} \cong 1.2V$ @ $R_{ON} = 8\Omega$ @ 25°C)
$I_{OH} = -[V_{CC}-(V_{D13}+V_{Q12/Q13}+V_{OH})]/(R14+R_{D13}+R_{Q13})$.
$I_{OH}(R14 = 12\Omega) = -[4.5V-(0.5V+1.2V+2.0V)]/23\Omega = -35mA$
$I_{OH}(R14 = 30\Omega) = -[4.5V-(0.5V+1.2V+2.0V)]/41\Omega = -20mA$
$I_{OS} = I_{OH}$ @ $V_{OH} = 0.0V$ and $V_{CC} = 5.5V$
$I_{OS}(R14 = 12\Omega) = -[5.5V-(0.5V+1.2V)]/23\Omega = -165mA$
$I_{OS}(R14 = 30\Omega) = -[5.5V-(0.5V+1.2V)]/41\Omega = -93mA$

Obviously, we have been very conservative in the I_{OH} specification to guardband against all conditions of temperature and input/output/supply voltage levels. The R_{ON} resistances of the output pullup transistors and blocking diode are large enough to prevent I_{OS} from exceeding –225mA for R14 = 12Ω and –150mA for R14 = 30Ω. (Refer to Table 214-1)



OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	X

Figure 214-6. 74F651–654 Registered Transceivers Storage Options (74F646–649 not shown)

Table 214-2. Parity Bus Family vs. The Competition

PART NUMBER	DESCRIPTION	TOTAL # of PINS	t_{PDmax}* IN to OUT	t_{PDmax}* IN to PARITY	I_{CCmax}**	POWER PINS	BROADSIDE DESIGN
74F455/F456 vs.	Octal Parity Buffer	24	7.5ns	16.0ns	110mA	Center	Yes
74F240/F244 + 74F280		38	7.5ns	14.5ns	125mA	Corner	No
74F655A/F656A vs.	Octal Parity Buffer	24	7.5ns	16.0ns	110mA	Corner	Yes
74F240/F244 + 74F280		38	7.5ns	14.5ns	125mA	Corner	No
74F657 vs.	Octal Parity Transceiver	24	7.5ns	16.0ns	110mA	Center	Yes
74F240/F245 + 74F280 + 1 AND Gate		38	8.0ns	14.5ns	125mA	Corner	No

NOTES:

* = Propagation Delays of DATA IN-to-DATA OUT and IN-to-PARITY OUT, T_A = 0° to 70°C, V_{CC} = +5.0V±10%, Output Load = C_L = 50pF & R_L = 500Ω

** = Worst Case Power, T_A = 0° to 70°C, V_{CC} = +5.0V±10%, Output Load = C_L = 50pF & R_L = 500Ω

74F821 – 74F863 Series

The 74F821 through 74F863 Series of Octal, 9-bit and 10-bit Buffers, Latch Buffers, Register Buffers and Transceivers are standardized around the AMD 298XX series with one significant difference – the Signetics' "Light-Load" NPN input offers a 50:1 reduction in input loading (1000uA vs. 20μA). This Series illustrates the standardized on 24-pin/300mil Slim-DIP packages, "Broadside" input/output pinouts and control function pins. All 74F8XX 3-state outputs are guaranteed to source/sink −15mA/64mA, except for the 74F84X Latched Buffers which are specified at −15/48mA.

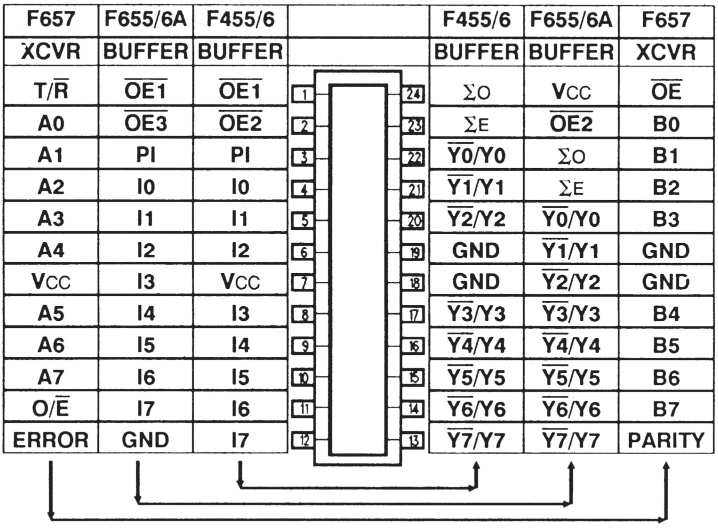
The logic diagram and pin configurations of the 74F828 Non-Inverting 10-Bit Buffer (Figure 214-1) and the 74F821-826 and 74F841-6 Registered/Latched Buffers (Figure 214-4a) are excellent illustrations of the standardized pin configuration illustrating "Broadside" chip design.

Figure 214-4b shows the pin-outs of the 74F827/8 Buffers and 74F861-4 Transceivers. There currently are no 9-bit buffer offerings in this Series.

Registered Transceivers Series

The 74F646-9 and 74F651-4 Octal Dual-Registered Transceivers offer a "Light-Load" combination of a 74F245 type transceiver with two 74F373/374 type octal registers within a 24-pin, Slim-DIP, Broadside input/output package. This Series offers a significant 6:1 package count reduction advantage over older technologies.

Figure 214-5a shows the 74F646 and 74F651 Transceivers Simplified Block Diagrams, and this Series' Pin Configurations are depicted in Figure 214-5b. Figure 214-6 graphically illustrates four optional storage and transfer modes of the 74F651 Octal, Non-Inverting, 3-State, Dual-Registered Transceiver. The 74F651 will be used to explain the operation of the entire Series. The 74F646/8 (3-State, INV/NINV) and the 74F647/9 (O.C., INV/NINV) Octal Dual-Registered Transceivers offer optional signal direction control logic and output enable to the 74F651-4 series.



F657	F655/6A	F455/6			F455/6	F655/6A	F657
XCVR	BUFFER	BUFFER			BUFFER	BUFFER	XCVR
T/$\overline{\text{R}}$	$\overline{\text{OE1}}$	$\overline{\text{OE1}}$	1	24	ΣO	V_{CC}	$\overline{\text{OE}}$
A0	$\overline{\text{OE3}}$	$\overline{\text{OE2}}$	2	23	ΣE	$\overline{\text{OE2}}$	B0
A1	PI	PI	3	22	$\overline{\text{Y0}}$/Y0	ΣO	B1
A2	I0	I0	4	21	$\overline{\text{Y1}}$/Y1	ΣE	B2
A3	I1	I1	5	20	$\overline{\text{Y2}}$/Y2	$\overline{\text{Y0}}$/Y0	B3
A4	I2	I2	6	19	GND	$\overline{\text{Y1}}$/Y1	GND
V_{CC}	I3	V_{CC}	7	18	GND	$\overline{\text{Y2}}$/Y2	GND
A5	I4	I3	8	17	$\overline{\text{Y3}}$/Y3	$\overline{\text{Y3}}$/Y3	B4
A6	I5	I4	9	16	$\overline{\text{Y4}}$/Y4	$\overline{\text{Y4}}$/Y4	B5
A7	I6	I5	10	15	$\overline{\text{Y5}}$/Y5	$\overline{\text{Y5}}$/Y5	B6
O/$\overline{\text{E}}$	I7	I6	11	14	$\overline{\text{Y6}}$/Y6	$\overline{\text{Y6}}$/Y6	B7
ERROR	GND	I7	12	13	$\overline{\text{Y7}}$/Y7	$\overline{\text{Y7}}$/Y7	PARITY

Figure 214-7. 74F Octal Parity Drivers/Transceiver Pin Configurations

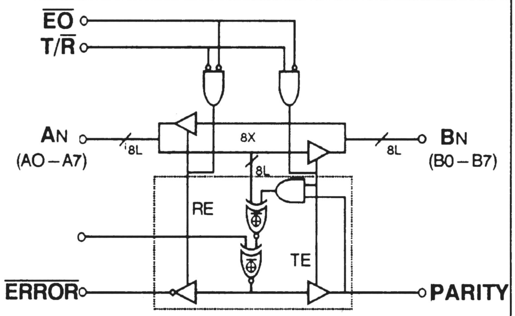


Figure 214–8a. 74F657 Simplified Block Diagram

This Series allows you to store or real-time transfer data in either direction through the transceiver function. Data at the AN port can be stored in either the AN port register or the BN port register and, then, can be transferred either from the AN port register to the BN port outputs or from the BN port register to the AN port outputs.

The same capabilities are available to data presented to the B–port. When a port's output buffers are enabled ($\overline{\text{OE}}$ = LOW and DIR = LOW for AN outputs enabled or HIGH for BN outputs enabled), the SXX select inputs (SAB and SBA) control the two EX–OR gates allowing the output port data to come either directly from the other port (real-time transfer) or from the other port's input storage register.

The CPAB and CPBA inputs are the LOW-to-HIGH edge-triggered clock inputs for the AN port register and BN port register. Data presented to either port's inputs can be clocked into its input register on a LOW-to-HIGH CPXX input regardless of the logic levels on any of the other mode control inputs.

The 74F651–4's OEAB and $\overline{\text{OEBA}}$ output enable inputs may be tied together to enable the BN outputs when HIGH or AN outputs when held LOW or can be used separately to independently control the two output ports. Tying the 74F651–4's OEAB and $\overline{\text{OEBA}}$ together is logically equivalent to the DIR input of the 74F646–9.

Parity Bus Series Advantages

The increased functional density of the Parity Bus Series produces a 2:1 package reduction (plus 1 AND gate) and, therefore, 38:24 pin reduction. Power dissipation savings of 82.5mW for the 74F455/456/655A/656A Drivers and 137.5mW for the 74F657 are also achieved through shared internal logic. Table 214–2 shows the package/pin advantage as well as the worst case propagation delays and ICC of the Family versus their competition.

Figure 214–7 is a summary of the pin configurations of entire Parity Bus Drivers and Transceiver Series.

The 74F455/456/655A/655A Octal Parity Bus Drivers and the 74F657 Octal Parity Bus Transceiver Series combines the popular Signetics 75F24X buffer/transceiver functions with the 74F280 9–bit Parity Generator/Checker, "Broadside" input/output pin configurations, "Light-Load" inputs and an increased guaranteed sink/source capabilities of −15mA/64mA for low impedance bus environments. The 74F445/446 Drivers with their multiple center-package ground supply pins are logically identical to the 74F655A/656A Drivers except for the latters' single corner-package supply pins and an additional $\overline{\text{Output Enable}}$ input. The 74F657 Parity Bus Transceiver allows the parity to be generated and checked in both directions in a single package replacing one 74F245 Transceiver, 20–pin DIP and two 74F280, 16–pin DIPs plus a couple of gates.

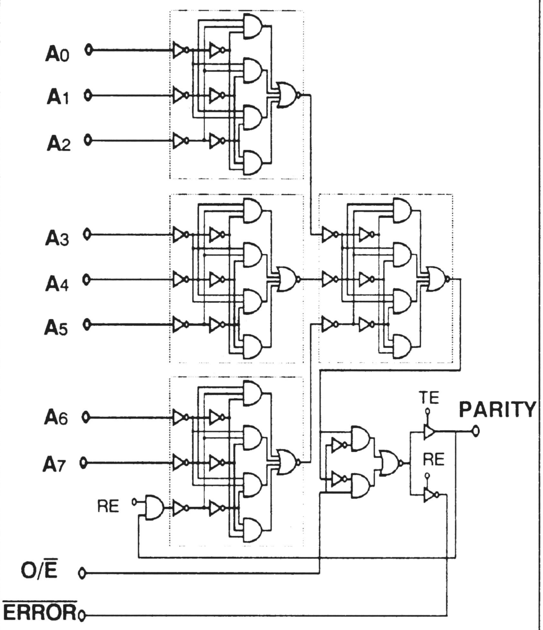


Figure 214–8b. 74F657 Parity Tree Logic Diagram

74F657 Operation

The 74F657 Parity Bus Transceiver, as shown in its simplified logic diagram Figure 214–8a, is a combination of a 74F245 Octal Transceiver and a 74F280A 9–Bit Parity Generator/Checker plus one AND gate. Figures 214–8b expands the logic block diagram of the Family's Parity Tree Logic (inside the dashed line of Figure 214-8a).

During TRANSMIT mode (AN = Hi–Z), the PARITY and $\overline{\text{ERROR}}$ outputs are generated from the AN input/output port. In the RECEIVE mode, the BN port is the input from the system or mother board bus (B–port outputs = Hi–Z).

For best speed performance, PARITY should always be generated from the AN port for the BN port (TRANSMIT mode), and parity $\overline{\text{ERROR}}$ should always be checked for data coming in on the B–port (RECEIVE mode). EVEN or ODD parity generation and checking is determined by the EVEN/$\overline{\text{ODD}}$ input (EVEN = HIGH & ODD = LOW).

In the TRANSMIT mode (T/$\overline{\text{R}}$ = HIGH), transmitted data travels from the A–port to the B–port in less than 8.0ns generating a PARITY bit output in less than 16.0ns. Whereas, in the RECEIVE mode (T/$\overline{\text{R}}$ = LOW), received data traverses from the B–port to the A–port path in, again, less than 8.0ns, but then, the $\overline{\text{ERROR}}$ checking output, being generated from the output data presented to the A–port and the PARITY input, takes an additional 16.5ns or less to stabilize. Therefore, the total RECEIVEd–data–to–$\overline{\text{ERROR}}$ checking output propagation time is the sum of the BN–to–AN delay (8ns) and the AN/PARITY–to–$\overline{\text{ERROR}}$ output delay (16.5ns) or 22.5ns.

However, in many cases, the propagation delay that has to be taken into consideration does not have to include parity calculation time and could be equal to that of just the transceiver part (8ns). This is due to the fact that it may not be too late to interrupt whatever needs to be interrupted in case of a parity error after the data has already gone by (i.e. via late bus error).

Parity Tree Analysis

The basic 3–Input Comparator Cell, inside the dashed line in Figure 214–8b, is used throughout the Parity Bus Series. If there are an even number of HIGH inputs (0 or 2) the output of the 3–input Comparitor Cell will be HIGH, while an odd number (1 or 3) will produce an output LOW. The 74F657's Parity Tree Logic, combines four of the 3–Input Comparators with a 2–input comparator, a 2–input AND gate and output buffers for PARITY and $\overline{\text{ERROR}}$ to produce the complete parity generator/checker logic.

The 74F588 IEEE–488 Octal Transceiver

The 74F588 is a non–inverting IEEE–488 standard transceiver contains eight bidirectional 3–state buffers. The BN port outputs can source/sink –15mA/64mA (guaranteed) and have series termination resistors as specified in the IEEE–488 specification. The AN port, which interfaces to the PC board or system logic bus, is guaranteed to source/sink –3mA/24mA. The 74F588 pinout in identical to that of the 74F545 Octal Transceiver with the IEEE–488 termination resistors in series with the BN port.

Metastability in Latches and Registers

Interfacing a basically asynchronous real–world with synchronous logic systems can and does cause many circuit designer headaches. The problem: latches and registers which are normally considered to have only two stable states (High and Low) actually have a third – The METASTABLE State. This third operating point occurs when the cross–coupled latch is exactly balanced. This state is only stable when there is no noise on the chip which would tend to destablize the perfect energy balance between the bistable states of the latch. Refer to Figure 214–9.

Metastability can occur when input data violate the setup time or hold time specifications at the clocking or strobing edge of the synchronizing clock input. With no system noise the latch can't decide "yes or no" so it is possible for the latch to "go metastable" or "maybe." With noise on the chip, random energy will "nudge" the latch toward one of its "bistable" states – HIGH or LOW. This metastable state time can range from nanoseconds to milliseconds. With today's very high performance logic families, the metastable condition can last for perhaps 1000 times the latch's normal propagation delay time. A metastable latch has an unpredictable delay time during which the output is between logic levels. This metastable state can easily last more than 50ns with today's high performance logic families and WILL cause systems to "crash" if great care isn't taken with asynchronous, real–world interfacing.

The D–type latch shown in Figure 214–9 has DATA applied to NAND gate 1 and $\overline{\text{DATA}}$ applied to NAND gate 2. When the LE (Latch Enable) input is LOW, gates 1 & 2 outputs are HIGH and the G3/4 R–S latch is latched and stable. When LE is HIGH, the latch appears to be transparent to the DATA input – Q equals DATA. On the HIGH–to–LOW transition of LE, the DATA logic level that meets the latch's setup and hold time is stored in the latch.

If DATA changes during the setup time to hold time period, it is possible for both outputs of gates 1 & 2 to be in the input tresholds region of gates 3 & 4, respectively. Under these conditions, the latch (gates 3 & 4) could be perfectly balanced in the METASTABLE state. Eventually, chip and system noise will cause the latch to be force into a HIGH/LOW stable state.

The Extended Octal-Plus© Family, while not entirely immune, has been made metastable resistant by using design techniques which force the latch toward a stable state much more quickly than older bus interface families.

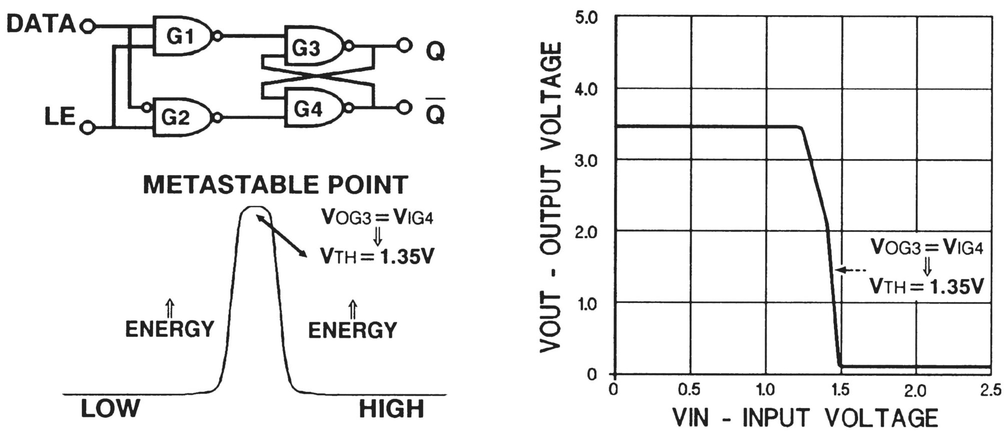


Figure 214-9. Metastability in Latches and Registers

Dual–Registered Transceiver Applications

Figure 214–10 illustrates how the 74F646–9 and 74F651–4 can be used to either synchronize data transfer between two systems or pipeline data. Data is stored in a register, then, while retreiving more data, the first data is read. When the second is available it can either be stored or read directly. Two slower systems can be multiplexed into a high speed system in the same way.

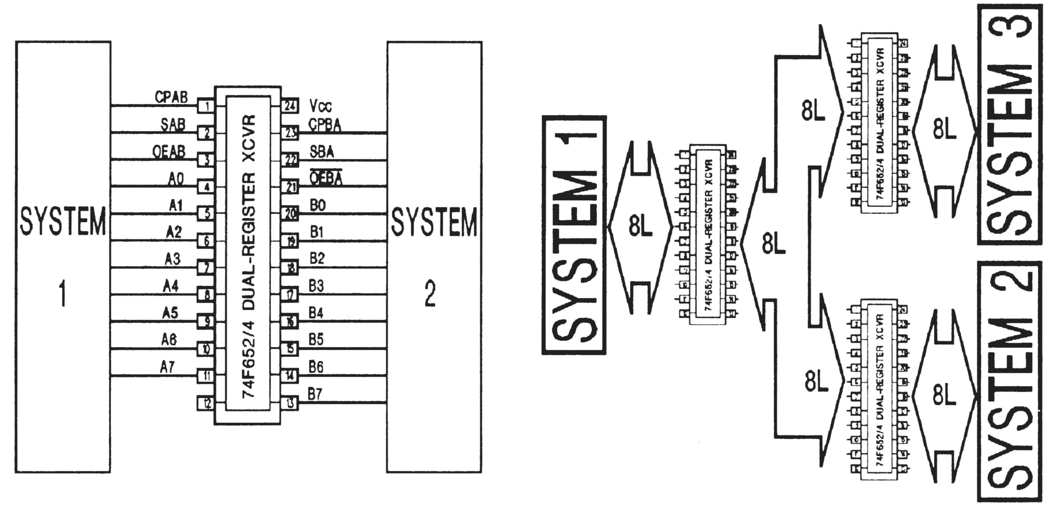

SYSTEM 1
CPAB
SAB
OEAB
A0
A1
A2
A3
A4
A5
A6
A7
74F652/4 DUAL-REGISTER XCVR
Vcc
CPBA
SBA
$\overline{\text{OEBA}}$
B0
B1
B2
B3
B4
B5
B6
B7
SYSTEM 2
SYSTEM 1
8L
8L
8L
8L
8L
8L
SYSTEM 3
SYSTEM 2

Figure 214-10. 74F Extended Octal–Plus© Dual–Registered Transceiver Applications

Parity Bus Transceiver Applications

Figure 214–11 illustrates the functional density advantages of the Parity Bus Series using the 74F657 in a typical microprocessor/data bus transceiver application. Note the 74F245 + 74F280A version would still require a 2–input AND gate and 3–state buffers for the PARITY and $\overline{\text{ERROR}}$ outputs. And, of course, it would require an order of magnitude higher input current than a single 74F657 would and would also introduce much higher capacitive loading (for both the bus and the microcontroller).

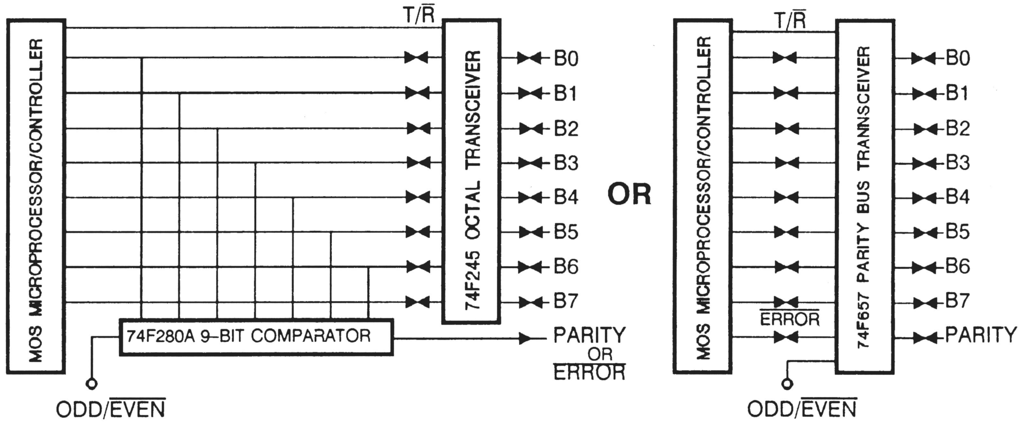

MOS MICROPROCESSOR/CONTROLLER
T/$\overline{\text{R}}$
74F245 OCTAL TRANSCEIVER
B0
B1
B2
B3
B4
B5
B6
B7
74F280A 9–BIT COMPARATOR
PARITY
OR
$\overline{\text{ERROR}}$
ODD/$\overline{\text{EVEN}}$
OR
MOS MICROPROCESSOR/CONTROLLER
T/$\overline{\text{R}}$
74F657 PARITY BUS TRANNSCEIVER
B0
B1
B2
B3
B4
B5
B6
B7
$\overline{\text{ERROR}}$
PARITY
ODD/$\overline{\text{EVEN}}$

Figure 214-11 74F657 Parity Bus Transceiver Applications

74F Extended Octal-Plus Family Applications

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Table 214-3 The Extended Octal–Plus© Family Capabilities Summary

Part Number	#-Bits	Polarity	Output	Brd-Side	I_{OH}/I_{OL} min	Storage	Speed	Parity	Comments
"Light-Load" Buffer and Line Driver Functions									
74F455/456	8-Bit	INV/NINV	3–St	Yes	–15/64mA	None	7.5ns	Yes	Multiple/Ctr Package GND Pins, Σ_E, Σ_O = –15/64mA
4F540/541	8-Bit	INV/NINV	3–St	Yes	–15/64mA	None	7.5ns	No	Broadside Pinout of F240
4F655A/656A	8-Bit	INV/NINV	3–St	Yes	–15/64mA	None	7.5ns	Yes	Σ_E, Σ_O = –15/64mA
74F827/828	10-Bit	NINV/INV	3–St	Yes	–15/64mA	None	9.0ns	No	
"Light-Load" Register and Latch Functions									
74F821/822	10-Bit	NINV/INV	3–St	Yes	–15/64mA	Reg	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enable}}$ & Clock EN Inputs
74F823/824	9-Bit	NINV/INV	3–St	Yes	–15/64mA	Reg	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enable}}$ & Clock EN Inputs
74F825/826	8-Bit	NINV/INV	3–St	Yes	–15/64mA	Reg	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enable}}$ & Clock EN Inputs
74F841/842	10-Bit	NINV/INV	3–St	Yes	–15/48mA	Latch	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enable}}$ & LE Enable Inputs
74F843/844	9-Bit	NINV/INV	3–St	Yes	–15/48mA	Latch	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enable}}$ & LE Enable Inputs
74F845/846	8-Bit	NINV/INV	3–St	Yes	–15/48mA	Latch	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enable}}$ & LE Enable Inputs
"Light-Load" Transceiver Functions									
74F545	8-Bit	NINV	A_N 3–St	Yes	–3/24mA	None	7.0ns	No	
			B_N 3–St	Yes	–15/64mA	None	7.0ns	No	
74F550/551	8-Bit	NINV/INV	B_N 3–St	Yes	–15/64mA	B_N–Reg	10.5ns	No	$A_N \rightarrow B_N$, ERROR , Status Registers, 50MHz
			A_N 3–St	Yes	–3/24mA	A_N–Reg	10.5–ns	No	$B_N \rightarrow A_N$, Multiple/Center Package GND Pins **
74F552	8-Bit	NINV	B_N 3–St	Yes	–15/64mA	B_N–Reg	10.5ns	Yes	$A_N \rightarrow B_N$, PARITY, $\overline{\text{ERROR}}$, Status Registers
			A_N 3–St	Yes	–3/24mA	A_N–Reg	10.5–ns	Yes	$B_N \rightarrow A_N$, Multiple/Center Package GND Pins **
74F588	8-Bit	NINV	A_N=3–St	Yes	–3/24mA	None	7.5ns	No	
			B_N 3–St	Yes	–15/64mA	None	7.5ns	No	IEEE-488/GPIB w/ Line Termination Resistors
74F620/623	8-Bit	INV/NINV	B_N 3–St	Yes	–15/64mA	None	7.5ns	No	$A_N \rightarrow B_N$
			A_N 3–St	Yes	–3/24mA	None	7.5ns	No	$B_N \rightarrow A_N$
74F621/622	8-Bit	NINV/INV	B_N OC	Yes	OC/64mA	None	13.0ns	No	$A_N \rightarrow B_N$
			A_N OC	Yes	OC/24mA	None	12.5ns	No	$B_N \rightarrow A_N$
74F640	8-Bit	INV	A/B 3–St	Yes	–15/64mA	None	7.5ns	No	$A_N \leftrightarrow B_N$
74F641/642	8-Bit	NINV/INV	B_N OC	Yes	OC/64mA	None	13.0ns	No	$A_N \rightarrow B_N$
			A_N OC	Yes	OC/20mA	None	12.0ns	No	$B_N \rightarrow A_N$
74F646/648	8-Bit	NINV/INV	A/B 3–St	Yes	–15/64mA	2 Reg	11.5ns	No	$A_N \leftrightarrow B_N$, Registers for A_N & B_N Ports, 80MHz (min.)
74F647/649	8-Bit	NINV/INV	A/B OC	Yes	OC/64mA	2 Reg	19.5ns	No	$A_N \leftrightarrow B_N$, Registers for A_N & B_N Ports, 40MHz (min.)
74F651/652	8-Bit	INV/NINV	A/B 3–St	Yes	–15/64mA	2 Reg	12.5ns	No	$A_N \leftrightarrow B_N$, Registers for A_N & B_N Ports, 80MHz (min.)
74F653/654	8-Bit	NINV/INV	B_N 3–St	Yes	–15/64mA	B_N–Reg	11.0ns	No	$A_N \rightarrow B_N$, B_N Port = 85MHz (min.)
			A_N OC	Yes	OC/64mA	A_N–Reg	20.0ns	No	$B_N \rightarrow A_N$, A_N Port = 45MHz (min.)
74F657	8-Bit	NINV	B_N 3–St	Yes	–15/64mA	None	8.0ns	Yes	$A_N \rightarrow B_N$, PARITY, $\overline{\text{ERROR}}$ = –15/64mA
			A_N 3–St	Yes	–3/24mA	None	8.0–ns	No	$B_N \rightarrow A_N$, Multiple/Center Package GND Pins
74F861/862	10-Bit	NINV/INV	A/B 3–St	Yes	–15/64mA	None	10.0ns	No	$A_N \leftrightarrow B_N$
74F863/864	9-Bit	NINV/INV	A/B 3–St	Yes	–15/64mA	None	10.0ns	No	$A_N \leftrightarrow B_N$
74F1245	8-Bit	NINV	B_N 3–St	Yes	–15/64mA	None	8.0ns	No	$A_N \rightarrow B_N$, "Light-Load" Pin-for-Pin F245 Replacement
			A_N 3–St	Yes	–3/24mA	None	8.0ns	No	$B_N \rightarrow A_N$
74F2951/2952	8-Bit	INV/NINV	A/B 3–St	Yes	–15/64mA	2 Reg	12.5ns	No	$A_N \leftrightarrow B_N$, Registers for A_N & B_N Ports, 80MHz (min.) **

NOTES: All parameters are worse–case, unless otherwise speified

3–St ⇒ 3–State

OC ⇒ Open Collector

Reg ⇒ LOW–to–HIGH Edge Clocked D–Type Register

Latch ⇒ HIGH Logic Level on the Latch Enable Logic, Data Passes Directly Through D–Type Latch,

⇒ HIGH–to–LOW Logic Level Transition of the Latch Enable, Data is Stored in the D–Type Latch

** ⇒ These device utilize standard FAST input structures producing input currents of +20μA & –0.6mA.

AN215

74FXXXX "Light Load" Input Products

Application Note

Major "Light-Load" Input Features

- Patented "Light-Load" NPN Input Structure
  - Normal Input Pins = ±20μA per input
  - Transceiver I/O Pins = ±70μA per I/O pin
  - Primarily Capacitive Loading = <10pF
- Ideal for MOS CPU, Peripherals & Semi-custom Bus Interfaces
- Patented Turn-OFF Speed-up Circuit
- No Significant Speed Disadvantage -- Standard 74F Speeds
- PC Board Transmission Line Drive Capability: –15/64mA I_{OH}/I_{OL}
- "Broadside" Design in 20–, 24– and 28–Pin Slim–DIP Packages
- "Light-Load" Family Includes:
  - 19 Buffers and Line Driver Parts
  - 19 Shift Register, Register & Latch Parts
  - 19 Transceivers (No Storage)
  - 8 Dual Registered Transceivers
  - 7 Arithmetic Functions

Introduction

The Signetics 74F "Light Load" product line is a high performance, TTL bus compatible series of very low input bias current (±20μA), buffer/driver, transceiver, register, multiplexer and arithmetic MSI functions. The patented "Light Load", ±20μA NPN input structure, shown in Figure 215–1, combined with a unique input speed-up circuit (also patented) makes this product line ideal for interfacing with all MOS devices, without any speed degradation. When compared to the I_{IL} of standard FAST inputs of 600μA (larger for some other logic families) this "Light Load" input shows a 30:1 reduction in I_{IL} loading (600μA/20μA).

These devices were specifically designed to meet the requirements of buffering low output drive MOS VLSI/LSI devices from the rigorous loading environment PC board/mother-board busses and system back planes. The "Light Load" Inputs and improved speed performance make this product line ideal for interfacing to low output drive capability, slower MOS CPU, peripherals and semi-custom chips used in most state-of-the-art logic designs today's. Using these "Light Load" Input bus products, MOS chip outputs will only have to drive the small amount of distributed PC trace capacitance and inductance loading. The MOS device output drive capability isn't wasted on drivers/transceivers with large DC input current drive requirements.

See Table 215-1 for a complete listing of the part numbers and functions of the "Light Load" product line.

"Flow-Through" Design

Figure 215–2 illustrates the pin configurations of the 74F84X Latched Buffer Series. Notice that all of the "Light Load" Input data bus products use a "Flow-Through" design which allows logic signals to flow into one side and out of the other without crossing or folding back on signal paths such as the 74F24X octal series. Comparing the physical PC board signal bus path layout required for the 74F845 Octal Registered Buffer to that of the zig-zag signal

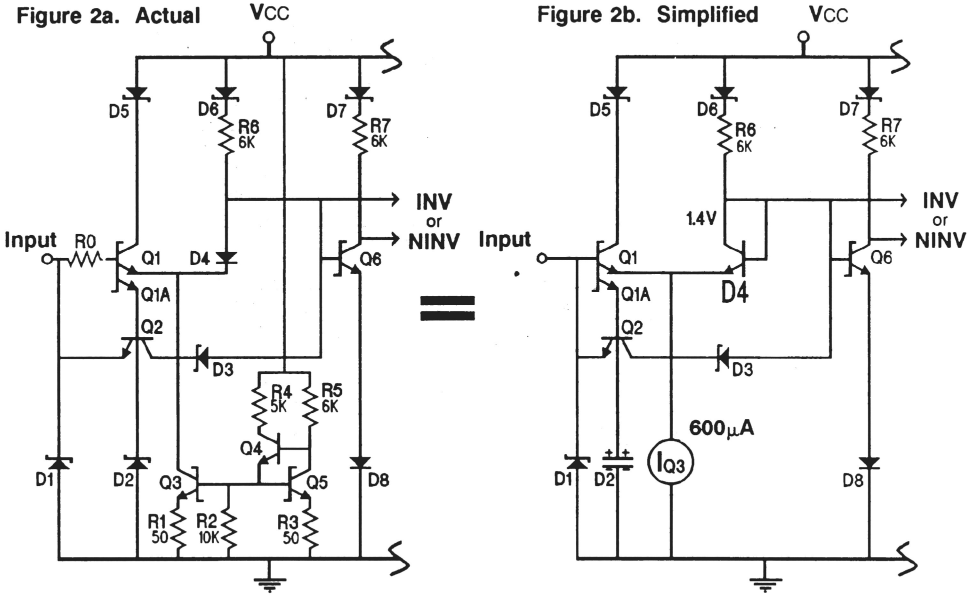
Figure 2a. Actual

Figure 2b. Simplified

Figure 215-1. The "Light-Load" and Speed-Up Circuit Input Structure (Actual & Simplified)

April 1988

The 74F "Light Load" Input Products

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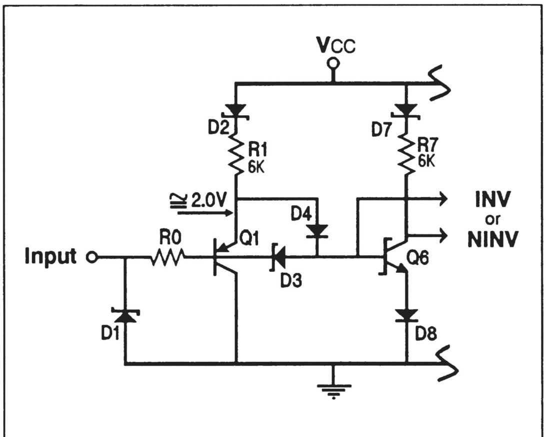


Figure 215-1c. Future "Light Load" PNP Input

path of the 74F240 Octal Inverting Buffer, you will see the significant advantages of the this product line's "Flow-Through" design in simplifying the design and layout of large, bus-oriented PC boards.

The "Light Load" Input product line combines "Flow-Through" design, high speed performance and high functional density into 20-, 24-and 28-pin, 300-mil Slim-DIP packages significantly reducing system propagation delays, parts count, power dissipation, PC board area/complexity and, therefore, total cost while enhancing total system reliability.

Input Structure - Differential Amplifier

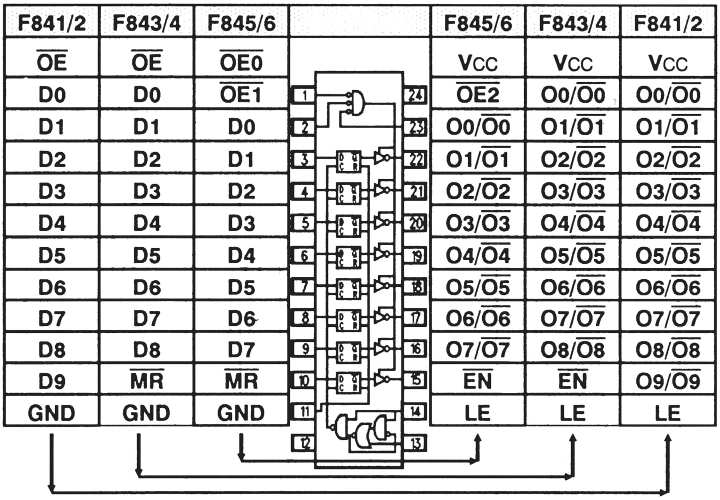
Figure 215-1 shows the circuit diagram of the patented "Light Load" NPN Input (Q1/3, R6 & D4) and the Turn-OFF Speed-Up Circuit (Q2, D2 & D3). This input structure is actually a linear differential amplifier consisting of Q1, D4 and a constant current sink made up of Q3/4/5 and R1/2/3. The input bias current of this amplifier is less than ±20μA for V_I between 0.0V and 5.5V. The Turn-OFF Speed-Up circuit (D2/Q2/D3) quickly discharges Q6's base-collector stored-charge to ground. The following analysis assumes room temperature and 5.0V_{CC} operation.

The Q1's base is the input side of the differential amplifier and D4's anode is the reference side. When the input is HIGH (2.0V), Q1 is turned-ON and I_{CE} plus I_{BE} current flows into Q3's constant current sink network of ~600μA. Since D4's anode is clamped at 1.3V to 1.4V by the V_{BE} of Q6 plus D8's voltage drop, and since Q1's emitter voltage is pulling the cathode of D4 up to greater than ~1.4V (the 2.0V_{IH} minus Q1's 0.6V_{BE}), R6's (6K) current can not flow through D4 and forward biases Q6's base-emitter.

Since Q6 is a Schottky clamped transistor, it has a V_{CEsat} ~0.5V. When Q6 is turned-ON by R6, the voltage at its collector drops to ~0.9V from ground (adding in D8 voltage drop) which turns-OFF the output totem-poll pull-down driver transistors and turns-ON the pull-up. This topic will be discussed in more detail in the next section (Refer to Figure 215-3).

Input Structure - Constant Current Sink

The constant current sink produced by Q3/4/5 and R1/2/3/4/5 sinks a relatively constant 600μA to ground. This "current mirror" circuit drives the base-to-ground voltage of Q3 and Q5 to Q5 V_{BE} plus the voltage drop across R3. Since Q3 and Q5 are identical, the voltage drops across R1 will equal that of R3. Therefore, the current



F841/2	F843/4	F845/6			F845/6	F843/4	F841/2
$\overline{OE}$	$\overline{OE}$	$\overline{OE0}$	1	24	VCC	VCC	VCC
D0	D0	$\overline{OE1}$	2	23	$\overline{OE2}$	O0/$\overline{O0}$	O0/$\overline{O0}$
D1	D1	D0	3	22	O0/$\overline{O0}$	O1/$\overline{O1}$	O1/$\overline{O1}$
D2	D2	D1	4	21	O1/$\overline{O1}$	O2/$\overline{O2}$	O2/$\overline{O2}$
D3	D3	D2	5	20	O2/$\overline{O2}$	O3/$\overline{O3}$	O3/$\overline{O3}$
D4	D4	D3	6	19	O3/$\overline{O3}$	O4/$\overline{O4}$	O4/$\overline{O4}$
D5	D5	D4	7	18	O4/$\overline{O4}$	O5/$\overline{O5}$	O5/$\overline{O5}$
D6	D6	D5	8	17	O5/$\overline{O5}$	O6/$\overline{O6}$	O6/$\overline{O6}$
D7	D7	D6	9	16	O6/$\overline{O6}$	O7/$\overline{O7}$	O7/$\overline{O7}$
D8	D8	D7	10	15	O7/$\overline{O7}$	O8/$\overline{O8}$	O8/$\overline{O8}$
D9	$\overline{MR}$	$\overline{MR}$	11	14	$\overline{EN}$	$\overline{EN}$	O9/$\overline{O9}$
GND	GND	GND	12	13	LE	LE	LE

Figure 215-2. 74F84X Latched Buffer Pin Configurations

through R1 equal the current through R3 times the ratio of R3:R1.

The base bias currents for Q3 and Q5 is supplied by Q4. Because of the relatively high βs of Q3 and Q5 (>50), their base currents of $\sim 10\mu A$ do not significantly effect the currents through R3 and R1 (β or BETA = transistor current gain). At 25°C and $V_{CC} = 5.0V$, R3's current is approximately equal to:

$I_{R3} = [V_{CC} - (V_{BE\text{-}Q4} + V_{BE\text{-}Q5})]/(R3 + R5)$

$I_{R3} = (5.0V - 1.2V)/(50\Omega + 6000\Omega) \cong 600\mu A$

Therefore:

$I_{CE\text{-}Q3} \cong I_{R1} = I_{R5} * (R3/R1) \cong 600\mu A$

With Q1's β also greater than 50, the HIGH logic level input bias current is less than $20\mu A$:

$I_{OH} = I_{CE\text{-}Q3}/BETA_{Q1} \cong 600\mu A/>50) < 12\mu A$

The "Light Load" PNP Input

We will soon be introducing a new product line of "Light Load" PNP devices. One of the first products will be the 74F821 through 74F826 Registered Buffers which will have the same pin configurations and options as the 74F841 through 74F846 Latched Buffers (See Figure 215–2). The 74F82X series will provide a positive–going edge triggered clock input to its 8-, 9- and 10-bit register storage parts versus the 74F84X series' HIGH level Latch Enabled latches.

With Signetics' latest oxide–isolated process, a new, high performance "Light Load" PNP input structure will soon be available. This new PNP input, shown in Figure 215–1c, provides a high impedance AND input structure versus the NPN input OR input and reduces the chip power dissipation by eliminating the requirement for a constant current source for each input.

The PNP input is still a differential amplifier with the cathode of D3 referenced to 2 V_{BE} voltage drops from ground. When the input is HIGH ($V_{IH} \geq 2V$), no Q1 emitter–base current can flow because the anode of D3 is clamped to the 2 V_{BE}. As D4 forward biased with the current from R1, the output driver transistor (Q6) turns ON. When the input is LOW ($V_{IL} \leq 0.8V$), Q1's emitter–base junction is forward biased which turns ON the β amplified emitter–collector current of Q1. When Q1 is ON, the anode of D4 is clamped OFF by the input V_{IL} voltage plus Q1's emitter–base drop ($V_{IL} + Q1_{VBE} \leq 0.8V + 0.6V = 1.4V$). Therefore, the input threshold at the base of Q1 is $\cong 1.4V$ (2 V_{BE}) at 25°C.

With the β of Q1 typically greater than 100, the V_{IL} input bias current is guaranteed to be less than $20\mu A$. With the input HIGH, the input leakage is also guaranteed to be less than $20\mu A$. The β amplification of Q1 is basically the only difference between this PNP input's $20\mu A$ I_{IL} and the standard diode input's I_{IL} of $600\mu A$.

When the base of Q1 is switched LOW, the Schottky diode D3 provides a turn–OFF speed–up path to ground which quickly discharges the base of the driver transistor (Q6).

Output Structures

A characteristic example of the output structures found throughout the 74FXXXX Light Load Product Line is the 74F657 Parity Bus Transceiver which has two basic output designs. Figure 215-3 illustrates the 74F657's output structure designs of these output structures: A_N Port's output (Figure 3b) is guaranteed to handle -3/+24mA (2.4/0.5V V_{OH}/V_{OL}), and the B_N Port (Figure 3a) can drive greater than -15/+64mA (2.0/0.55V V_{OH}/V_{OL}). The A_N port is

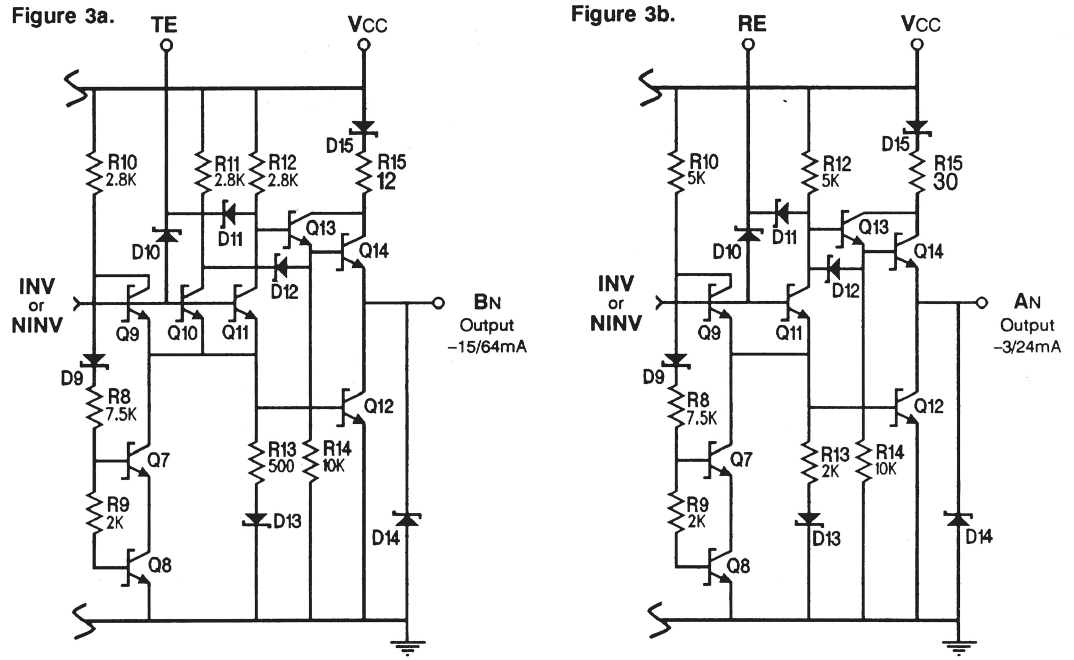


Figure 3. Two Typical "Light-Load Output" Structures (74F657)

The 74F "Light Load" Input Products

AN215

Table 215-1. 74FXXXX Light Load Input Products

Part Number	#-Bits	Polarity	Output	Broad–Side	I_{OH}/I_{OL} min	Storage	Speed	Parity	Comments
"Light-Load" Buffers and Line Drivers									
74F125/6	4-Bit	NINV	3-St	No	–15/64mA	None	6.5ns	No	Separate output enables (F125 = $\overline{EN}$ & F126 = EN)
74F365/6	6-Bit	NINV	3-St	No	–15/64mA	None	7.5ns	No	Common output enable
74F367/8	6-Bit	INV	3-St	No	–15/64mA	None	7.5ns	No	Two output enables controlling 3 outputs each
74F455/6	8-Bit	INV/NINV	3–St	Yes	–15/64mA	None	7.5ns	Yes	Multiple/Ctr Package GND Pins, Σ_E, Σ_O = –15/64mA
74F540/1	8-Bit	INV/NINV	3–St	Yes	–15/64mA	None	7.5ns	No	Broadside Pinout of F240
74F655A/6A	8-Bit	INV/NINV	3–St	Yes	–15/64mA	None	7.5ns	Yes	Σ_E, Σ_O = –15/64mA
74F804/1804	6-Bit	2I–NAND	3-St	No	–48/48mA	None	4.0ns	No	PNP Hex 2–InNAND Gate, F1804 has Ctr Supply Pins
74F805/1805	6-Bit	2I–NOR	3-St	No	–48/48mA	None	4.0ns	No	PNP Hex 2–Input NOR Gate, F1805 has Ctr Supply Pins
74F808/1808	6-Bit	2I–AND	3-St	No	–48/48mA	None	5.0ns	No	PNP Hex 2–Input AND Gate, F1808 has Ctr Supply Pins
74F827/8	10-Bit	NINV/INV	3–St	Yes	–15/64mA	None	9.0ns	No	
74F832/1832	6-Bit	2I–OR	3-St	No	–48/48mA	None	5.5ns	No	PNP Hex 2–Input OR Gate, F1832 has Ctr Supply Pins
74F1240/1	8-Bit	INV/NINV	3-St	No	–15/64mA	None	6.5ns	No	Light Load pin replacements for F240/1
74F1244	8-Bit	INV/NINV	3-St	No	–15/64mA	None	7.0ns	No	Light Load pin replacements for F244
74F30240/4	8-Bit	INV/NINV	OC	Yes	OC/160mA	None	15.0ns	No	Octal, 30Ω PC Board Data Transmission Line Driver
"Light-Load" Registers and Latches									
74F166	8-Bit	NINV	3–St	Yes	–1/20mA	S/R	110MHz	No	Serial/Parallel –In, Serial–Out
74F195	4-Bit	NINV	3–St	Yes	–1/20mA	S/R	110MHz	No	Serial/Parallel –In, Serial–Out
74F273	8-Bit	NINV	3–St	No	–1/20mA	S/R	120MHz	No	D-Type Flip–Flops
74F377	8-Bit	NINV	3–St	No	–1/20mA	S/R	100MHz	No	D-Type Flip–Flops
74F595	8-Bit	NINV	3–St	Yes	–3/20mA	S/R	80MHz	No	S or P–In, Serial-Out w/D-Register Output Storage
74F597	8-Bit	NINV	3–St	Yes	–3/20mA	S/R	80MHz	No	S or P–In, Serial–Out w/D-Register Input Storage
74F598	8-Bit	NINV	3–St	Yes	–3/20mA	S/R	80MHz	No	F597 w/Multiplexed Inputs and Outputs
74F821/2	10-Bit	NINV/INV	3–St	Yes	–15/64mA	Reg	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enables}}$ & Clock EN Inputs
74F823/4	9-Bit	NINV/INV	3–St	Yes	–15/64mA	Reg	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enables}}$ & Clock EN Inputs
74F825/6	8-Bit	NINV/INV	3–St	Yes	–15/64mA	Reg	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enables}}$ & Clock EN Inputs
74F841/2	10-Bit	NINV/INV	3–St	Yes	–15/48mA	Latch	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enables}}$ & LE Enable Inputs
74F843/4	9-Bit	NINV/INV	3–St	Yes	–15/48mA	Latch	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enables}}$ & LE Enable Inputs
74F845/6	8-Bit	NINV/INV	3–St	Yes	–15/48mA	Latch	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enables}}$ & LE Enable Inputs
"Light-Load" Transceivers/Latched or Registered Transceivers									
74F545	8-Bit	NINV	A_N=3–St	Yes	–3/24mA	None	7.0ns	No	Pin–for–Pin Replacement for the Intel 8286
			B_N=3–St	Yes	–15/64mA	None	7.0ns	No	
74F588	8-Bit	NINV	A_N=3–St	Yes	–3/24mA	None	7.5ns	No	
			B_N=3–St	Yes	–15/64mA	None	7.5ns	No	IEEE-488/GPIB w/ Output Line Termination Resistors
74F620/23	8-Bit	INV/NINV	B_N=3–St	Yes	–15/64mA	None	7.5ns	No	A_N ↔ B_N, A_N=–3/24mA
74F621/22	8-Bit	NINV/INV	B_N=OC	Yes	OC/64mA	None	13.0ns	No	A_N ↔ B_N, AN=OC/24mA
74F640	8-Bit	INV	A/B=3–St	Yes	–15/64mA	None	7.5ns	No	A_N ↔ B_N
74F641/42	8-Bit	NINV/INV	A/B=OC	Yes	OC/64mA	None	13.0ns	No	A_N ↔ B_N
74F646/48	8-Bit	NINV/INV	A/B=3–St	Yes	–15/64mA	2–Reg	11.5ns	No	A_N ↔ B_N, Registers for A_N & B_N Ports, 80MHz (min.)
74F647/49	8-Bit	NINV/INV	A/B=OC	Yes	OC/64mA	2–Reg	19.5ns	No	A_N ↔ B_N, Registers for A_N & B_N Ports, 40MHz (min.)
74F651/2	8-Bit	INV/NINV	A/B=3–St	Yes	–15/64mA	2–Reg	12.5ns	No	A_N ↔ B_N, Registers for A_N & B_N Ports, 80MHz (min.)
74F653/4	8-Bit	NINV/INV	B_N=3–St	Yes	–15/64mA	B_N–Reg	11.0ns	No	A_N → B_N, B_N Port = 85MHz (min.)
			A_N=OC	Yes	OC/64mA	A_N–Reg	20.0ns	No	B_N → A_N, A_N Port = 45MHz (min.)
74F657	8-Bit	NINV	B_N=3–St	Yes	–15/64mA	None	8.0ns	Yes	A_N ↔ B_N, PARITY I/O, ODD/$\overline{\text{EVEN}}$ In & $\overline{\text{ERROR}}$ Out
74F861/2	10-Bit	NINV/INV	A/B=3–St	Yes	–15/64mA	None	10.0ns	No	A_N ↔ B_N
74F863/4	9-Bit	NINV/INV	A/B=3–St	Yes	–15/64mA	None	10.0ns	No	A_N ↔ B_N
74F1242/3	8-Bit	INV	A/B=3–St	No	–15/64mA	None	7.5ns	No	A_N ↔ B_N, Light Load pin replacements for F240/1
74F1245	8-Bit	INV	A/B=3–St	Yes	–15/64mA	None	6.5ns	No	A_N ↔ B_N, Light Load pin replacements for F245
74F30245	8-Bit	NINV	B_N=OC	Yes	OC/160mA	None	15.0ns	No	Octal, 30Ω Transmission Line Drive, B_N =0.6mA I_{IL}
			A_N=3–St	Yes	–3/24mA	None	7.0ns	No	A_N "Light-Load" Inputs
74F30640	8-Bit	INV	B_N=OC	Yes	OC/160mA	None	15.0ns	No	Octal, 30Ω Transmission Line Drive, B_N =0.6mA I_{IL}
			A_N=3–St	Yes	–3/24mA	None	7.0ns	No	A_N "Light-Load" Inputs
"Light Load" Arithmetic Functions									
74F85	4-Bit	INV/NINV	3–St	No	–1/20mA	None	14.5ns	No	4-Bit Magnitude Comparator
74F280A/B	9-Bit	NINV	3–St	Yes	–1/20mA	None	14.5ns	Yes	Parity Generator/Checker, "B" is faster than "A" version
74F604/5	16-Bit	NINV	3-St/OC	Yes	–3/24mA	D-Reg	80MHz	No	Dual 8–Bit Registered Octal Multiplexer

NOTES: All parameters are worse–case, unless otherwise speified
3–St ⇒ 3–State
OC ⇒ Open Collector
Reg ⇒ LOW–to–HIGH Edge Clocked D–Type Register
Latch ⇒ HIGH Logic Level on the Latch Enable Logic, Data Passes Directly Through D–Type Latch,
⇒ HIGH–to–LOW Logic Level Transition of the Latch Enable, Data is Stored in the D–Type Latch
S/R. ⇒ Shift Register

designed to drive the chip side of the PC board to backplane interface, while the B_N Port is capable of driving PC board data transmission lines and back plane signal line with a characteristic impedance as low as 70Ω.

Referring back to Figure 215–1a, the base drive current for Q9/10/11 comes from either R6 for an inverting output or R7, if the output is non-inverting. For the inverting case, D4 is back-biased when the base voltage applied to Q1 ($\geq 2.0V_{OH}$) and Q9 base drive is supplied from R6. Q9's base is clamped at the sum of base-emitter forward biased voltage drops of Q9/10/11 and Q12. Q12's base drive primarily comes from R10/11/12 when Q9/10/11 are ON.

When Q9/10/11 begin to turn–ON, the base drive for Q12 must first overcome the R13/D13 base clamp before current can flow into Q12's base. During the output voltage HIGH to LOW transition, this delay minimizes totem-pole feed–through current into the ground lead by allowing the collector of Q11 (Phase Splitter Transistor – Q_{PS}) to pull down toward 1 V_{BE} + 1 V_{CEsat} and, thereby, turning–OFF the Q13/14 darlington totem–pole output pull–up driver before Q12 completely turns–ON.

When the gate input switches from V_{IH} to V_{IL} ($\leq 0.8V$), the charge stored in D2 discharges through the base–emitter of Q2. Q2 (through D3) quickly pulls the bases of Q9/10/11 toward ground. When the collector of Q9 rises high enough (~1.3V) to forward bias the Q12 base clamping network of D9/R8/R9/Q7/Q8, Q12 is quickly turned–OFF before the Q13/14 totem pole pull–up can turn–ON. This design minimizes feed-through ground during the output voltage LOW to HIGH transition.

The 3-state, totem-pole output structures of both the A_N and B_N ports have Schottky blocking diodes, D15, in their pull-ups. Their purpose is to block leakage current from flowing into the outputs when V_{CC} is either open or shorted to ground. These diodes will not let current flow until the output voltage reaches 5.5V.

The I_{OS} limiting resistors, R15, limit the amount of current that can be sourced from the HIGH to ground. Note that R15 is 12Ω for the B_N outputs and 30Ω for the A_N outputs. Therefore, under the same conditions, the B_N output pull-up structure will be able to source 2.5 time more current than the A_N outputs.

Minimizing Ground Bounce

Refer to Application Note AN213 – 74F30XXX Family Applications for a detailed discussion of "ground-bounce" and internal noise generation due to reduced ground lead inductance. When a TTL output switches from LOW to HIGH or HIGH to LOW some feed-through or crossover current will be injected into the ground lead of the IC while both the pull-up and pull-down output drive structures are ON simultaneously. The larger the number of switched outputs the larger the feed-through current and "ground bounce."

"Ground bounce" directly effects the input threshold of a gate and, therefore, its noise sensitivity. The newer output structure design used in the "Light Load" NPN Input Product Line allow all outputs to switch simultaneously with minimal "ground bounce."

AN216
Arbitration In Shared Resource Systems

Application Note

INTRODUCTION

The need for more powerful and faster systems gave birth to multiprocessing and multitasking systems. But to achieve this, cost and reliability were not to be sacrificed. To reduce cost it is vital to share resources, but to do so requires reliable means of arbitration. In a multiprocessing system, a single bus may be shared between various processors or intelligent peripherals. The resources shared by processors (Figure 1) are generally termed as global resources and those shared between the local processor and the peripherals (Figure 2) are typically known as local resources. Whether local or global, there always exists a protocol that will connect and disconnect various devices to and from the shared resources. Various bus architectures in existence today have different ways of doing this.

No matter what the protocol of a specific bus, there is always a method which dictates how arbitration shall be performed between two or more devices. Some systems employ synchronous arbitration and some use an asynchronous approach. The third option is not to use arbitration at all, but instead to employ time-multiplexing. This is used mainly in data communications by dividing the common media into various time slots. Each processor (station) is assigned a predetermined time for using the media. If the station does not need to use the media during its assigned time-slot, it may pass control to the next station. This obviously results in an inefficient use of the bus bandwidth.

Synchronous and asynchronous arbitration have their advantages and disadvantages, and are both used in system designs. Some applications may even use a combination of the two. Generally, synchronous arbitration is used in systems where the designer can take the time to synchronize signals with the master clock. In synchronous arbitration the request is sampled on a clock edge, and therefore if it is asserted close to, but after the sampling clock edge, it will not be recognized

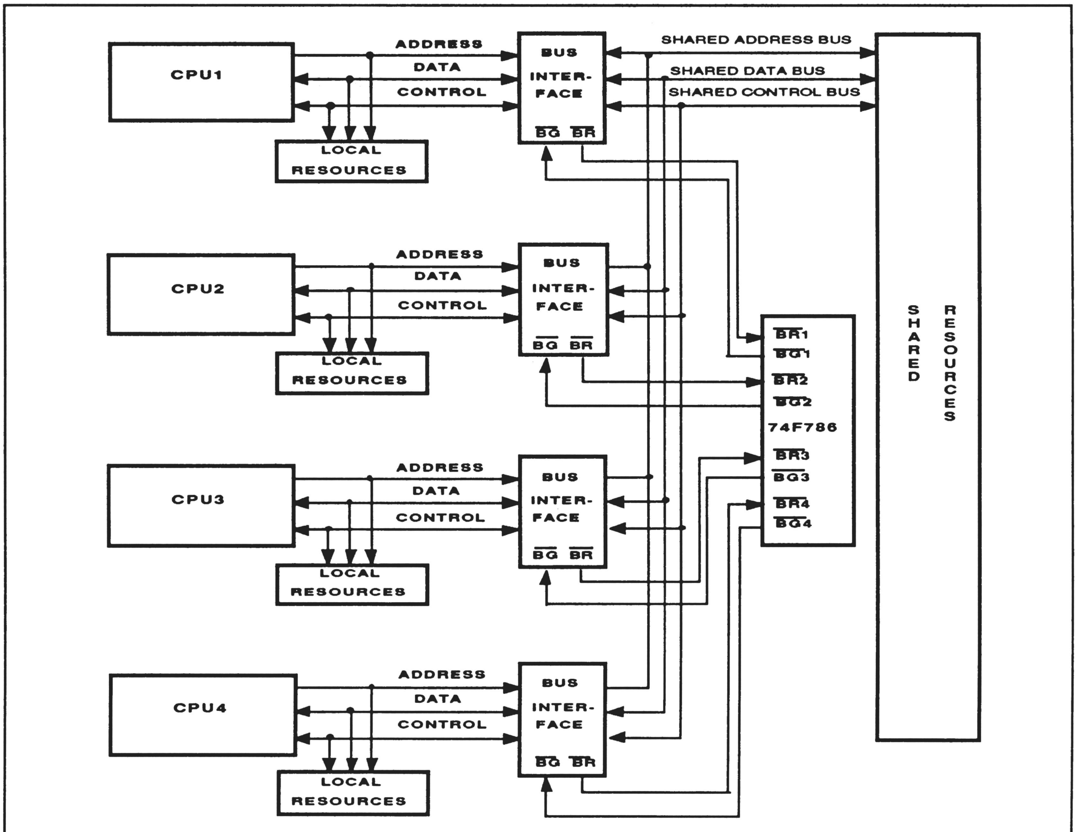

CPU1
ADDRESS
DATA
CONTROL
BUS INTER-FACE
BG BR
LOCAL RESOURCES
SHARED ADDRESS BUS
SHARED DATA BUS
SHARED CONTROL BUS
CPU2
ADDRESS
DATA
CONTROL
BUS INTER-FACE
BG BR
LOCAL RESOURCES
BR1
BG1
BR2
BG2
74F786
BR3
BG3
BR4
BG4
SHARED RESOURCES
CPU3
ADDRESS
DATA
CONTROL
BUS INTER-FACE
BG BR
LOCAL RESOURCES
CPU4
ADDRESS
DATA
CONTROL
BUS INTER-FACE
BG BR
LOCAL RESOURCES

Figure 1: Sharing global resources

until after a whole clock cycle. Todays applications, where speeds are being pushed to their limits may not find that an optimal solution. Therefore more and more designers tend towards asynchronous arbitration because it is much faster on the average. Since applications vary drastically from one to another, some may be better served by first-come-first-serve arbitration, some with fixed priority and some with dynamic priority.

In a first-come-first-served scheme as the name implies, the request to be asserted first is selected first. All other requests made after the first are queued in their respective order of assertion. After the current request is serviced, the request asserted second will be selected and so on. If the request just serviced is asserted again, before all other active requests are serviced, it will be placed at the end of the queue. In a fixed priority method all inputs have a hard-wired priority and cannot be changed. In a dynamic priority assignment the user can change the priority depending upon the system needs. For example, processors performing vital tasks may be placed at a higher priority as compared to processors doing background tasks.

Arbitration, whether synchronous or asynchronous, always brings up the question of "metastability". A hard fact that relates itself all the way back to the beginning of the history of electronics. In its simplest definition it is the state of a flip- flop that is neither a logic"1" or a logic"0", and is a result of violations of its set-up and hold times. This condition must be allowed and dealt with in arbitration and synchronization designs.

Metastability

Various publications have talked about this subject and given recommendations for reducing but not completely eliminating this potential problem. Briefly the suggestions consist of using very fast flip-flops (with very small set-up and hold times), using multiple flip-flops and delay lines and designing of metastable-hardened flip-flops. Please note that a metastable-hardened flip-flop does not necessarily mean that it will never enter a metastable state, but rather it is a flip-flop that is highly optimized to be used in applications where the system designer can not guarantee the minimum set-up and hold times specified by the manufacturer. Since, as of today, the design of a metastable free flip-flop is not practically possible, the next best thing that could be done is design of a flip-flop with significantly reduced set-up and hold times and reduced propagation delays. This will ensure reduced probability of being in a metastable state. Since we still will have some probability of not meeting the minimum set-up and hold times and potentially being in a metastable state, another requirement to be im-

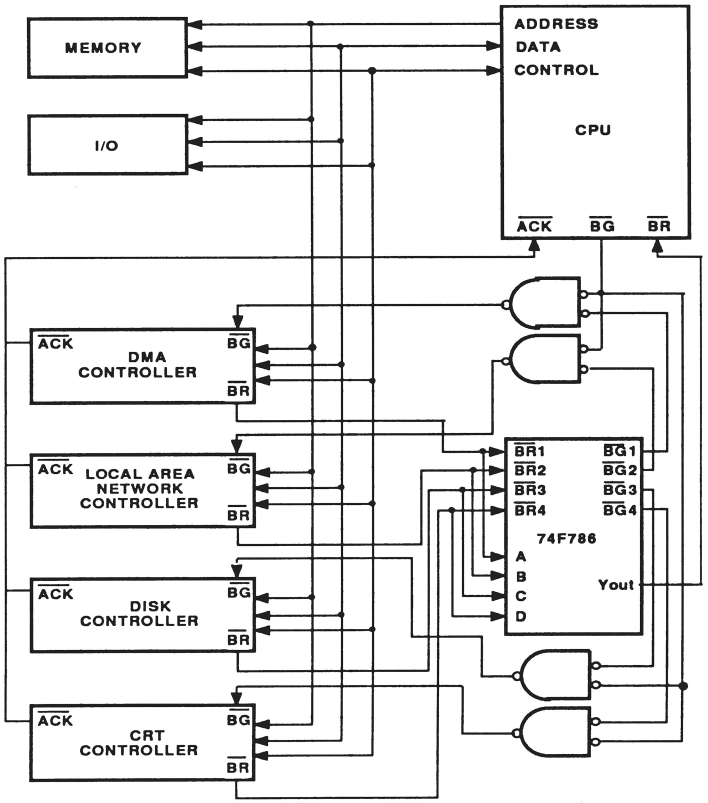


Figure 2: Sharing local resources

posed on this flip-flop would be to hold its previous state and not to propagate this invalid state to its outputs until it has decided to settle in a "0" or a "1" state. By doing so it could be guaranteed that the outputs of a flip-flop will never be in an undetermined state even though the flip-flop may internally be in a metastable state. The penalty that the user would expect to pay in such a design will be a propagation delay that can extend beyond the maximum specified in the data sheet.

74F786- 4-Input Asynchronous Arbiter

The key consideration when arbitrating for shared resources is that access may not be granted to more than one device at a given time. If this could be guaranteed, it would improve reliability. This application note describes a product from Signetics, which guarantees against simultaneous grants and does so at very high speeds. The Signetics 74F786 (Figure 3) is a general purpose asynchronous bus arbiter designed to address the needs for real-time applications, where arbitration is desired between multiple devices sharing common resources. The design goal was to provide for a device, the outputs of which could be guaranteed against logic hazards (glitches), metastability and that no more than one output could be active at a given time. The arbiter has four Bus Request ($\overline{BR}_n$) inputs which allow arbitration between two to four asynchronous inputs. The priority

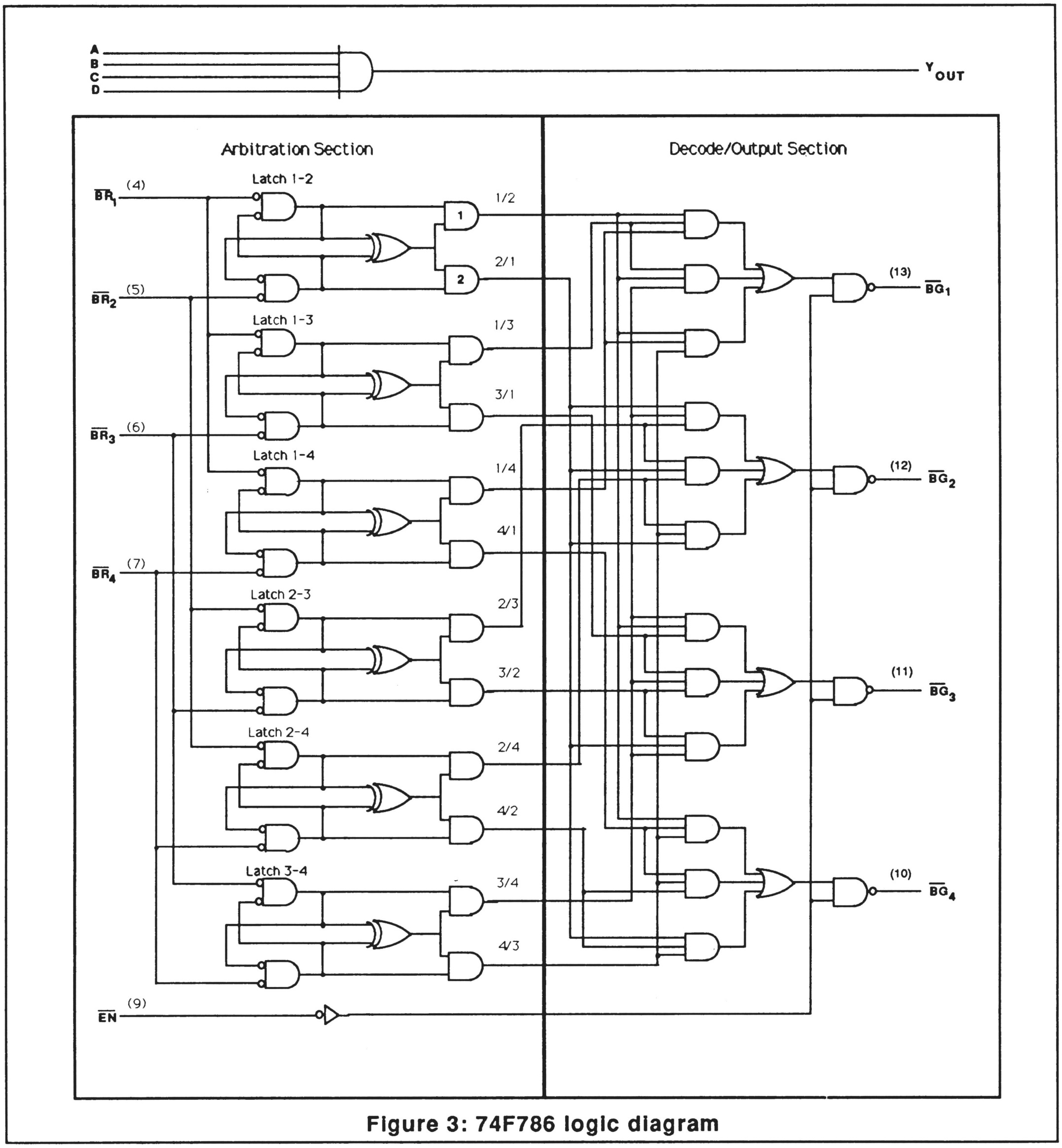

A
B
C
D
Y OUT
Arbitration Section
Decode/Output Section
BR1 (4)
BR2 (5)
BR3 (6)
BR4 (7)
EN (9)
Latch 1-2
Latch 1-3
Latch 1-4
Latch 2-3
Latch 2-4
Latch 3-4
1
2
1/2
2/1
1/3
3/1
1/4
4/1
2/3
3/2
2/4
4/2
3/4
4/3
(13) BG1
(12) BG2
(11) BG3
(10) BG4

Figure 3: 74F786 logic diagram

is determined on a first-come-first-served basis. Corresponding to each input is a separate Bus Grant ($\overline{BG}_n$) output which indicates which one of the request inputs is served by the arbiter at a given time. All these outputs are enabled by a common enable ($\overline{EN}$) input. Also included on-chip, is a general purpose four-input AND gate which may be used to generate a bus request signal (Figures 2) or as an independent AND gate.

Since the Bus Request inputs have no inherent priority, the arbiter assigns priority to the incoming requests as they are received. Therefore, the first request asserted will have the highest priority. When a Bus Request is received, its corresponding Bus Grant becomes active, provided $\overline{EN}$ is LOW, and no other Bus Grant is active. Typically, a Bus Grant is selected in 6.6 nsec from the time of assertion of a request input. If additional Bus Requests are made after the first request goes LOW, they are queued in their respective order. When the first request is removed, the arbiter services the request with the next highest priority, based upon a first-come-first-served algorithm.

Metastable-Free Outputs

The 74F786 logic diagram (Figure 3) consists of two sections: the arbitration section and the decoding/output section. Within the arbitration section lie six independent 2-input arbiters each of which arbitrates between the two Bus Request ($\overline{BR}_n$) inputs connected to that specific arbiter. Each 2-input arbiter is comprised of two cross-coupled NOR gates, an EX-OR gate and two AND gates. The cross-coupled NOR gates are designed so that they are securely latched when a schottky diode voltage difference appears between the outputs of these NOR gates. The EX-OR gate is designed so that its output will remain LOW until there is at least 1Vbe difference between its inputs. This creates a noise-margin of 1Vbe (base to emitter voltage)-1Vsky (schottky voltage) ≈ 0.3 Volts and assures that the output of the EX-OR will not go HIGH until after the two NOR gates have resolved any contention problems. This guarantees that neither of the outputs of a 2-input arbiter can be in a metastable state, and also that both outputs cannot be high simultaneously. As is clear from Figure 3, the first 2-input arbiter is responsible for deciding between the $\overline{BR}_1$ and $\overline{BR}_2$ inputs. Since both AND gate outputs cannot be high at the same time, the other three possible configurations are; First, AND gate1 is HIGH indicating that $\overline{BR}_1$ arrived at the latch before $\overline{BR}_2$ (designated 1/2); second, AND gate2 is HIGH indicating $\overline{BR}_2$ arrived before $\overline{BR}_1$ (designated 2/1) and third both AND gates are LOW indicating that neither $\overline{BR}_1$ nor $\overline{BR}_2$ has been latched.

Glitch-Free Outputs

The decode section of the 'F786 is responsible for insuring that the outputs do not glitch or produce a logic hazard. While there are three possible Karnaugh mappings, to produce an optimum decode section with a minimum number of transistors and balanced propagation times, the mapping in Table 1 was chosen. Solving Table 1 for $\overline{BG}_1$-$\overline{BG}_4$ yields the following equations:

$\overline{BG}_1=1/2.1/3.1/4+1/2.1/3.3/4+1/2.1/4.4/3$
$\overline{BG}_2=2/1.2/3.2/4+2/1.2/3.3/4+2/1.2/4.4/3$
$\overline{BG}_3=3/1.3/2.3/4+1/2.3/1.3/4+2/1.3/2.3/4$
$\overline{BG}_4=4/1.4/2.4/3+1/2.4/1.4/3+2/1.4/2.4/3$

To see if a glitch can occur let's take the worst possible case, that is, let $\overline{BR}_1$ beat $\overline{BR}_2$, 2 beat 3, 3 beat 4 and 4 beat 1 (a possible situation when all inputs are asserted simultaneously). Also, let's have the outputs of the arbitration section switch sequentially. Initially, all the variables in the equations are false (remember, the outputs of the arbitration section have three possible states). First, when 1/2 goes true 2/1 must remain false. This eliminates several terms from playing a role in deciding which output becomes active. In fact, $\overline{BG}_2$ has been removed from the list and is no longer a contender. At this point, while all the outputs are high (inactive) we have decided that $\overline{BG}_2$ will remain inactive. This leaves us with the following equations.

$\overline{BG}_1=1/2.1/3.1/4+1/2.1/3.3/4+1/2.1/4.4/3$
$\overline{BG}_3=3/1.3/2.3/4+1/2.3/1.3/4+\cancel{2/1.3/2.3/4}$
$\overline{BG}_4=4/1.4/2.4/3+1/2.4/1.4/3+\cancel{2/1.4/2.4/3}$

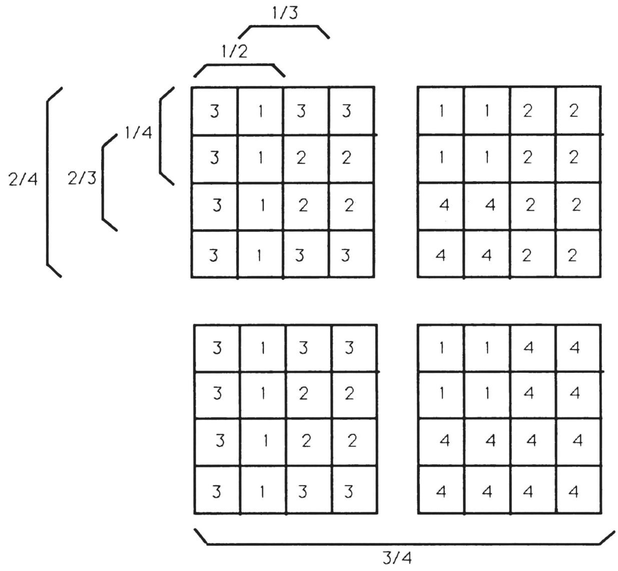
Similarly when 2/3 goes true 3/2 must remain false, which further eliminates a term from thus set of 3 equations.

$\overline{BG}_1=1/2.1/3.1/4+1/2.1/3.3/4+1/2.1/4.4/3$
$\overline{BG}_3=\cancel{3/1.3/2.3/4}+1/2.3/1.3/4+\cancel{2/1.3/2.3/4}$
$\overline{BG}_4=4/1.4/2.4/3+1/2.4/1.4/3+\cancel{2/1.4/2.4/3}$

Now when 3/4 goes true 4/3 must remain false. This eliminates $\overline{BG}_4$ from the contending list and the contest now is between $\overline{BG}_1$ and $\overline{BG}_3$ as indicated from the following equations.

$\overline{BG}_1=1/2.1/3.1/4+1/2.1/3.3/4+\cancel{1/2.1/4.4/3}$
$\overline{BG}_3=\cancel{3/1.3/2.3/4}+1/2.3/1.3/4+\cancel{2/1.3/2.3/4}$

When 4/1 goes true 1/4 must remain false.


1/3
1/2
1/4
2/4
2/3
3/4

3	1	3	3	1	1	2	2
3	1	2	2	1	1	2	2
3	1	2	2	4	4	2	2
3	1	3	3	4	4	2	2
3	1	3	3	1	1	4	4
3	1	2	2	1	1	4	4
3	1	2	2	4	4	4	4
3	1	3	3	4	4	4	4

Table 1: 74F786 Karnaugh mappings

Still no decision has been made and is dependent on the two 2-4 and 1-3 latches not taken into account yet. In this case the 2-4 latch status is a don't care, so the outcome of the 1-3 latch dictates the Bus Request granted.

$\overline{BG}_1$=1/2.1/3.3/4
$\overline{BG}_3$=1/2.3/1.3/4

If the 1-3 latch settles in the 1/3 state $\overline{BR}_1$ gets the grant, and with 3/1 remaining false, $\overline{BG}_3$ will remain inactive. Similarly if the 1-3 latch goes to the 3/1 state $\overline{BR}_3$ gets the grant, and with 1/3 remaining false $\overline{BG}_1$ will remain inactive.

Notice that the Bus Grant was given in this case without regard to the 2-4 latch. In fact, a quick review shows that neither the 2-3 latch nor the 1-4 latch played a role in making the decision. Each grant is dependent on the state of three latches. By the nature of the encoding logic, as the three activating latches are switched, three outputs are forced to remain in an inactive state. This insures a glitch-free output.

Let's assume that in the example above, the 1-3 latch goes to the 1/3 state and hence $\overline{BG}_1$ is asserted. At this time the other five latches in the circuit will be in 1/2, 4/1, 2/3, 2/4 and 3/4 states. If at this point $\overline{BR}_3$ is removed, then latch 3-4 changes from 3/4 to 4/3 and hence $\overline{BR}_4$ steals the grant (with 1/2.4/1.4/3). This concludes that if three or more requests are asserted precisely at the same time, and one of them is removed prior to being serviced, it may cause premature termination of the present grant and assertion of another grant. Therefore, when using three or more Bus Requests it is not advised to remove a request before being serviced. On the other hand, arbitration between two requests does not have this restriction. The user if necessary, may decide to remove an ungranted request at his discretion.

Extended Propagation Delays

Since the outputs of the six 2-input arbiters can not display a metastable condition, the Bus Grant outputs can not display a metastable condition because the decoding/output section does not have any storage element to go metastable. Even though the Bus Grant outputs can't go metastable, the cross-coupled NOR gates can. To determine the metastability characteristics of these NOR gates, the 'F786 was evaluated by Mr. Thomas J. Chaney of Washington University in St. Louis, Missouri, who is considered to be a leading expert in this field. Table 2 gives of the 19 devices supplied to him, the test results from the fastest, the slowest and a typical package. In order to determine the Mean Time Between Package Unresolved (MTBPU) with the relative arrival times of the two input signal transitions uniformly distributed, the following formula is used:

MTBPU= $[\exp(t'/\tau)]/[T_0(\text{Input 1 rate})(\text{Input 2 rate})]$.

Where:

t'= Time given to resolve contention between inputs after they are asserted and τ and T_0 are device parameters derived from tests and can most nearly be defined as:

τ= A function of the rate at which a latch in a metastable state resolves that condition.

& T_0= A function of the measurement of the propensity of a latch to enter a metastable state. T_0 is also a very strong function of the normal propagation delay of the device.

Solving for t', the resolving time measured from the arrival of the first input, and setting up the equation so the value of T_0 in Table 2 (given in nsec.) can be substituted directly is:

$t'=(\tau)\ln[(T_0)(3E14)]$.

The implication of the above equation is that, even though typical propagation delay through the arbiter is about 6.6nsec, contention between inputs may extend this time significantly and can be calculated from Table 2.

Package	Latch	Output Measured	τ (nsec)	T_0 (nsec)	h (nsec)	t' for 1 failure/century (inputs at 10E6hz)
FASTEST	1-2	13	.38	175E2	6.6	16.6
	1-3	13	.39	79E2	6.6	16.4
	1-4	13	.39	69E2	6.6	16.4
	2-3	12	.38	109E2	6.6	16.1
	2-4	12	.39	68E2	6.6	16.5
	3-4	11	.38	181E2	6.6	16.3
SLOWEST	1-2	13	.44	34E2	6.6	18.1
	1-3	13	.44	17E2	6.6	18.0
	1-4	13	.43	26E2	6.6	17.8
	2-3	12	.44	16E2	6.6	17.9
	2-4	12	.46	8E2	6.6	18.5
	3-4	11	.44	29E2	6.6	18.2
TYPICAL	1-2	13	.41	56E2	6.6	17.3
	1-3	13	.42	24E2	6.6	17.2
	1-4	13	.43	17E2	6.6	17.5
	2-3	12	.43	18E2	6.6	17.4
	2-4	12	.39	72E2	6.6	16.6
	3-4	11	.41	49E2	6.6	17.2

Where h= typical propagation delay through the device.

Table 2: 74F786 test results for all latches for three packages.
All tests with V_{cc}=5.0vdc and at room temperature

AN217

Metastability Tests For The 74F786- A 4-Input Asynchronous Bus Arbiter

Application Note

INTRODUCTION

Under contract with Signetics, Mr. Thomas J. Chaney of Washington University, St. Louis tested a set of nineteen 74F786 samples (packages) to determine the metastable state recovery statistics for the circuits. The tests were conducted using a procedure described in a paper entitled "Characterization and Scaling of MOS Flip-Flop Performance", (section IV), by T. Chaney and F. Rosenberger, presented at the CalTech Conference on VLSI, Jan. 1979. The general test procedure was to test all 19 packages under one condition, then test the best, worst, and an average package in more detail. According to Mr. Chaney, the test results from the 19 packages formed one of the tightest groupings that he had ever seen. As the parts were numbered, package No. 7 had the fastest resolving times, No.11 produced some of the slowest resolving times, and No.1 had resolving times near the middle of the test results. This ranking of the test results from 3 packages remained the same through out the balance of the test program, which supports the complete testing of only 3 packages. In general, the poorest performance resulted when the packages were heated to near 75 °C with Vcc = 4.5vdc and the best performance resulted when the packages were cooled to near 0 °C with Vcc = 5.5vdc.

The variation within one package caused by the temperature and Vcc changes was greater than the variation from package to package. It must be noted that none of the packages tested even approached the data sheet input to output worst case propagation delay of 10.5ns. All the packages tested for a single active output, had propagation delays of about 6ns. Typically, the parts with longer propagation delays also have slower resolving times. Thus one would expect that the delay time needed to have only one failure in 32 years using a 10nsec. propagation delay part would be much longer than a value derived from just adding 10-6=4 ns to the above calculations. Thus it appears that the poorest performance measured in this study should be considered a measurement at the edge of the typical range for 74F786 parts.

It must also be noted that the tight grouping of this set of packages means that, when comparing differences between these test results, the measured error, as outlined in "Measured Flip-Flop Responses to Marginal Triggering", IEEETC, Dec. 1983, is significant. This is illustrated in association with Table 5.

Test Program And Data

Through out the test period, the connections to some of the package pins was as shown in Figure 1. The 4 input pins (1, 2, 3 and 15) to the AND gate were all grounded. The output of the AND, pin 14, was left open. The output enable $\overline{\text{EN}}$ pin (9) was grounded. The power ground pin (8) was grounded and the Vcc power pin (16) was connected to Vcc. The 4 input pins to the arbiter (4, 5, 6 and 7) were treated as a group with two of the pins always receiving an input from the tester and the other two inputs always connected to Vcc through 1KΩ resistors. For any arbiter input pair configuration, there are two outputs (of the set: Pins 10, 11, 12 and 13) active. These two active output pins are each connected to a grounded 510Ω resistor, a grounded 30pF silvered mica capacitor, and a grounded scope probe (13pF). Thus each active output pin has a load of approximately 500Ωs to ground and 50pF to ground (43pF plus 5 to 10pF wiring capacitor). In addition, the active output pin being tested was connected to the input of a comparator (3pF max.). The other input to this comparator was referenced to 1.5vdc. The 1.5vdc reference voltage was not varied with Vcc. The two arbiter input signals generated by the tester were negative going pulses, each of the same width (approximately 100ns), which were time shifted relative to each other to produce metastable behavior in the arbiter circuit. This form of input causes only one of the two possibly active outputs to switch low.

First Pass Through Packages

The test conditions used for the selection process from the 19 packages is shown in Figure 1 with the results shown in Table 1. The values reported in Table 1 were calculated with t' (defined later) at 7.60 and 9.93ns. Note that the active inputs are pins 6 and 7 and the output tested is pin 11. The last column of this table is the period, after two requests, required to assure that the pack-

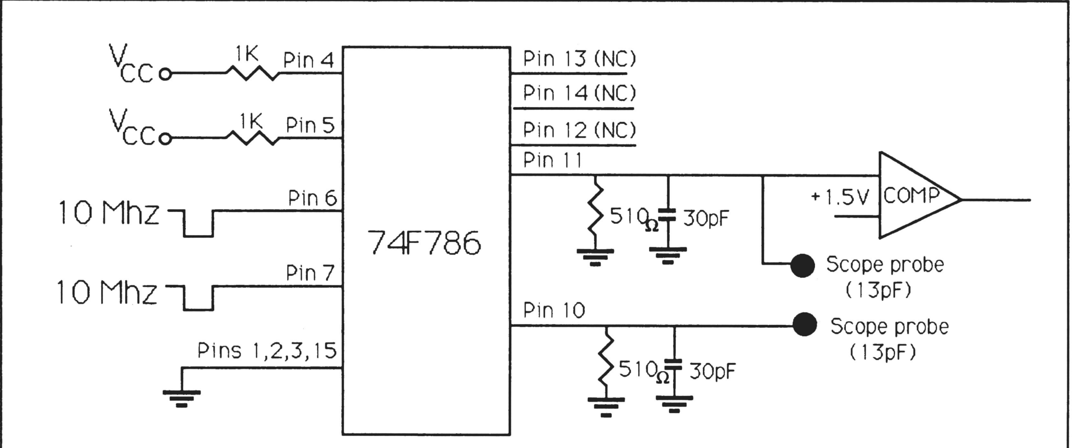


Figure 1: Test set-up for the 74F786

July 18, 1988

age would fail to resolve less than once per century. These numbers are based on the assumption that the 2 inputs are not synchronized and both are running at 10mhz (a 100ns clock period). It is assumed that the relative arrival times of the two input signal transitions are uniformly distributed over the clock period. The Mean Time Between Package Unresolved (MTBPU) is then:

MTBPU = $[\exp(t'/\tau)/[(T_0)(\text{Input1 rate})(\text{Input2 rate})]$

Where:
t'= Time given to resolve contention between inputs after they are asserted and τ and T_0 are device parameters derived from tests and can most nearly be defined as:
τ = A function of the rate at which a latch in a metastable state resolves that condition and
T_0= A function of the measurement of the propensity of a latch to enter a metastable state. T_0 is also a very strong function of the normal propagation delay of the device. Also one century = 3E9 seconds.

Solving for t', the resolving time measured from the arrival of the first request, and setting up the equation so the value of T_0 in Table 1 (given in ns) can be substituted directly gives:

$$t' = (\tau)1n[(T0)(3E14)]$$

As a result of the first round of tests, three packages were selected for further testing. Package 7 was selected as the fastest, package 11 as the slowest, and package 1 as a typical package.

Package Number	τ (ns)	T_0(ns)	h (ns)	t' for 1 failure/century (inputs at 10E6hz)
1	0.44	17E2	6.6	17.8
2	0.44	15E2	6.6	18.0
3	0.39	12E2	6.6	16.6
4	0.46	9E2	6.6	18.5
5	0.44	9E2	6.6	17.7
6	0.40	63E2	6.6	16.9
7	0.39	103E2	6.6	16.6
8	0.46	8E2	6.6	18.6
9	0.44	22E2	6.6	18.1
10	0.46	9E2	6.6	18.4
11	0.45	18E2	6.6	18.5
12	0.45	14E2	6.6	18.3
13	0.45	11E2	6.6	18.3
14	0.45	15E2	6.6	18.2
15	0.45	11E2	6.6	18.2
16	0.43	30E2	6.6	17.6
17	0.44	16E2	6.6	18.0
18	0.39	126E2	6.6	16.9
19	0.43	31E2	6.6	17.8

Table 1: Test results for inputs on pins 6 & 7 and ouput measured at pin 11. V_{cc} = 5.0vdc at room temperature. t' = 7.60 and 9.93ns

Input Pins	Latch Under Test	Output Pins Active
4,5	Latch 1-2	13,12 - test pin 13
4,6	Latch 1-3	13,11 - test pin 13
4,7	Latch 1-4	13,10 - test pin 13
5,6	Latch 2-3	12,11 - test pin 12
5,7	Latch 2-4	12,10 - test pin 12
6,7	Latch 3-4	11,10 - test pin 11

Table 2: Arbiter inputs and corresponding latches and output mapping

Second Set Of Tests

Using the logic diagram of the 74F786 (Figure 2), it is possible to construct Table 2. Note from Table 2 that thus far, all testing has been conducted on latch 3-4 (pins 6 &7). The second set of tests, conducted only on the 3 packages selected from the first set of tests, involved testing each of the 6 latches in the package to select the poorest performing latch in each package. This step also included testing each of the two active output pins for each input condition to select the path with the longest propogation delay.

Package Number	Latch	Output Measured	τ (ns)	T_0(ns)	h (ns)	t' for 1 failure/century (inputs at 10E6hz)
7	1-2	13	.38	175E2	6.6	16.6
7	1-3	13	.39	79E2	6.6	16.4
7	1-4	13	.39	69E2	6.6	16.4
7	2-3	12	.38	109E2	6.6	16.1
7	2-4	12	.39	68E2	6.6	16.5
7	3-4	11	.38	181E2	6.6	16.3
11	1-2	13	.44	34E2	6.6	18.1
11	1-3	13	.44	17E2	6.6	18.0
11	1-4	13	.43	26E2	6.6	17.8
11	2-3	12	.44	16E2	6.6	17.9
11	2-4	12	.46	8E2	6.6	18.5
11	3-4	11	.44	29E2	6.6	18.2
1	1-2	13	.41	56E2	6.6	17.3
1	1-3	13	.42	24E2	6.6	17.2
1	1-4	13	.43	17E2	6.6	17.5
1	2-3	12	.43	18E2	6.6	17.4
1	2-4	12	.39	72E2	6.6	16.6
1	3-4	11	.41	49E2	6.6	17.2

Table 3: Test results for all 6 latches from packages 7, 11 and 1. All tests with V_{cc} = 5.0vdc and at room temperature

The results of this comparison testing is shown in Table 3. The results from this Table indicate that latches 1-2 and 3-4 have longer propogation delays than the middle four latches. This propagation delay difference is less than 0.4ns. For each of the conditions tested and reported in Table 3, there is a second active pin that could have been used to measure the performance of the latch under test. For package 1 only, the other active pin was tested for each of the latchs. The results of this test are shown in Table 4. In theory, the results should be the same except for possible differences in propogation delay. The value of τ should be the same, but the value of T_0 could be different. In all 6 cases, the active pin previously not tested had a shorter propagation delay (function of T_0) than the active pin that was tested.

Table 4 also indicates something else. That

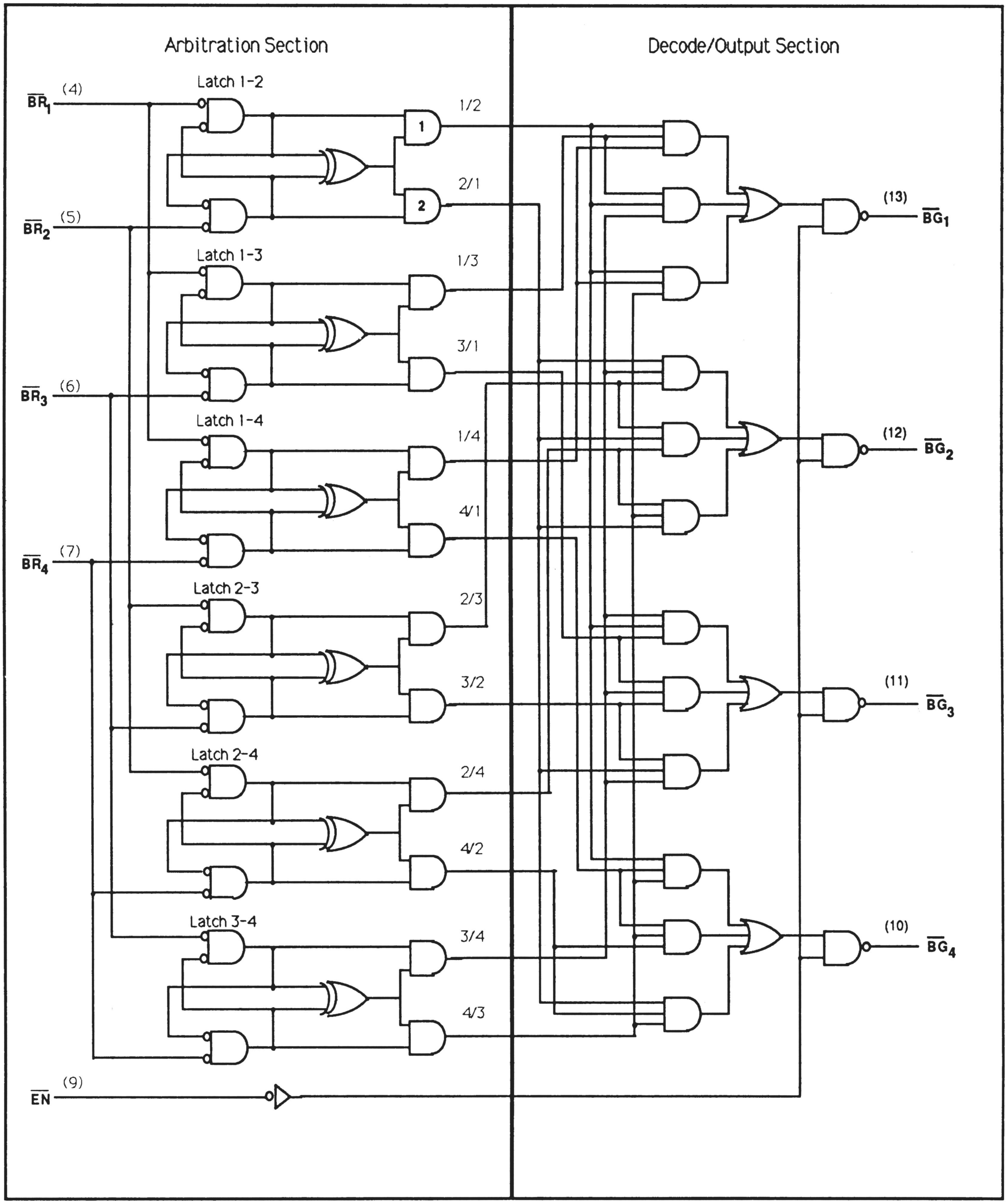

Arbitration Section
Decode/Output Section
$\overline{BR}_1$ (4)
$\overline{BR}_2$ (5)
$\overline{BR}_3$ (6)
$\overline{BR}_4$ (7)
$\overline{EN}$ (9)
Latch 1-2
Latch 1-3
Latch 1-4
Latch 2-3
Latch 2-4
Latch 3-4
1
2
1/2
2/1
1/3
3/1
1/4
4/1
2/3
3/2
2/4
4/2
3/4
4/3
(13) $\overline{BG}_1$
(12) $\overline{BG}_2$
(11) $\overline{BG}_3$
(10) $\overline{BG}_4$

Figure 2: 74F786 logic diagram

is the accuracy with which the data in this report can be interpreted. Note that τ varies as much as 0.05ns, which is within the 0.06ns measurement error range of the test equipment used.

The results of the second set of tests are:
(1) The 6 latches in each of the 3 selected packages behaved the same, relative to each other.
(2) In all 3 packages, the latch selected is of little importance, therefore, Latch1-2 was selected at random for further testing.
(3) It was reasonable to continue with the 3 selected packages and to restrict further testing to latch1-2 and to only record data from pin 13.

Temperature And Power Supply Variation Testing

The temperature and power supply variation testing was conducted on packages 1, 7 and 11. These tests were conducted on latch1-2 only of each package (inputs 4 and 5, results measured at pin 13). The results are shown in Table 5. The poorest performance was measured again from package 11. The worst case condition was measured at Vcc = 4.5vdc and the case temperature at 75°C and is shown in Table 5 as a bold entry. This line gives what could be considered the worst case measured performance from the 19 packages tested.

Package Number	Latch	Output Measured	τ (ns)	T_0(ns)	h (ns)	t' for 1 failure/century (inputs at 10E6hz)
1	Latch 1-2	13	0.41	156E2	6.6	17.3
1	Latch 1-2	*13	0.39	160E2	6.6	16.8
1	Latch 1-2	12	0.36	390E2	6.6	15.8
1	Latch 1-3	13	0.42	24E2	6.6	17.2
1	Latch 1-3	*13	0.39	101E2	6.6	16.5
1	Latch 1-3	11	0.36	137E2	6.6	15.6
1	Latch 1-4	13	0.43	17E2	6.6	17.5
1	Latch 1-4	*13	0.40	77E2	6.6	16.7
1	Latch 1-4	10	0.35	201E2	6.6	15.3
1	Latch 2-3	12	0.43	18E2	6.6	17.4
1	Latch 2-3	*12	0.40	63E2	6.6	16.7
1	Latch 2-3	11	0.37	88E2	6.6	15.5
1	Latch 2-4	12	0.39	72E2	6.6	16.6
1	Latch 2-4	*12	0.39	79E2	6.6	16.6
1	Latch 2-4	10	0.36	96E2	6.6	15.5
1	Latch 3-4	11	0.41	49E2	6.6	17.2
1	Latch 3-4	*11	0.40	99E2	6.6	16.9
1	Latch 3-4	10	0.36	246E2	6.6	15.7

*These values were computed using the subset of sample times used to measure the response from the other active pin in each case.

Table 4: Test results for all 6 latches from package 1, measured and/or computed different ways. All tests with V_{cc} = 5.0vdc and at room temperature

Package Number	V_{cc}	Temperature	τ (ns)	T_0(ns)	h (ns)	t' for 1 failure/century (inputs at 10E6hz)
7	4.5	3 °C	0.37	260E2	6.6	16.3
7	5.5	3 °C	0.38	67E2	6.6	15.8
7	4.5	75 °C	0.44	70E2	6.6	18.4
7	5.5	75 °C	0.43	37E2	6.6	17.7
11	4.5	3 °C	0.41	88E2	6.6	17.4
11	5.5	3 °C	0.39	64E2	6.6	16.6
11	4.5	Room Temp.	0.42	76E2	6.6	17.9
11	5.5	Room Temp.	0.42	30E2	6.6	17.5
11	4.5	75 °C	0.50	15E2	6.6	20.3
11	**4.5**	**75 °C**	**0.51**	**8E2**	**6.6**	**20.6**
11	5.5	75 °C	0.47	19E2	6.6	19.3
1	4.5	Room Temp.	0.42	93E2	6.6	17.7
1	5.5	Room Temp.	0.42	48E2	6.6	17.1
1	4.5	75 °C	0.44	69E2	6.6	18.7
1	5.5	75 °C	0.44	37E2	6.6	18.3

Table 5: Test results for latch1-2 from packages 7,11 and 1.All tests with V_{cc} = 4.5vdc-5.0vdc and temperatures from 0°C to 75°C

AN218
DESIGN HIGH PERFORMANCE MEMORY BOARDS USING FAST LOGIC AND SIMPLE TRANSMISSION LINE TECHNIQUES
Application Note

INTRODUCTION AND OVERVIEW

With ever increasing memory speeds and correspondingly higher speed drivers, transmission line effects in memory boards are becoming more and more of a problem. An engineer can easily control, manipulate or work around the transmission line effects if he has all the information he needs and he understands how to use it. This article will supply that information and understanding as well as a fairly detailed look at some of the most common problems encountered in memory board design.

The article has three main parts. The first part lists and briefly explains the transmission line equations which will be used in the rest of the paper. The second part provides capacitance, inductance, and driver current/voltage information which is useful when applying the transmission line equations to memory boards. The third part is a detailed look at problems which often arise in memory board design and an evaluation of the solutions in common use.

PART 1: TRANSMISSION LINE EQUATIONS

A signal line in the memory array of a bare printed circuit board has both capacitance and inductance (L) distributed along its length. When the memory chips are inserted, the input capacitance of each input the signal line must drive is added to the line's distributed capacitance to give the total capacitance (C). The characteristic impedance (Z_0) of the signal line is given by Equation 1. Note that since (L) and (C) are both directly proportional to the length of the line, characteristic impedance is not a function of line length.

Eq. 1 $Z_0=(L/C)^{1/2}$

Equation 2 gives the current (I) a driver needs to source in order to change the voltage on a signal line by an amount (V). Notice that I-V relationship of the line at its input is that of a resistance (Z_0) to the voltage existing on the line before the driver tried to change it.

Eq. 2 $I=V/Z_0$

When the voltage is changed at the driven end of a signal line, the voltage wave travels down the line at a finite speed. Equation 3 gives the time (T) it takes for a transition to propagate from one end of the signal line to the other.

Eq. 3 $T=(LC)^{1/2}$

When a voltage wave ($V_{incident}$)travels down a signal line and encounters an impedance change from Z_0 to some new impedance (Z_1), $V_{incident}$ will split into a reflected part ($V_{reflected}$) and transmitted part ($V_{transmitted}$). $V_{reflected}$ will (as the name implies) travel back up the line toward the driver, and $V_{transmitted}$ will travel on down the line in the original direction of propagation. $V_{reflected}$ and $V_{transmitted}$ are given by Equations 4 and 5.

Eq. 4 $V_{reflected}=V_{incident}(Z_1-Z_0)/(Z_1+Z_0)$

Eq. 5 $V_{transmitted}=V_{incident}+V_{reflected}$

PART 2: TRANSMISSION LINE PARAMETERS IN MEMORY BOARDS

In order to use the preceding equations, an engineer will need to know the inductance and the capacitance of the signal lines in his memory board, and the output I-V relationship of the drivers on that board. This section provides the information needed for a quantitative understanding of all the examples which will be shown later. However, there are simply too many memory drivers and memory parts to fully document here. The information will still provide a very broad qualitative understanding of transmission line behavior in memory boards, and this qualitative understanding is a very powerful design and debug tool.

INDUCTANCE AND CAPACITANCE

Figures 1 and 2 show how the distributed inductance and capacitance of a signal line vary with width and dielectric thickness on a fiberglass memory board with a ground plane. These figures are not exact, but they don't have to be exact. A 15 percent error in the calculated characteristic impedance or propagation delay of a memory board signal line is unlikely to cause any problems, and this means that a 30 to 35 percent error in the inductance or the capacitance of a signal line will likely be allowable (because of the square root relationship between L and C and Z_0). By the same reasoning, a typical input capacitance of 3pF is suggested for calculations, although from some memory suppliers it will be closer to 2pF, while from others it will be closer to 4pF.

Note that on a two layer memory board there is no ground plane, so Figures 1 and 2 can't be applied. The distributed capacitance for 15 mil line on a typical 60 mil thick two layer memory board is about 1pF/inch, and the distributed inductance is around 20nH/inch.

BALLPARK CALCULATIONS

Ballpark estimates for the characteristic impedance and propagation speed can be calculated using the preceding information and typical packing densities for various memory packaging modes. The dual-in-line package (DIP), for instance, is typically packed on a board at around a 0.5 inch pitch so that there are two inputs for a one inch length of line. This means that the input capacitance on a one inch length of line will be 6pF. Figures 1 and 2 show that for a typical four layer memory board, with a line width of 10 mils and a dielectric thickness of 15 mils, the distributed capacitance for a one inch length of line will be about 3pF, and the distributed inductance for the line will be about 12nH. The values for L and C (required for use in Equations 1 and 3) for this one inch DIP

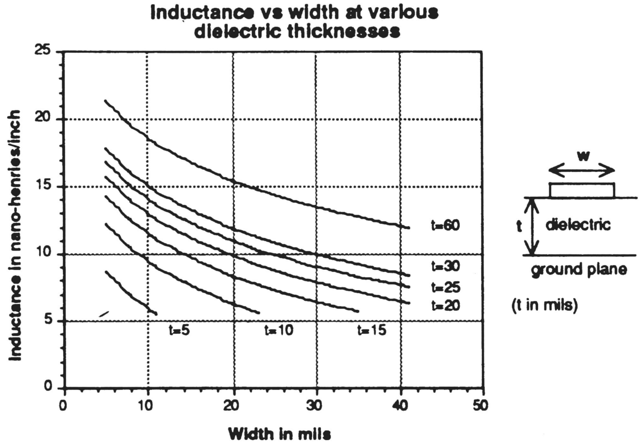


Figure 1

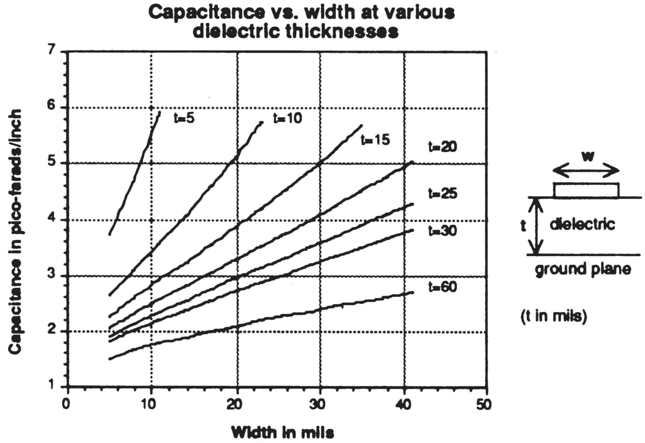


Figure 2

Package	Pitch	L	C	Z0	T
DIP	0.5 inch	12 nH	9 pF	37 ohms	0.3ns
ZIP	0.2 inch	12 nH	18 pF	26 ohms	0.5ns
SIP	0.3 inch	12 nH	103 pF*	11 ohms	1.1ns

* SIP capacitance includes on-module wiring capacitance of 6 pF per module.

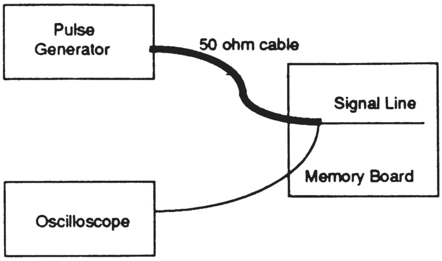
Table 1

memory line will be 12nH and 9pF. The ballpark characteristic impedance and propagation delay for one inch lengths of DIP, ZIP, and SIP memory lines are shown in Table 1.

MEASURING IMPEDANCE AND PROPAGATION DELAY

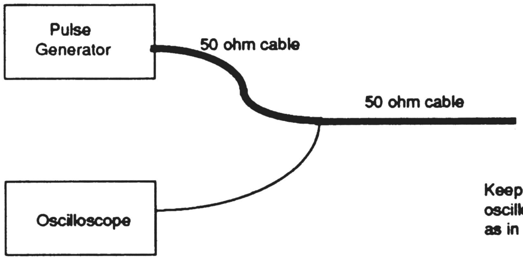
Often an engineer will want to analyze a board which has already been built. In this case, it is easy to directly measure the characteristic impedance and the propagation delay of the signal lines using an oscilloscope and a pulse generator rather than calculating it from its inductance and capacitance. To do this, connect the pulse generator, unterminated signal line, and oscilloscope as shown in Figure 3a. The oscilloscope waveform will have the same basic shape as the one in Figure 3c. The initial voltage drop (V1) is the transmitted signal from the 50 ohm cable to the signal line, and the second voltage drop (V2) is its reflection from the unterminated (infinite impedance terminated) end of the signal line. Notice that for a change in impedance from some finite impedance (Z_0) to an infinite impedance, Equation 4 predicts that the reflected signal will be of the same magnitude and sign as the incident signal, i.e., the initial voltage drop will travel to the end of the line and then reflect as a voltage drop of the same magnitude as the first, and then it will propagate back up the signal line to the oscilloscope input. The time difference (2T) between the midpoints of these two voltage drops is twice the propagation delay of the signal line. Measure V1 and record it as $V_{transmitted}$. Then replace the signal line with a length of 50 ohm cable about a meter long as shown in Figure 3b. The oscilloscope waveform will still have the same basic shape, but the initial voltage drop will probably be different. Since this time the initial voltage drop (V1) is the transmitted signal from 50 ohms to 50 ohms, it will be equal to the incident signal. Measure V1 and this time record it as $V_{incident}$. Application of Equations 4 and 5 followed by a little algebraic manipulation yields the characteristic impedance of the signal line:

$$Z_0 = (V_{transmitted}/(2V_{incident} - V_{transmitted}))\ 50\Omega$$



Notes: The pulse generator must be set with a low enough amplitude and a high enough DC offset that reflections don't go below ground or above Vcc. The signal's edge rate must be less than twice the line delay. The oscilloscope probe must have a high impedance. The memory board should have power applied and the memory chips installed.

Figure 3a



Keep the pulse generator and oscilloscope settings the same as in Figure 3a.

Figure 3b

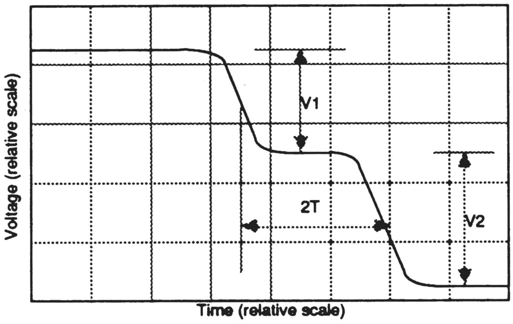


Figure 3c

DRIVER I-V CHARACTERISTICS

In order to anticipate the behavior of a particular driver in a memory board, an engineer will need to know the driver's I-V output characteristics. This information is given in Figures 4 and 5 for the parts which are used later as examples. Figure 4 shows the current each part will sink as a function of output voltage when it is in the low state, and Figure 5 shows the current each part will source as a function of output voltage when it is in the high state.

It should be noted that the curves for the 74F765 are representative of the standard 24ma FAST™ output, the curves for the 74F3037 are representative of the standard FAST™ 30 ohm line driver output, and the curves for the 74F765-1 are representative of all Signetics DRAM controllers which have a "dash one" designation.

PART 3: COMMON PROBLEMS AND THEIR SOLUTIONS

Transmission line problems in memory boards generally become significant when signal line propagation delays approach or exceed 1ns. The reasons for this will become apparent in the analysis of the following problems. A look at the "ballpark" estimates made earlier shows that a 1ns long transmission line translates to about 3 inches of DIP, 2 inches of ZIP, or 1 inch of SIP based memory line. Since these lengths are exceeded in most memory boards, transmission line problems are very common.

UNDERSHOOT

One of the most common problems noticed in memory design is a violation of the specified minimum input voltage of the memory chips (-1v). An example of this is shown in Figure 6 where a 24ma FAST™ part drives a 60 ohm line hard enough that the reflection at the opposite end of the line goes 3.5 volts below ground. This violation (usually referred to as "undershoot") would almost certainly cause the memory chips to malfunction.

The analysis of Figure 6 starts with a load-line method which proves to be very important for determining the incident wave. The 60 ohm transmission line of Figure 6 is initially settled to a high voltage of about 5 volts. When the line's driver then goes into the low state, its output voltage and current is given by the intersection of the driver's output I-V curve (Figure 4) with the input I-V curve of the transmission line. This input I-V curve is a line through the points (5v,0ma) and (0v,83ma) (from Equation 2), and the point of intersection of the two curves is about (.75v, 75ma). The incident voltage wave ($V_{incident}$) is a -4.25 volt change from 5 volts to .75 volts. This voltage wave propagates to the end of the line opposite the driver where it encounters an impedance change from 60 ohms to an infinite impedance. The reflected wave (from Equation 4) at this impedance change will be $V_{reflected} = V_{incident} = -4.25$ volts, i.e., a change from .75 volts to -3.5 volts, and subsequent reflections of this wave account for the continued peaks and valleys.

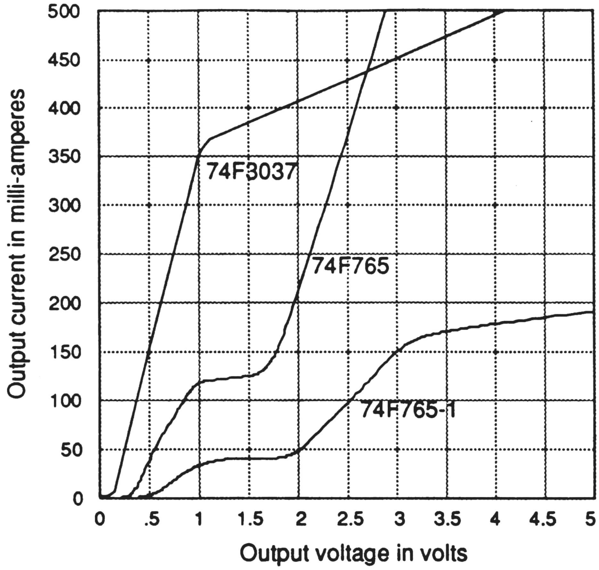


Figure 4 Voltage vs Current of Low State Outputs

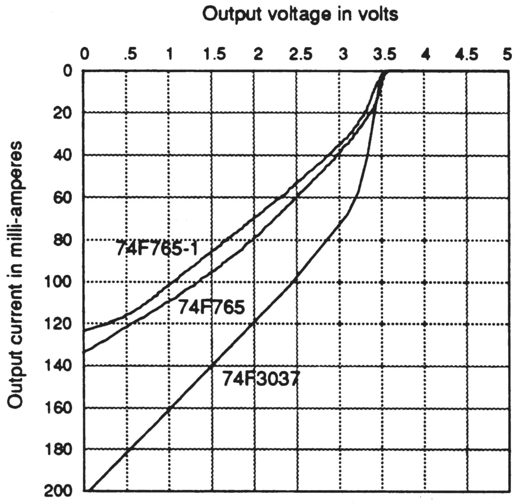


Figure 5 Voltage vs Current of High State Outputs

There are three basic methods an engineer can use to work around this problem.

Method 1. Use a slower driver and/or drive pieces of the line in parallel to effectively speed up the line.

Method 2. Increase the impedance of the driver or decrease that of the line.

Method 3. Put some finite impedance on the end of the line opposite the driver.

Method 1
(Slow Driver, Fast Line)

The idea behind the first method is to allow only one volt of the transition to fit onto the line at a time. By limiting the slew rate of the driver to less than 1 volt in twice the propagation delay of the line, one can guarantee that the undershoot will also be less than a volt. To apply this method to the example in Figure 6, we would break the 5ns long transmission line into four 1.25ns long sections and use a driver which made the 5 volt transition in a minimum of eight nanoseconds. The drawbacks of this method make it impractical for most designs. These drawbacks include:

- the requirement for a controlled slew rate driver with a very specific slew rate;
- the impact on timing due to the required slow transition time;
- the layout inconvenience of short memory lines in systems having more than an eight bit word.

Method 2
(Reflected Wave Switching, or "series termination")

The idea behind the second method is to reduce $V_{incident}$ to 50% of the total desired transition and then rely on the reflection from the unterminated end of the line to complete the transition. The usual way of doing this is by putting a resistor in series with the output of the driver (see Figure 7a) so that the impedance of the driver is roughly matched to that of the line. It is easy to show (from Equation 2) that this will result in an incident wave equal to half the desired transition and (from Equation 4) that the reflection from the unterminated end of the line will complete the transition. Since the driver's impedance is equal to that of the line, the reflected wave will not produce a second reflection when it returns to the driver (see Equation 4).

The two ends of a line driven with the series termination method are monitored by an oscilloscope in Figure 7b. Notice that the voltage at the driven end of the line is in the input threshold region for a time equal to twice the propagation delay of the line. This time spent in the threshold region often skews the address lines enough with respect to the row and column address strobes in dynamic memory boards that the row and column address setup times fail or become marginal. This problem can be avoided by allowing for an extra 2T worth of setup time in the design, but the increased delay quickly becomes

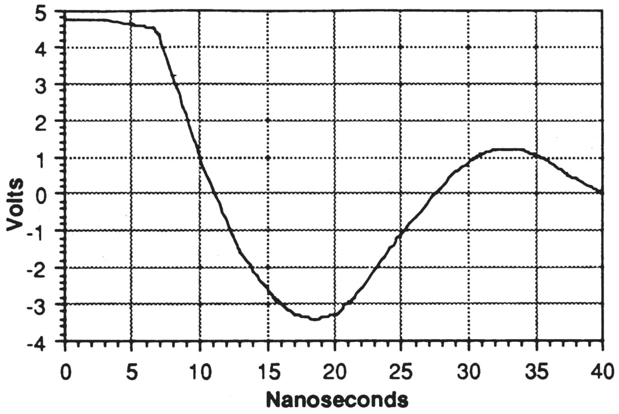


Figure 6 Oscilloscope view of the un-terminated end of an address line. The line has 32 DIPs, a line delay of 5ns, and it is driven by a 74F153.

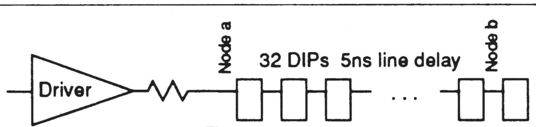


Figure 7a

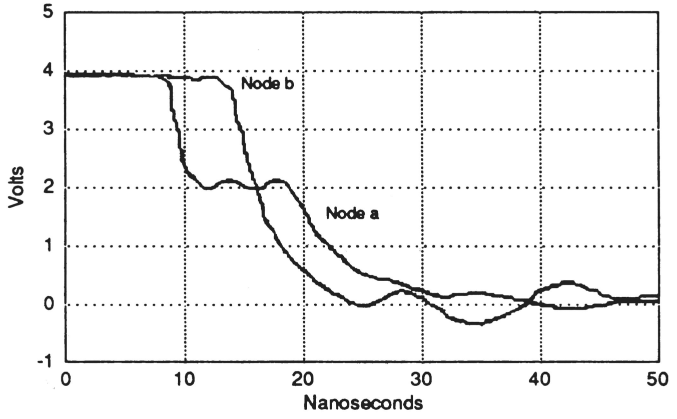


Figure 7b

a problem in large memory boards. Since any ground noise can easily cause multiple transitions to be made on signals which are left in the threshold region, this method should be used with caution on the strobe lines.

Series termination is probably the most widely used method for driving signal lines on memory boards. One reason for its popularity is that a very rough match between the driver's impedance and the impedance of the line will still make a memory line behave properly. It can be shown from Equations 2 and 4 that if the driver's impedance is within +50% and –40% of the line's characteristic impedance, the reflected wave will not violate the –1 volt minimum input voltage specification or the .8 volt maximum low input voltage specification. Thus a 30 ohm output impedance will work reasonably well with the ballpark estimates made previously for DIP and ZIP packages even if a large variation in input capacitance occurs from one memory chip vendor to the next.

The series termination method is offered by Signetics and several other companies in integrated circuits (the 74F721 and 74F723 for example). Signetics also offers an extension of this idea in some of its dynamic RAM controllers (see Figure 8). The output stage for these controllers will reflected wave switch lines in the 17 to 67 ohm range rather than the 18 to 45 ohm range one gets with the more conventional 30 ohm output impedance.

Method 3 (Terminations)

The basic idea behind this method is to place some terminating impedance at the end of the line opposite the driver. The simplest form of this would be a resistor ($R=Z_0$) to a constant voltage. In this case the reflection (undershoot) would be eliminated (see Equation 4). This termination can be generalized to the two resistor network in Figure 9c in which two resistors in parallel equal Z_0 and the terminating voltage is usually set to around three volts by a 2 to 3 ratio in the resistors. This termination offers very high performance, and it is particularly suited to high speed, high drive, open collector drivers like the 74F3038.

The high D.C. power dissipation of termination 9c can be avoided by using a capacitor to provide the constant voltage (see Figure 9e). This termination offers adequate undershoot suppression, and at the same time the lack of D.C. current flow often provides higher noise margins. This termination and the previous one should only be used in cases where the driver has adequate drive to fully switch the line with the incident wave, because there will be no reflection to make up for partial transitions.

Finally, Figure 9d shows a diode termination which can be used with any driver whether it is switching lines on the incident wave or not, and this termination has a lower power dissipation than either of the previous two terminations. This termination will also tend to speed up the transition time at the terminated end of the transmission line (notice that this transition time is always slow due to losses in

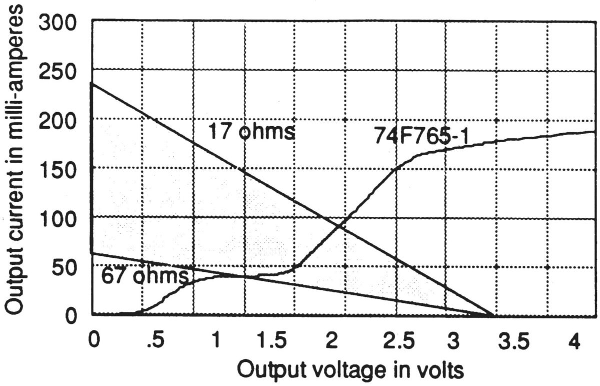


Figure 8 **Current vs voltage for 74F765-1 output and 17 to 67 ohm transmission lines settled to 4 volts. Since the intersection of the output curve with each of the transmission line curves is between 1.5 and 2.4 volts, these impedances are all suited to first reflected wave switching by the 74F765-1 (the incident wave to 2.4 v will reflect to .8 v and the incident wave to 1.5 v will reflect to -1 v).**

the line). The 74F133 has a high speed Schottky diode from ground to each of its 13 inputs, so it can be used as a low cost termination pack for this method. The method typically limits undershoot to just short of a volt which is not as good as can be achieved with the previous terminations, and the method is somewhat worse in relation to noise, but it can be used very effectively.

NOISE

Often, when one signal line is switched, voltage spikes (noise) will appear on adjacent lines. These voltage spikes can generally be traced to the lead frame inductance of the driver, the inductance of the ground plane, or the mutual inductance between adjacent signal lines. This noise is generally increased as transition times and line spacings are decreased and as line lengths are increased. Lines with terminations 9a, 9b and 9d will typically exhibit more noise than those terminated with 9c and 9e.

Noise can easily become a very serious problem in memory design, but Figure 10 shows that adherence to a few simple guidelines will keep noise down to an acceptable level even under the most adverse conditions. First, use a ground plane or minimize the length of the ground trace from the driver to the memory chips. Second, use lots of decoupling capacitors (especially on two layer boards). Finally, if noise does become a problem, change to a different termination and/or driver.

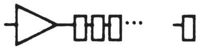
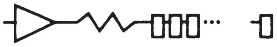
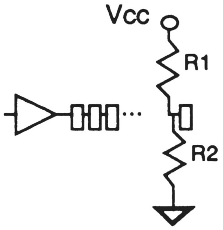
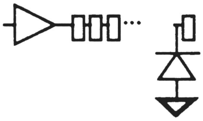
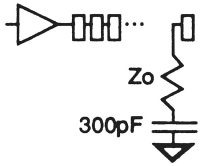
BRANCH INDUCED WAVEFORM DISTORTION

Infrequently, memory lines travel a considerable distance as a single line (several nanoseconds) and then branch into two or more directions. This can result in severe waveform distortion like that shown in Figure 11. In this example, a series terminated line travels 3ns as a single line and then splits into two parallel branches which are each 3ns long. The 2 volt incident wave travels down the line to the branch where the impedance of the line is effectively halved. At this point a reflection of $2\,V \times (.5\,Z_0 - Z_0)/(.5\,Z_0 + Z_0) = -.67$ volts travels back towards the driver, which drops the voltage of this first section of line back down from 2 volts to 1.3 volts. This section of the line stays at 1.3 volts for 6ns, at which point the reflections return from the unterminated ends of the two branches and bring the voltage back up above the input threshold again. The glitch seen at the driven end of this line would clearly be undesirable on any memory signal line.

Avoid long branches.

SUMMARY

The steadily increasing speed of memories, memory drivers and the systems these devices are being used in has created a need for engineers to understand, manipulate, subdue, or work around transmission line effects. This paper has presented the basic tools needed to accomplish this task, and it has given insight into where they are useful. Although several line driving and terminating techniques have been discussed, their individual advantages and disadvantages make it difficult to make general recommendations which are not tied to specific applications. The basic equations which govern transmission line behavior should augment the discussions on line driving and terminating techniques and their impact on undershoot and crosstalk, allowing the reader to adapt the ideas to his specific application.

 **Figure 9a**	Reflections	- Large, edge rate dependent
	Noise	- Poor
	Power	+ Low power
	Noise Margins	+ Large noise margins
	Hints	Often equivalent to 9b when driving SIPs or parallel banks of DIPs or Zips
 **Figure 9b**	Reflections	+ Limits or eliminates undershoot
	Noise	Poor on very low impedances, but good on higher impedances.
	Power	+ Low power
	Noise Margins	+ Good DC noise margins
		- Leaves signals in the threshold for 2T during transitions
	Hints	Increases setup times by 2T
 **Figure 9c**	Reflections	+ Limits or eliminates undershoot
	Noise	+ Low noise
	Power	- High power
	Noise Margins	- Usually has poor noise margins unless high current drivers are used
	Hints	Works well with high speed, high drive, open collector parts like the 74F3038 Only good for incident wave switched lines $Z_0 = R1R2/(R1+R2)$
 **Figure 9d**	Reflections	+ Typically limits undershoot to just less than a volt
	Noise	- Poor
	Power	+ Low power
	Noise Margins	+ Large noise margins once reflections have settled out -1 volt undershoot tends to reflect for several times the line delay which leaves the line somewhat susceptable to noise
	Hints	74F133 can be used as a diode pack. Avoid extremely fast edge rates.
 **Figure 9e**	Reflections	+ Limits or eliminates undershoot
	Noise	+ Good
	Power	+ Low DC power dissipation
	Noise Margins	+ Large noise margins
	Hints	Primarily for incident wave switched lines

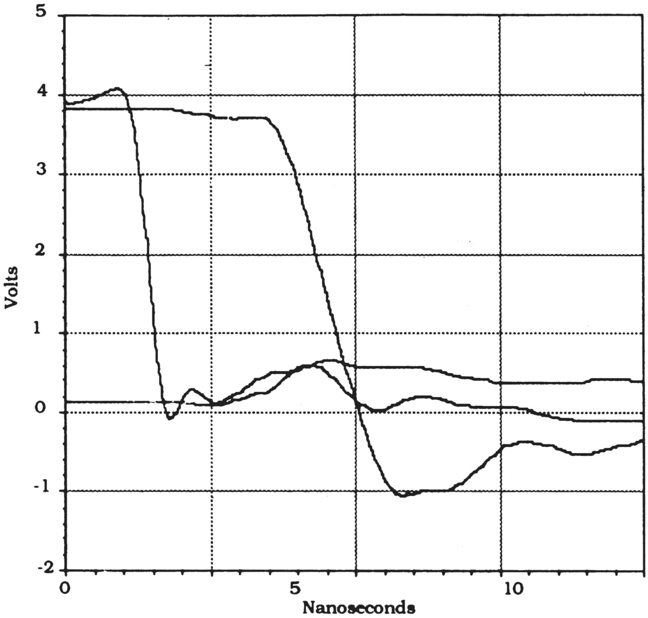


Figure 10 Two adjacent diode terminated lines driven by a 74F3037 on a dual layer Board. The sub-nanosecond edge rate of the driver does not induce excessive noise on the adjacent line even in this poor environment.

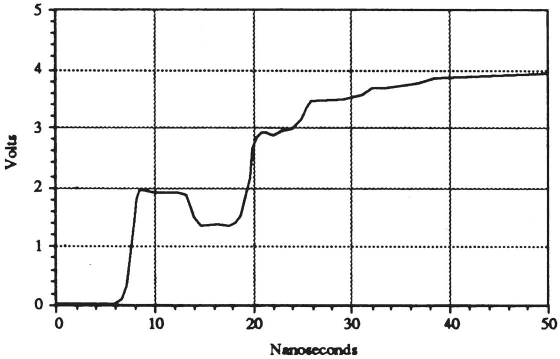


Figure 11 Branch induced waveform distortion

NOTES

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DATA HANDBOOK SYSTEM

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